Status of IP Fast Feedback Prototype

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- **FONT4 tests at KEK/ATF**
- **EM background tests at SLAC/ESA (T-488)**

FONT: Feedback On Nanosecond Timescales

Oxford + Daresbury:

Philip Burrows
Glenn Christian
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Tony Hartin
Alexander Kalinin
Colin Perry
Vice Glen White

Graduate students:
Christine Clarke
Christina Swinson
Ben Constance

SLAC, KEK, DESY, CERN

IP Intra-train Feedback Concept

Vibrations/noise cause beams to miss one another

Kick beam back into collision

e+

e-

Outgoing beams deflected

Measure beam position

Feedback circuit

'Intra-train' FB

smaller detector

smaller L*

QD0

warm

QF1

vacuum
connection
& feedback
kicker

common cryostat

larger detector

larger L*
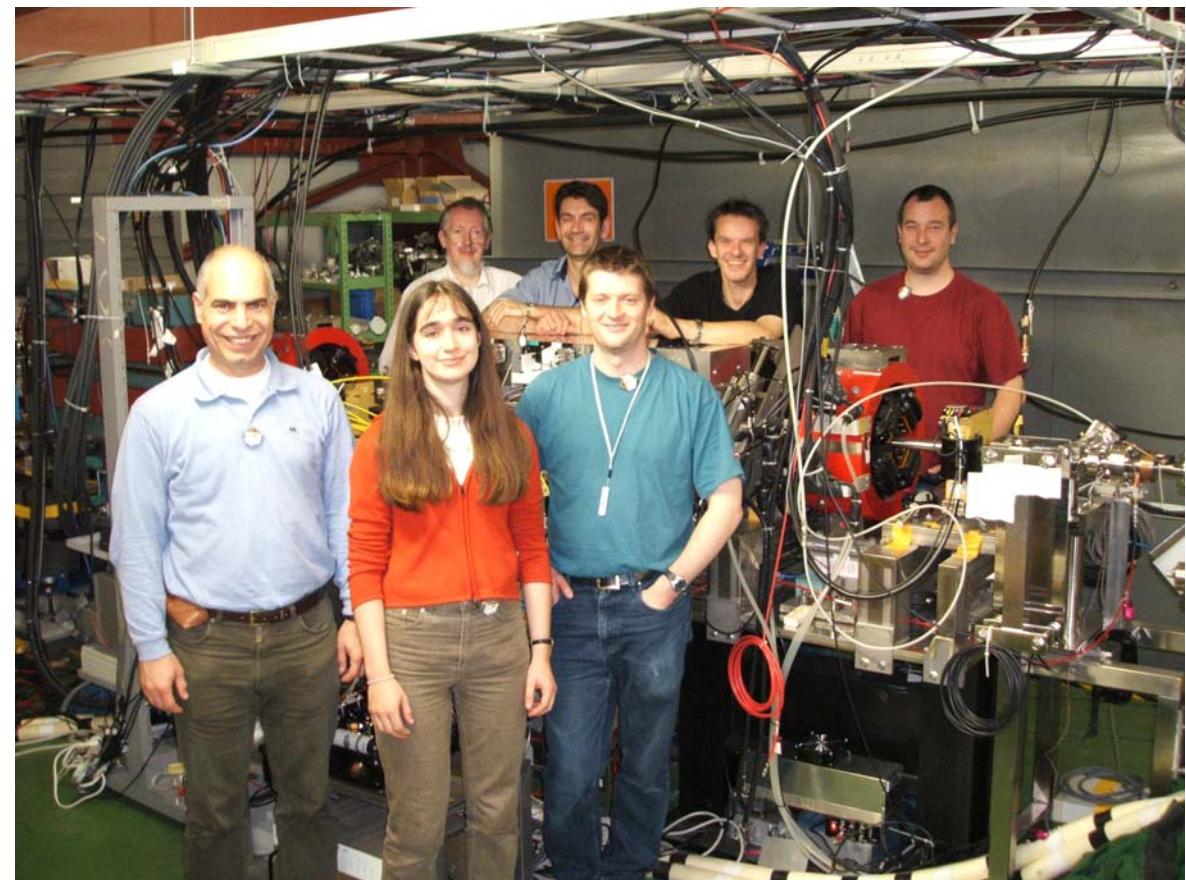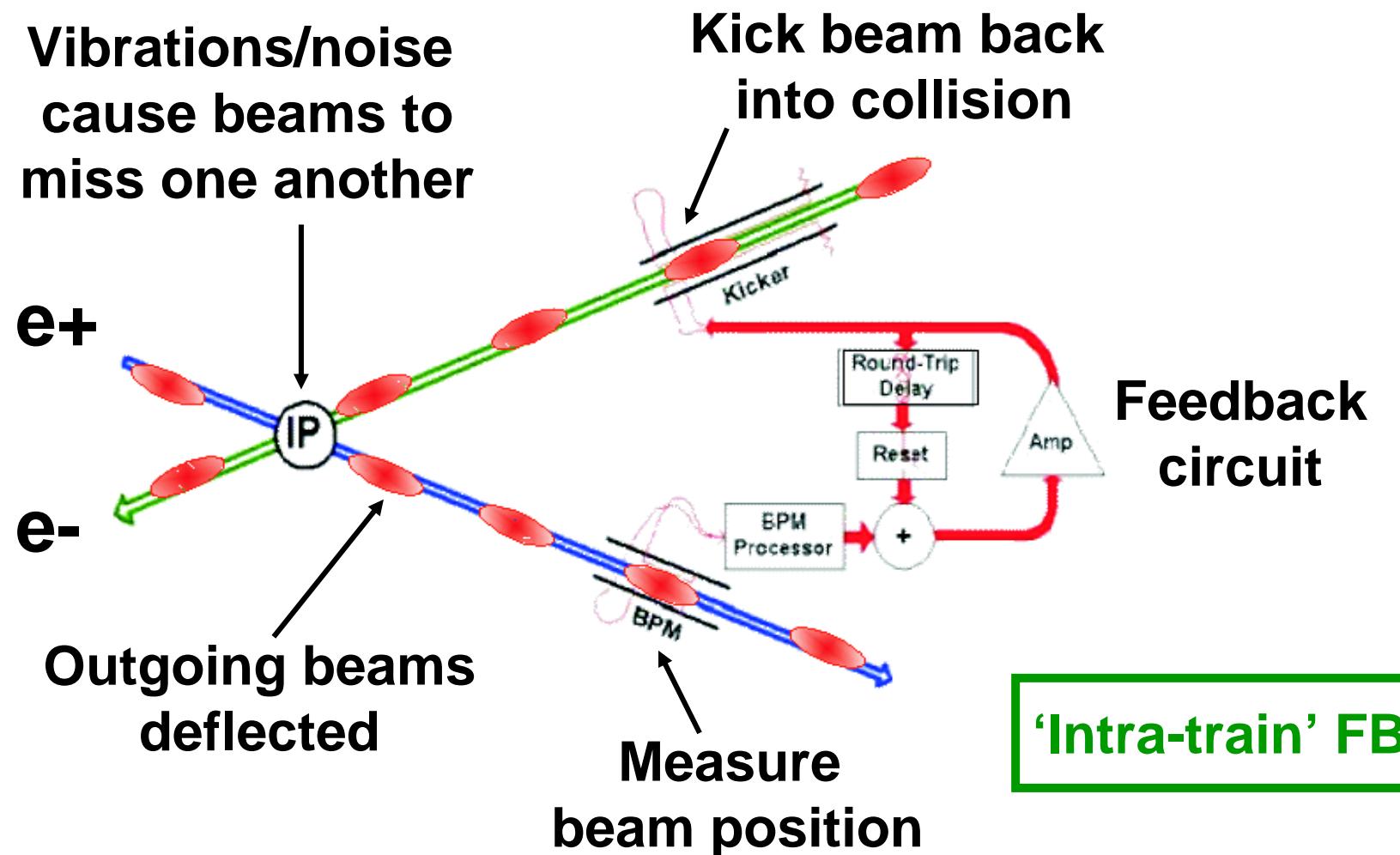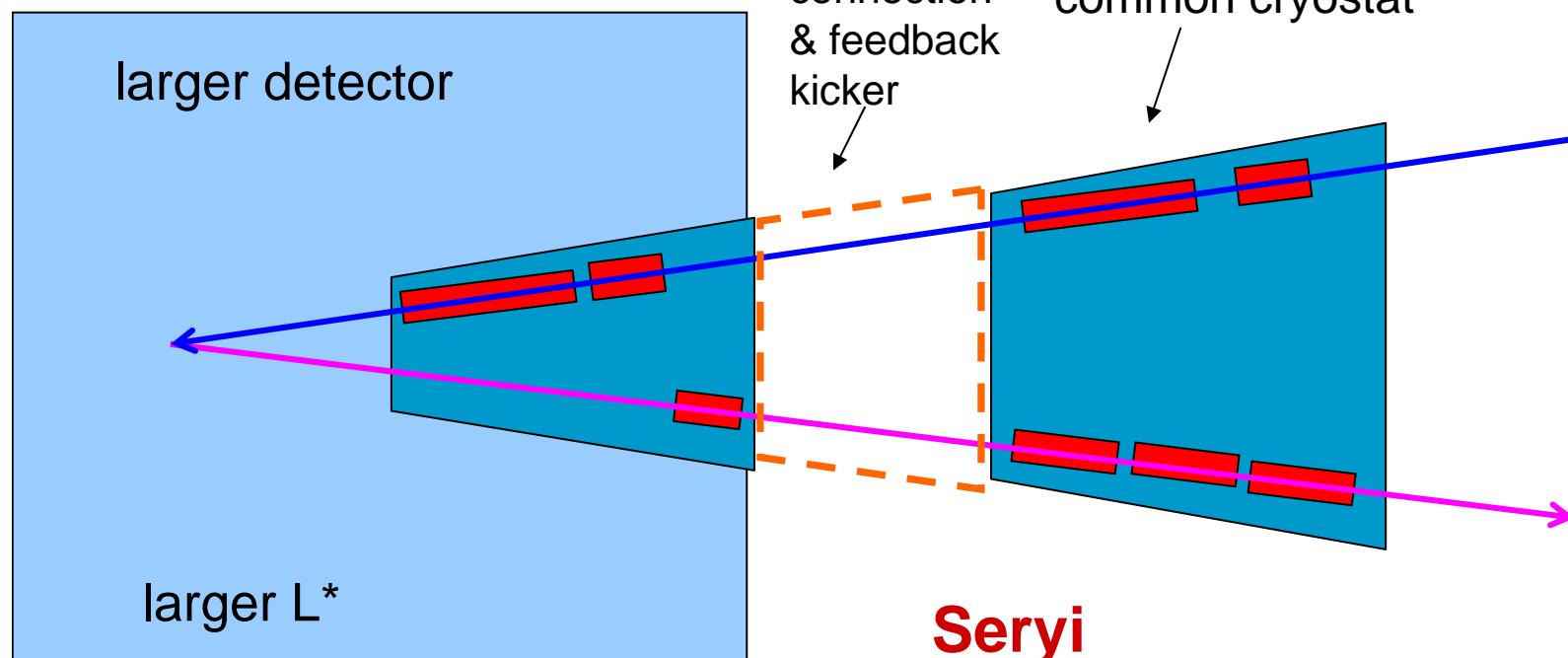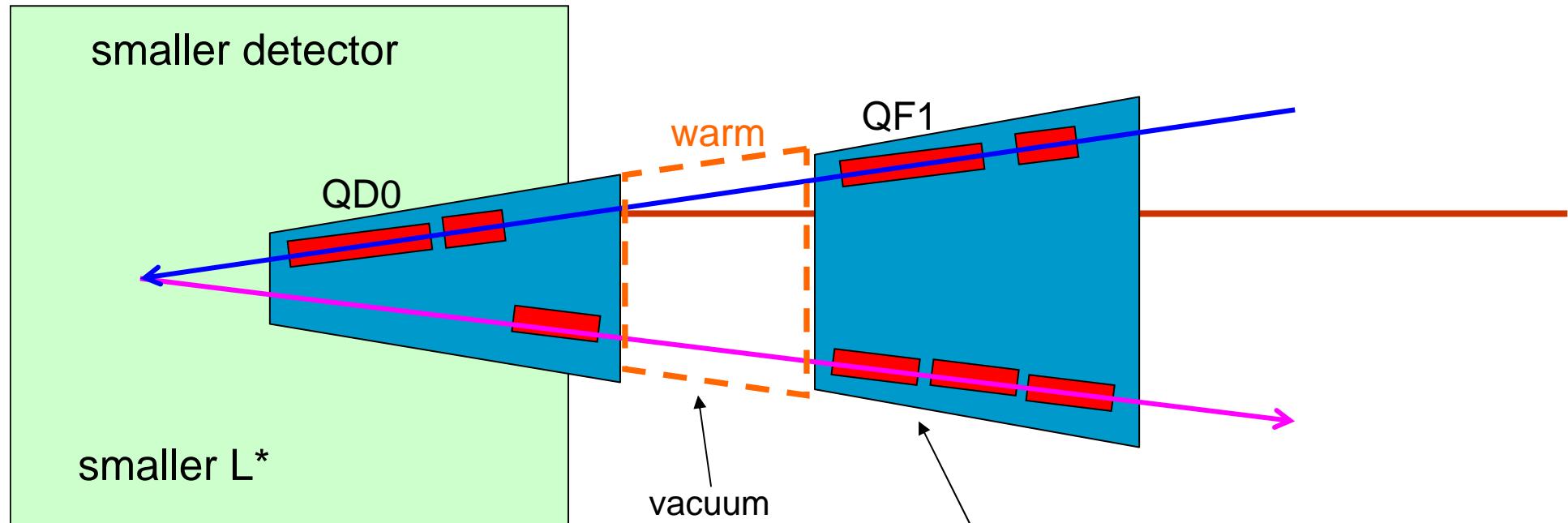
Seryi

P.N. Burrows

ECFA/GDE Meeting, BDIR session, Valencia, 9/11/06

ILC digital feedback prototype (FONT4)
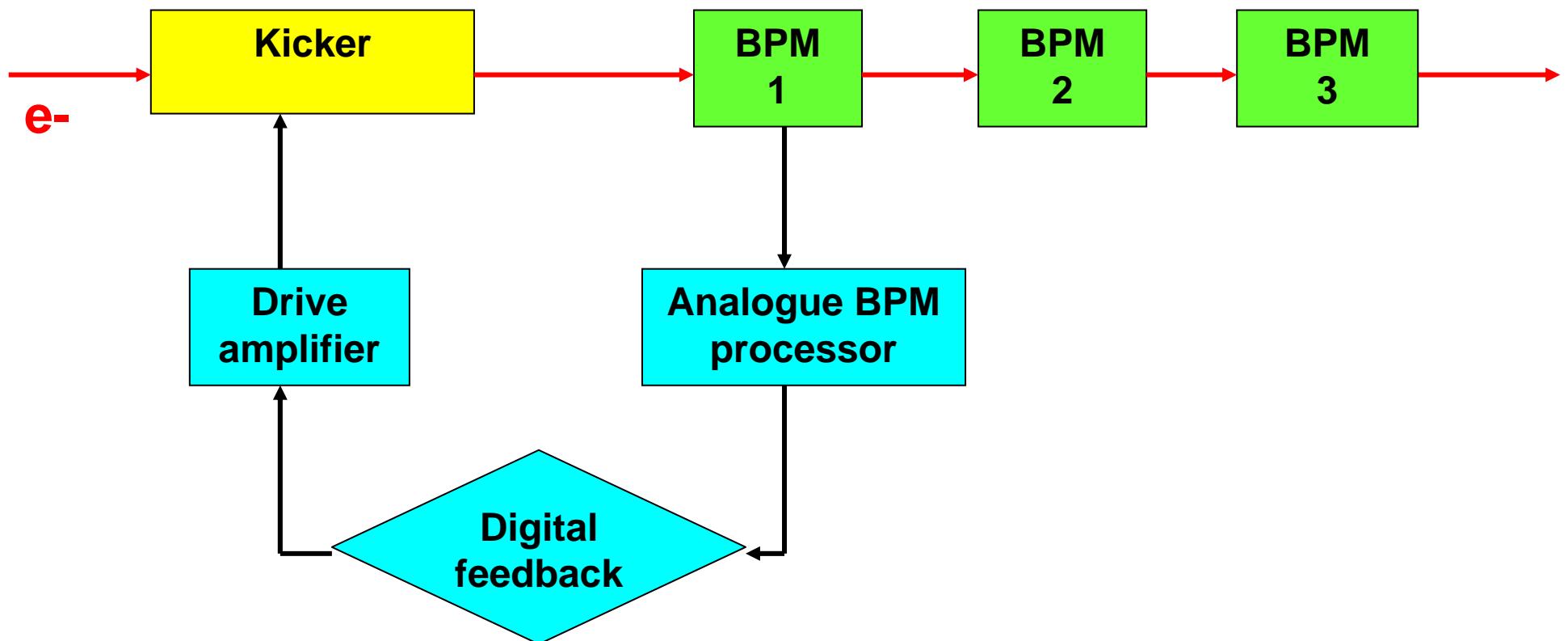
FONT4: latency budget

- **Time of flight kicker – BPM:**   **7ns**
- **Signal return time BPM – kicker:**   **15ns**
  - **Irreducible latency:**   **22ns**

- **BPM processor:**   **7ns**
- **ADC/DAC (3.5 89 MHz cycles)**   **40ns**
- **Signal processing (8 357 MHz cycles)**   **25ns**
- **FPGA i/o**   **3ns**
- **Amplifier**   **40ns**
- **Kicker fill time**   **3ns**
  - **Electronics latency:**   **118ns**

- **Total latency budget:**   **140ns**

FONT4 hardware

e-

Kicker

BPM 1

BPM 2

BPM 3

Drive amplifier

Analogue BPM processor

Digital feedback

In fabrication by TMD
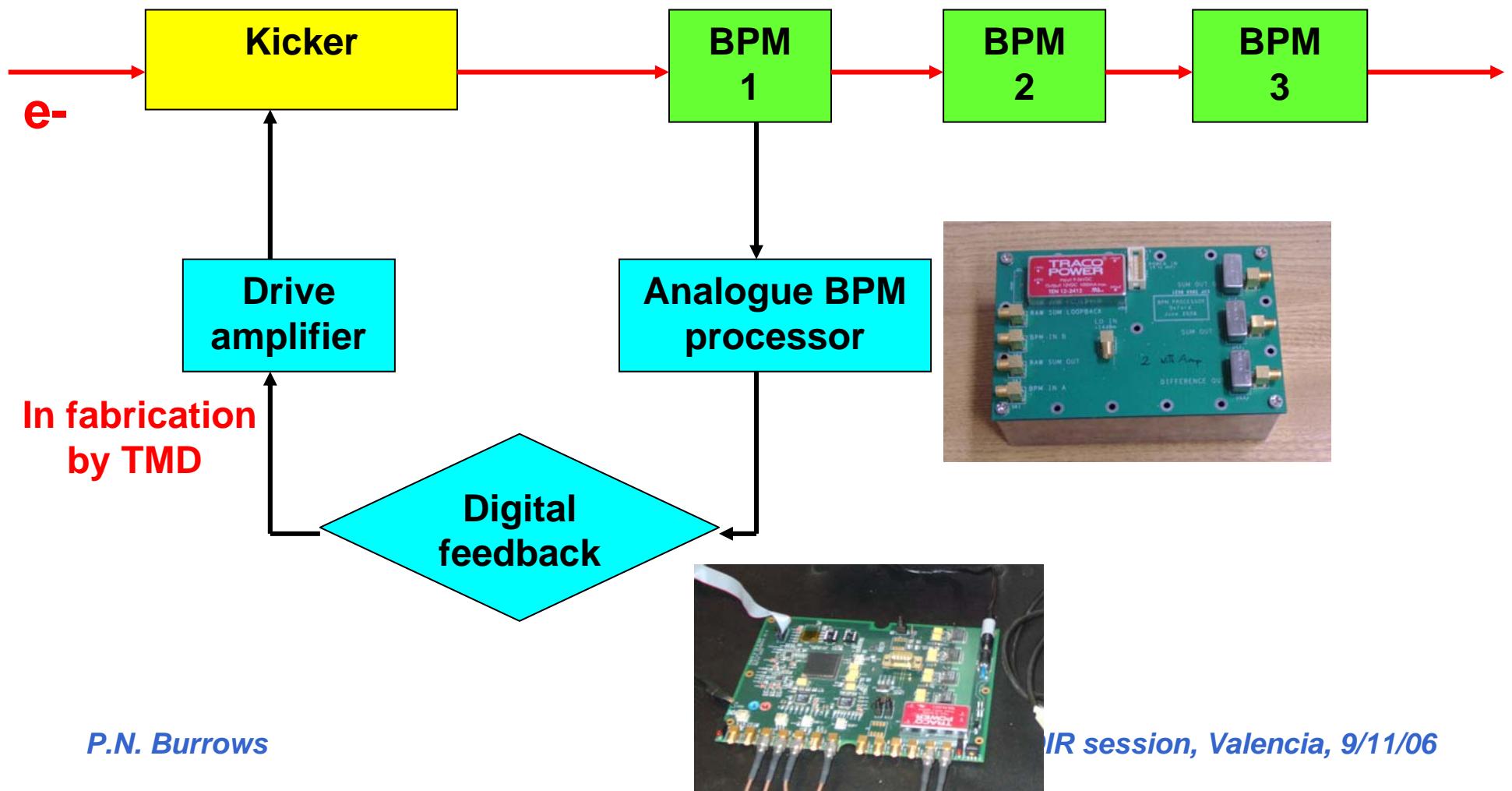
# FONT beamline at KEK ATF

(1.3 GeV 3-bunch train w. spacing c.150ns)

BPM processor board
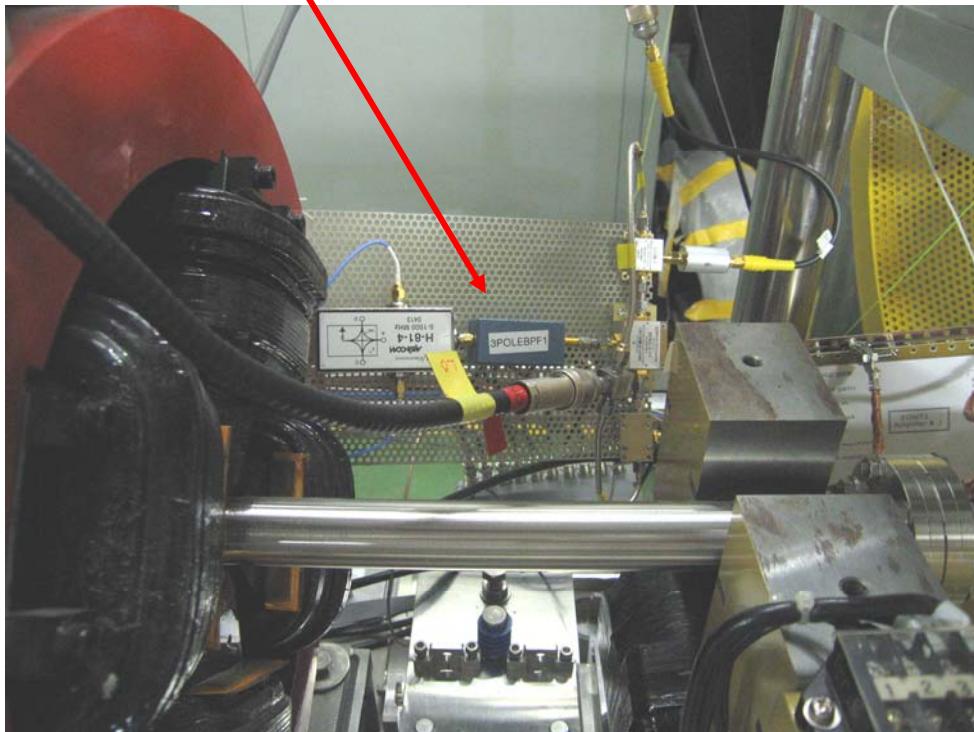
FEATHER kicker

Amplifier/FB board
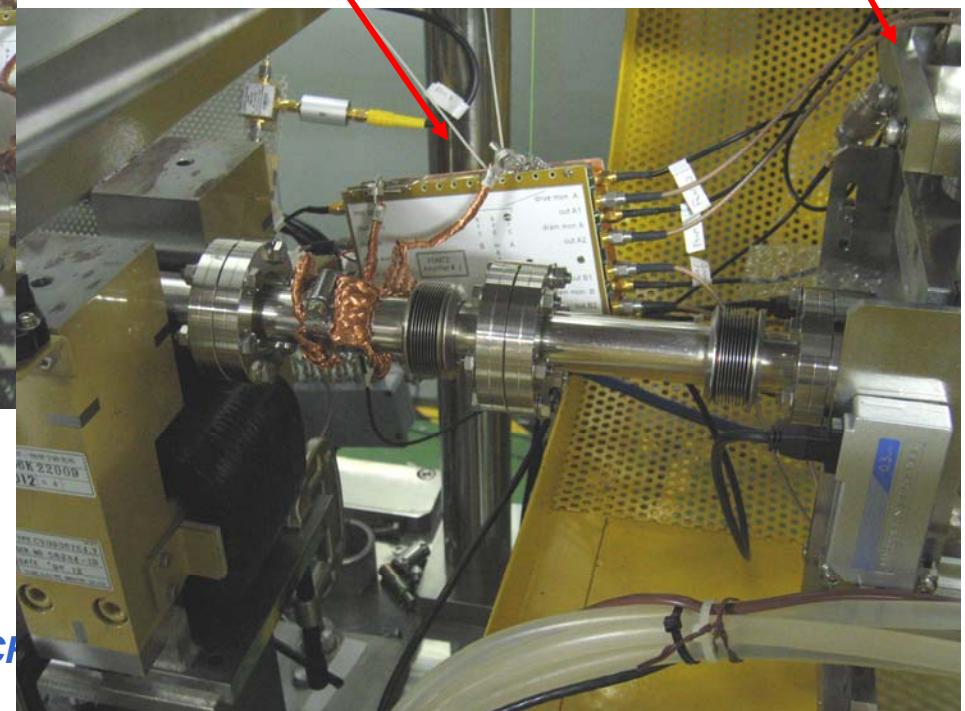
FONT4 initial beam tests (June 2006)
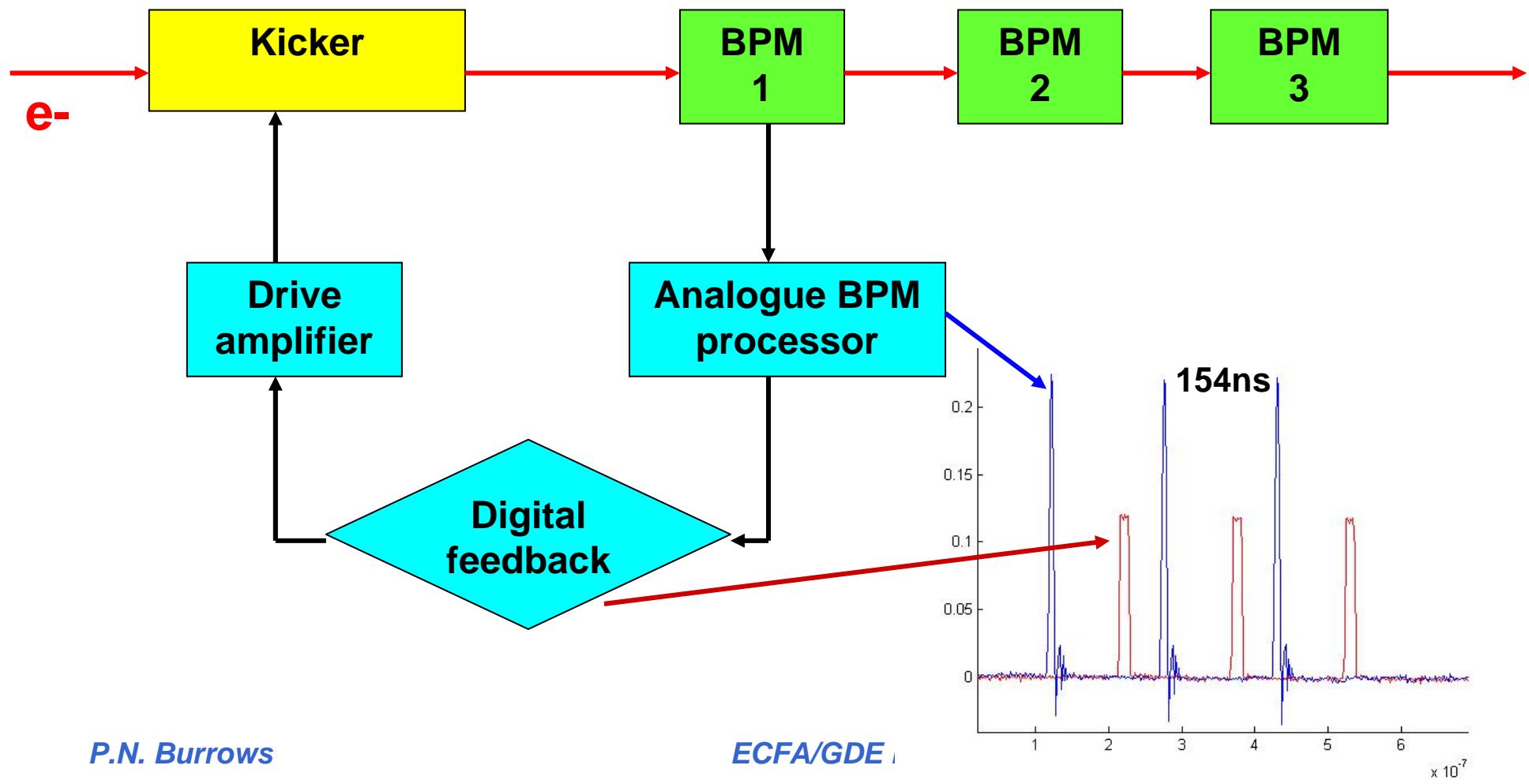
FONT4 test plan

June 2006:

    1st test of PCB version of analogue BPM processor

    2nd tests of digital FB: timing, synchronisation, triggering,
        gain adjustment in FPGA
        (ADC clocking @ 714/10 = 71 MHz)

November 2006:

    3rd tests of digital FB: ADC clocking @ 357/4 = 90 MHz

    2nd tests of (modified) PCB BPM processor

January – March 2007:

    1st test of FONT4 amplifier

    Closed-loop FB

2007-2008:

    Develop into 'turnkey' system

2009-2010:

   Deploy x, x', y, y' system at ATF2

Oxford test bench setup

Oxford test bench setup

ILC interaction region
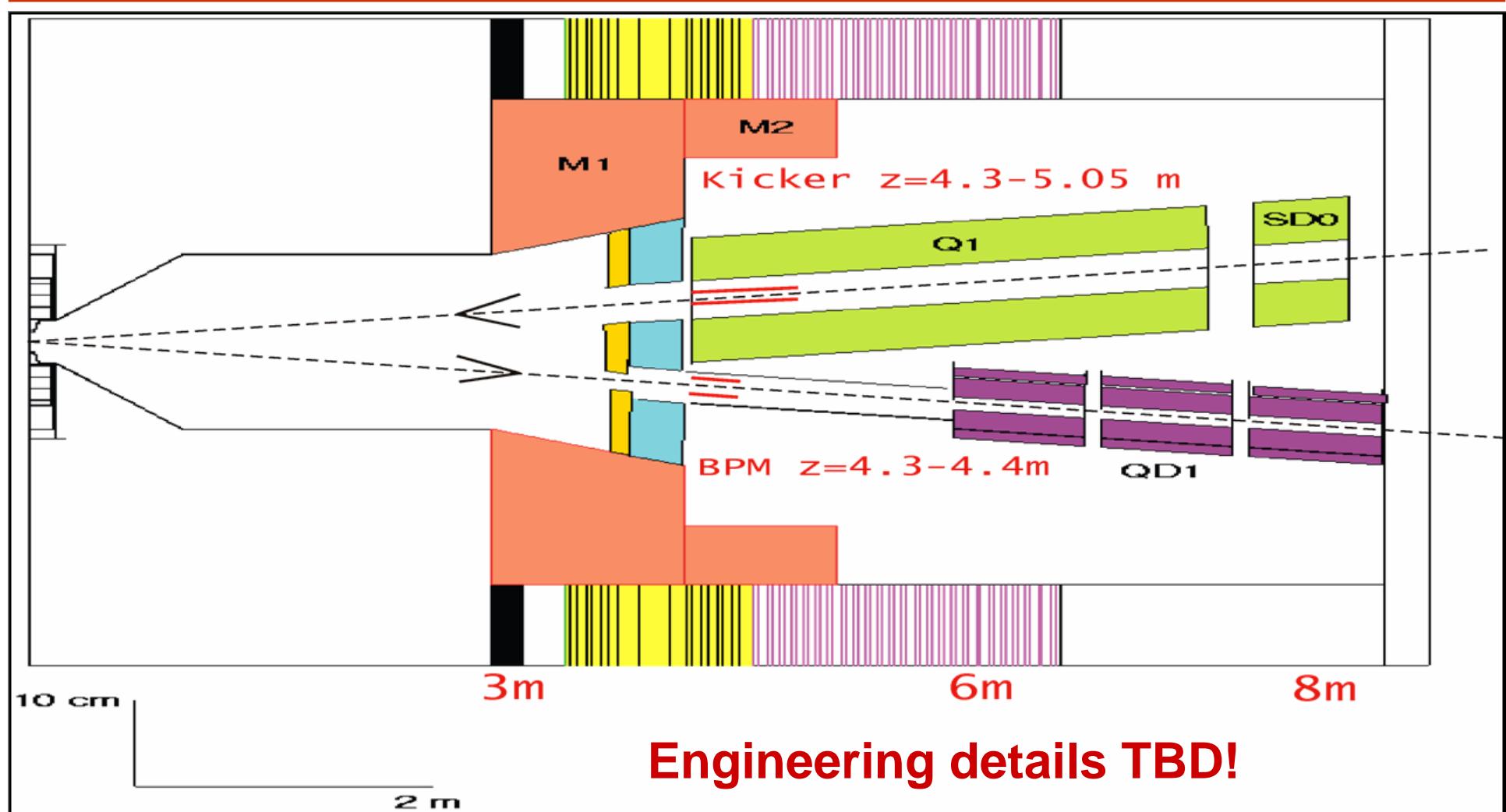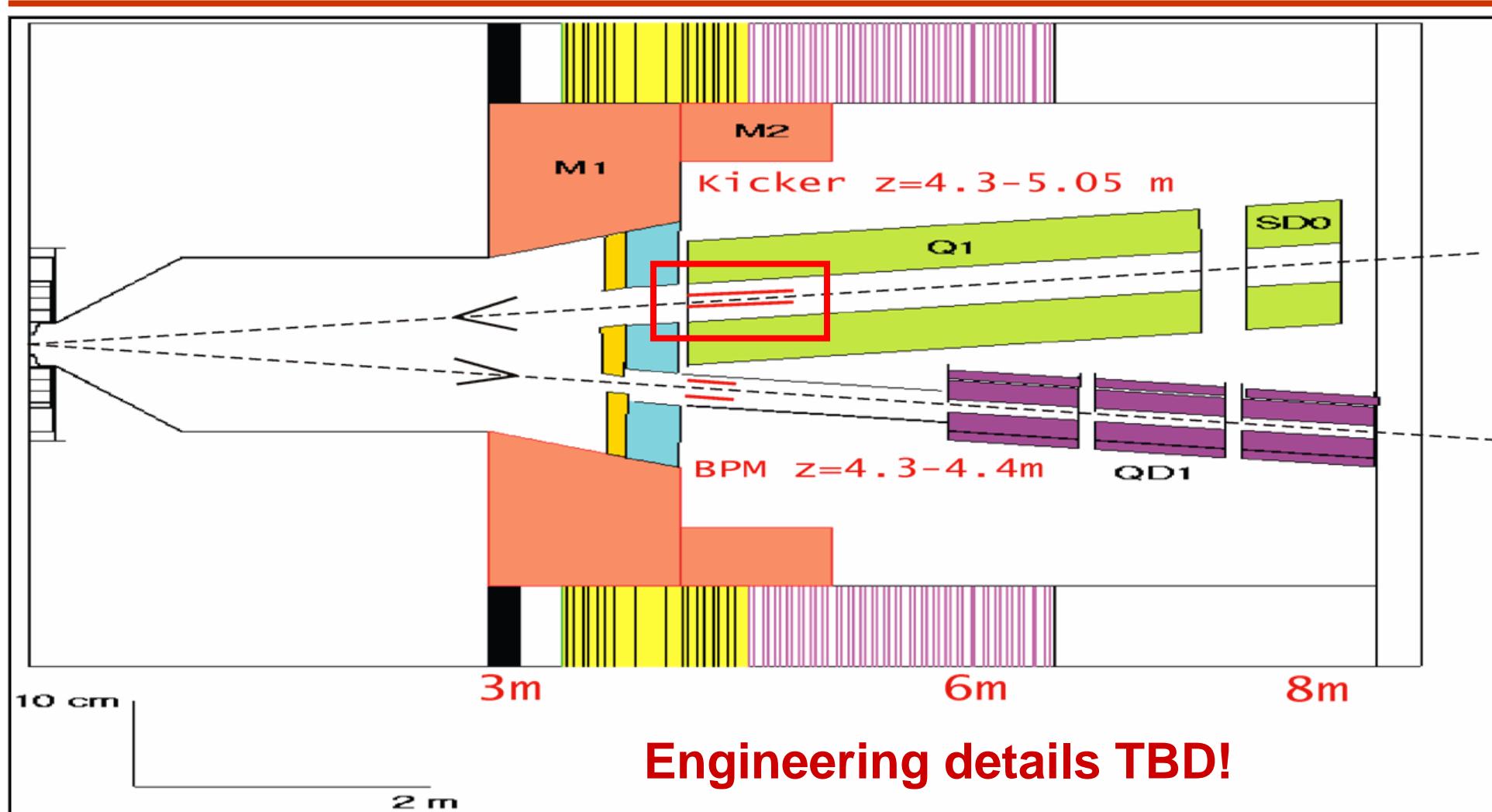
Labels within figure:
M2
M1
Kicker z=4.3-5.05 m
SD0
Q1
BPM z=4.3-4.4m
QD1
10 cm
3m
6m
8m
2 m

Engineering details TBD!

Nominal IP feedback hardware locations

Kicker z=4.3-5.05 m

BPM z=4.3-4.4m

M1

M2

SD0

Q1

QD1

3m

6m

8m

10 cm

2 m

Engineering details TBD!

Nominal IP feedback hardware locations

Engineering details TBD!

Pair-induced EM backgrounds

Low Z mask

e+e- pairs

BPM

Pair-induced EM backgrounds

Low Z mask

Density of BPM Spray Primaries

e+e- pairs

BPM
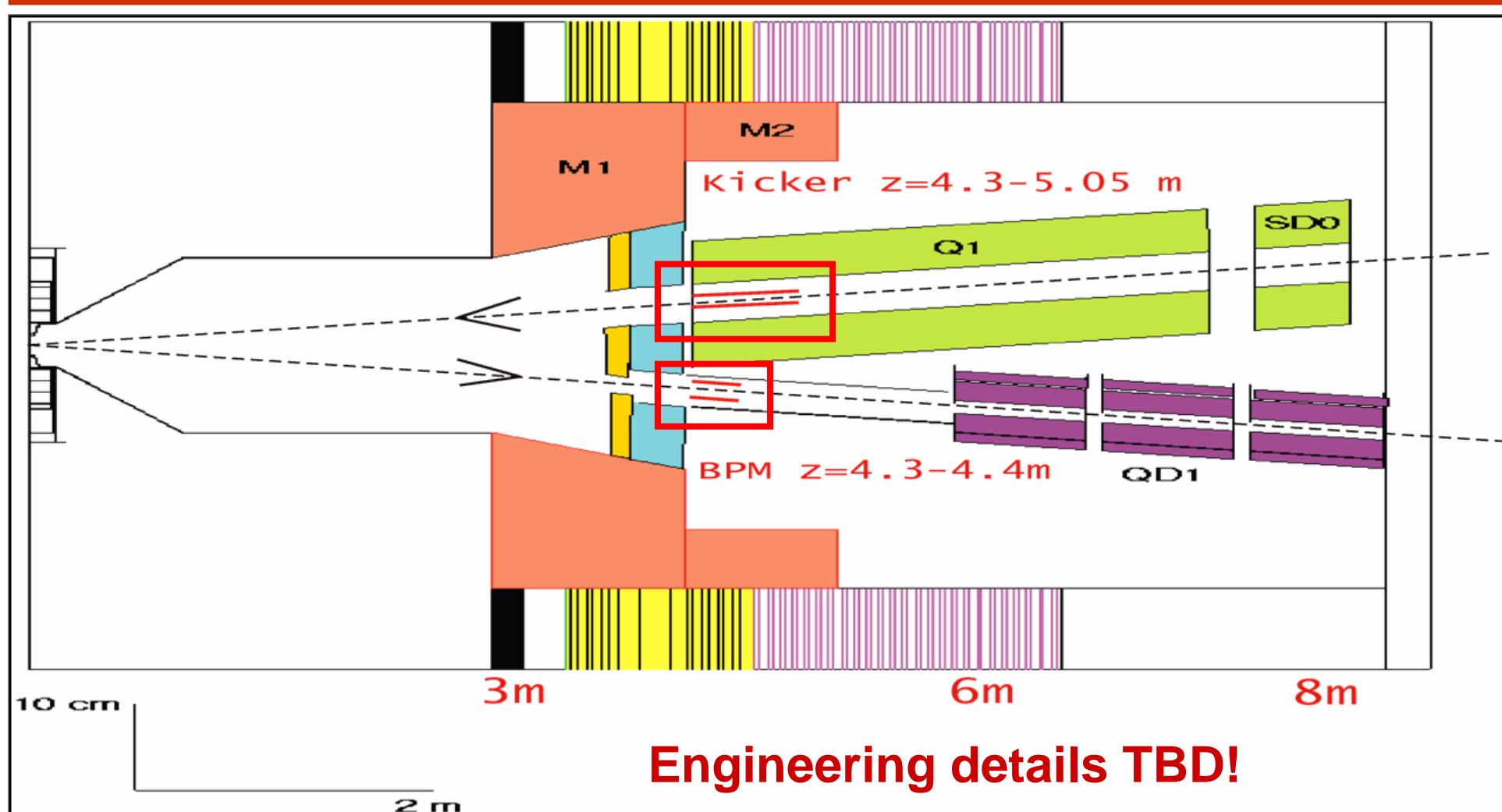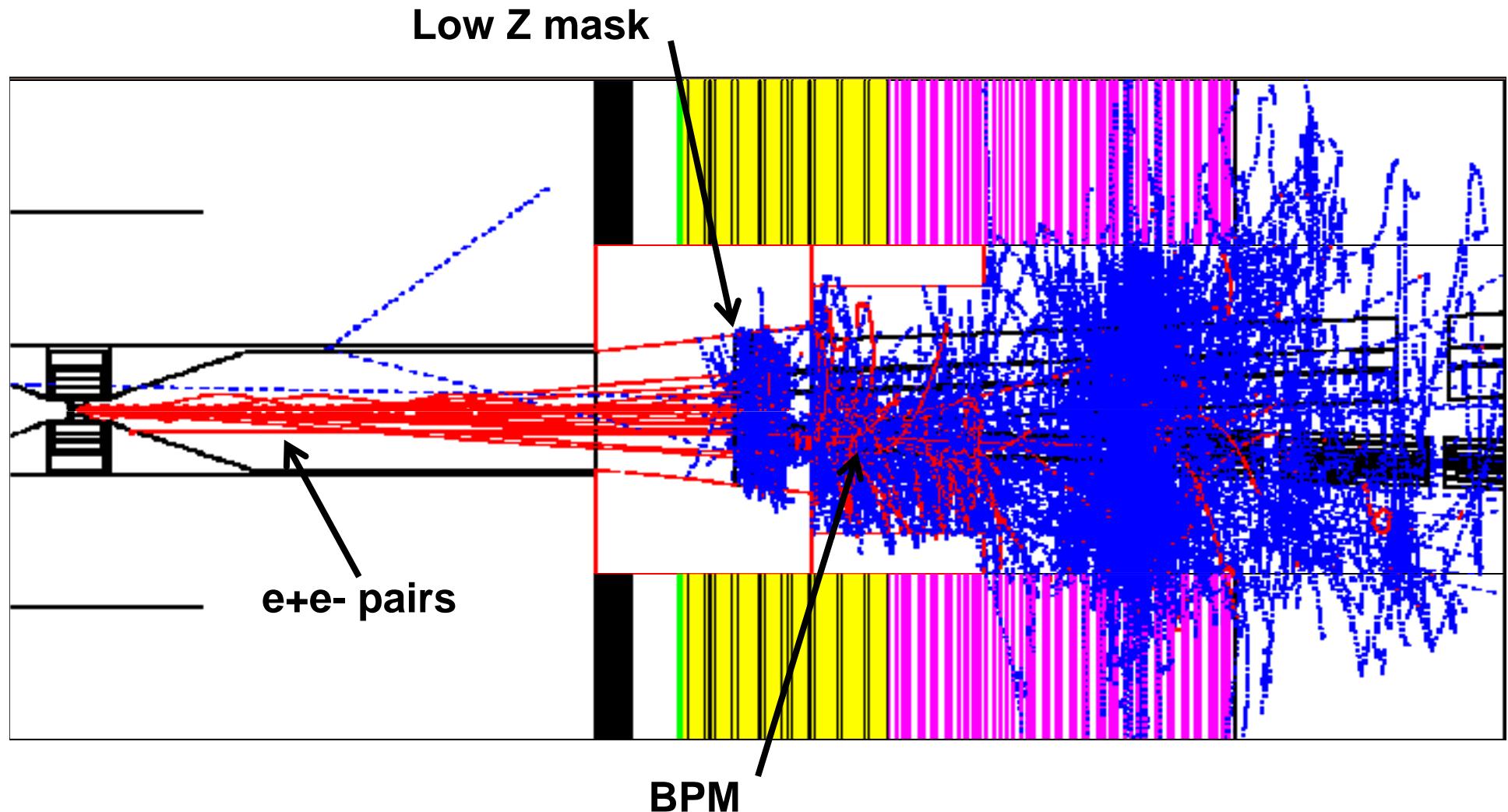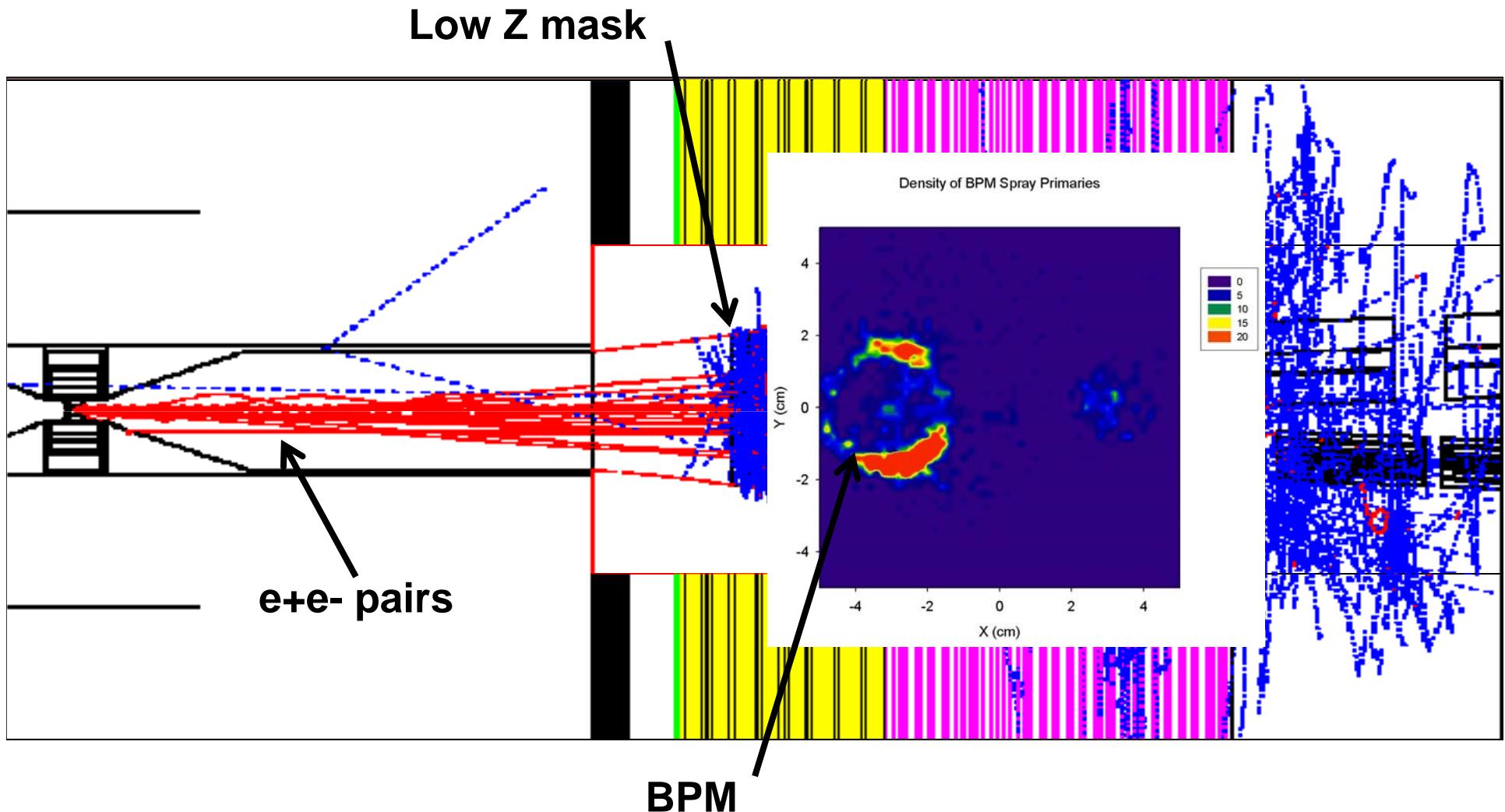
FONT Test Module for ESA
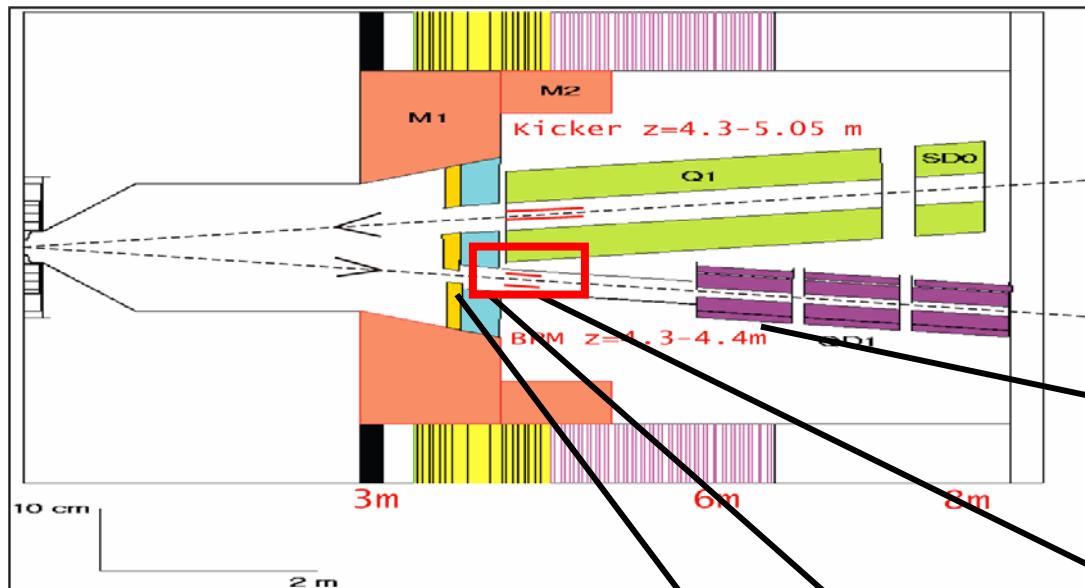
Material model
of ILC outgoing
beamline

QFEX1

BPM

beamcal

low Z
mask

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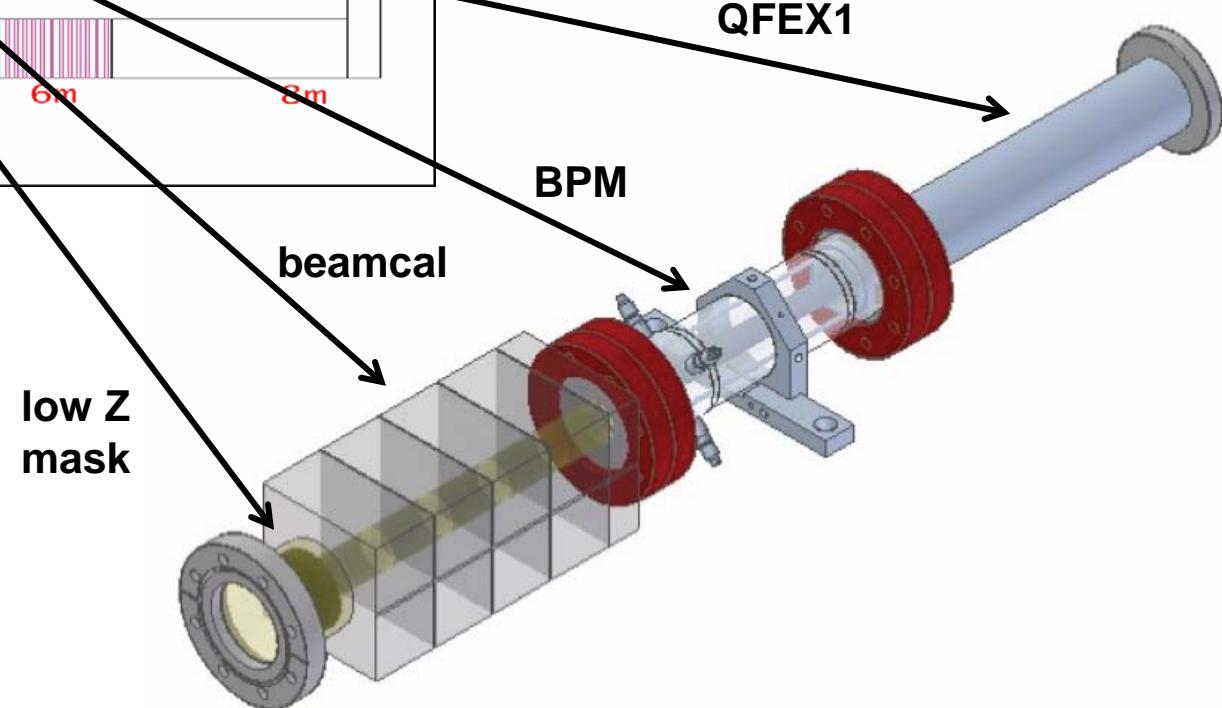
FONT Test Module (T-488)
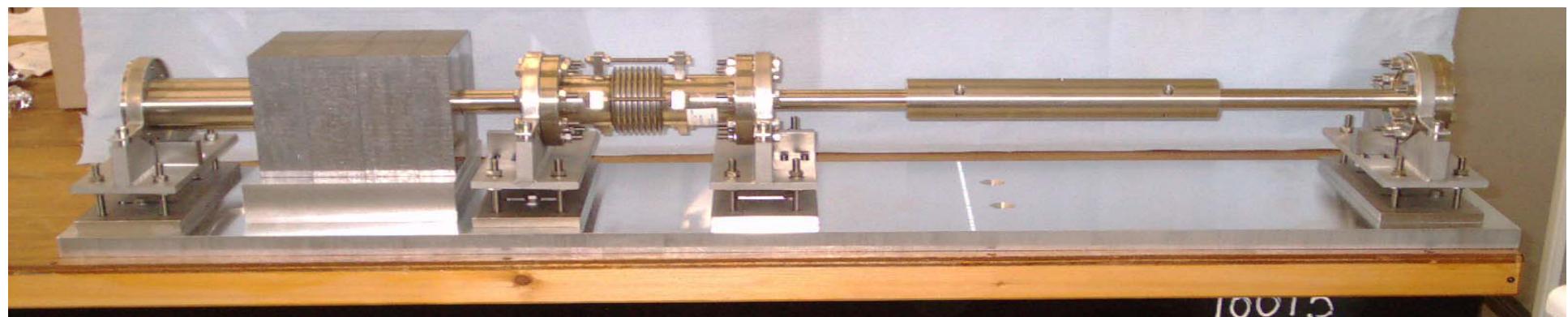
Beam

Installation at ESA
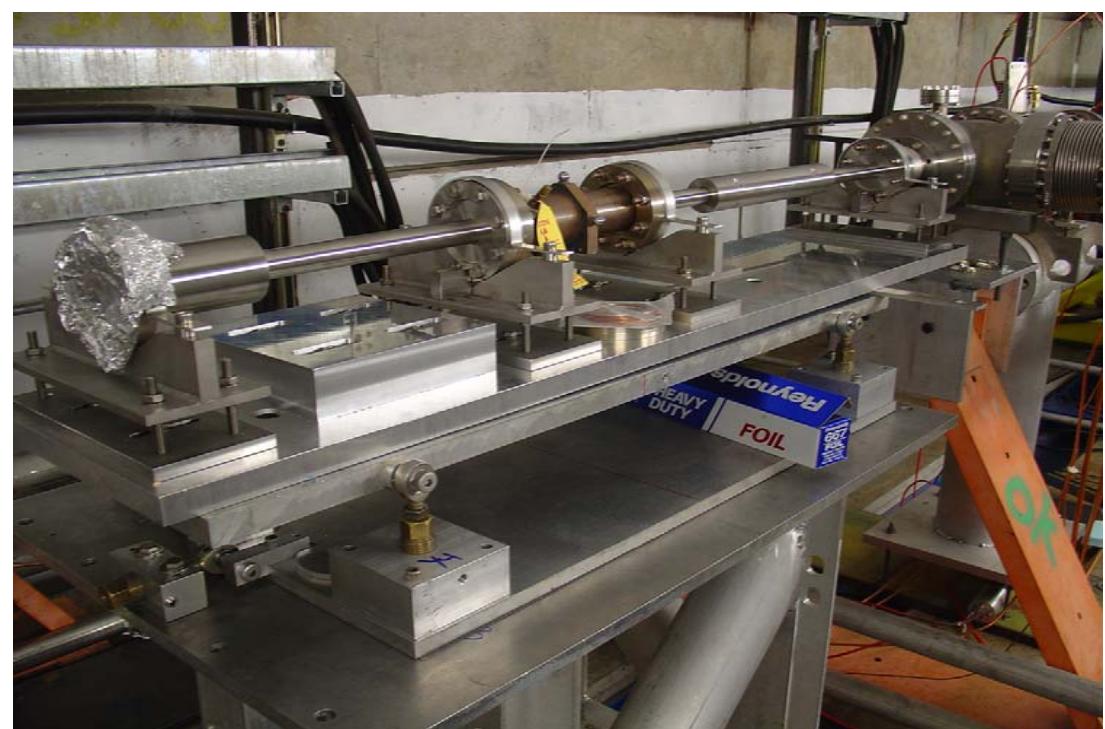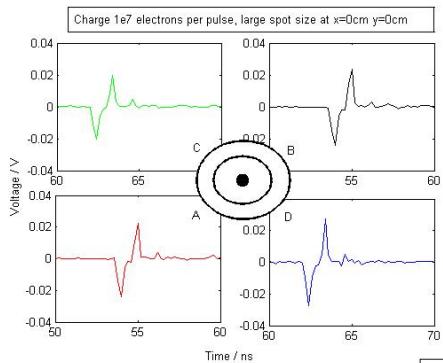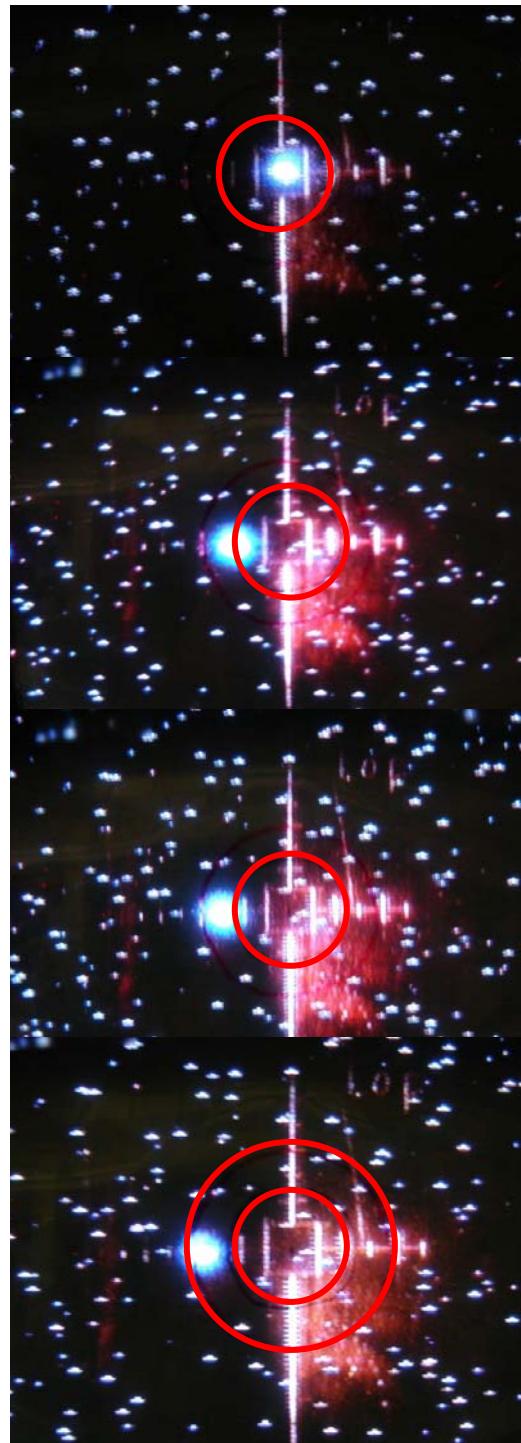
Beam scan across module
(12 Jul 06)
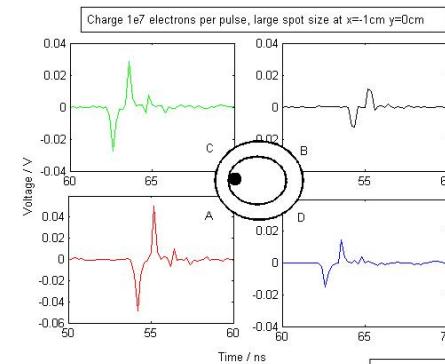
107 beam**
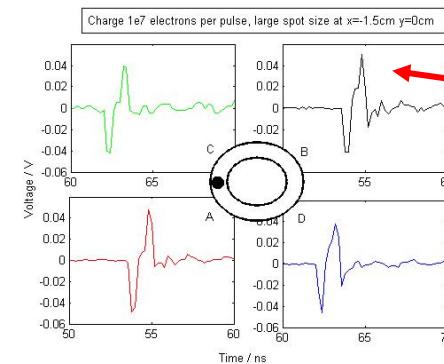
Noticeable degradation of signals
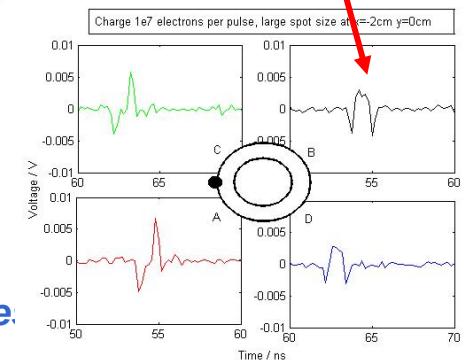
Modelling in progress

# Modelling of ESA data

- **Primary beam simulation and transport (MAD)**

- **Generate showering in module (GEANT3); track shower particles to BPM**

- **Simulate response of BPM to noise hits**

**Beam scan across module**

Total charges at upstream end

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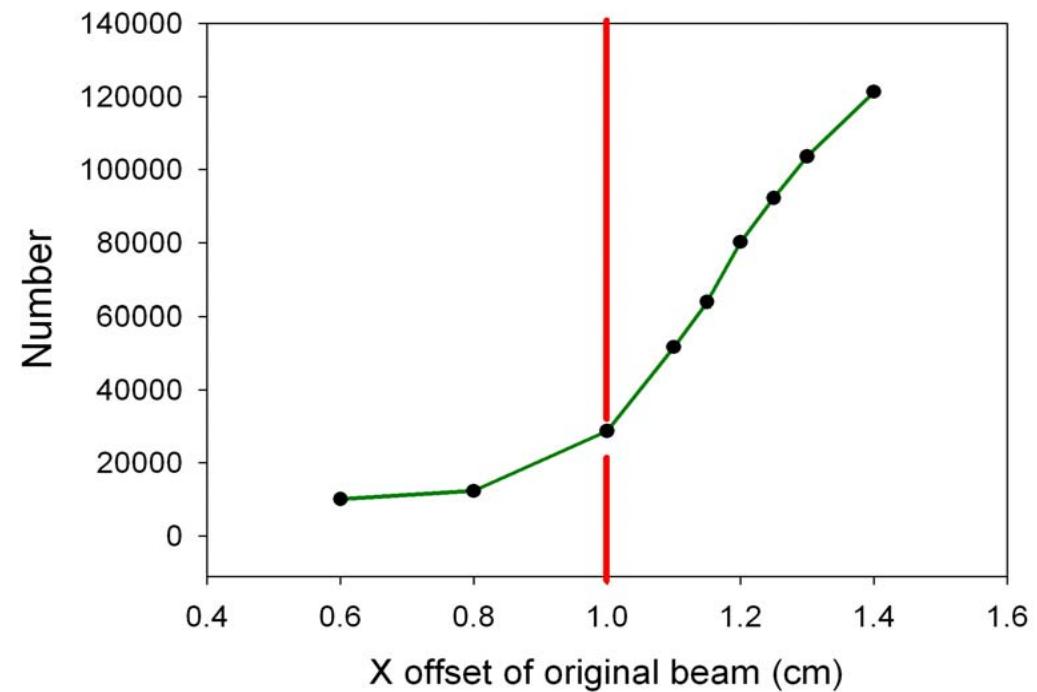
Modelling of noise on BPM strips

BPM wall

BPM strip

"noise" voltage pulse

Charges incident on strips
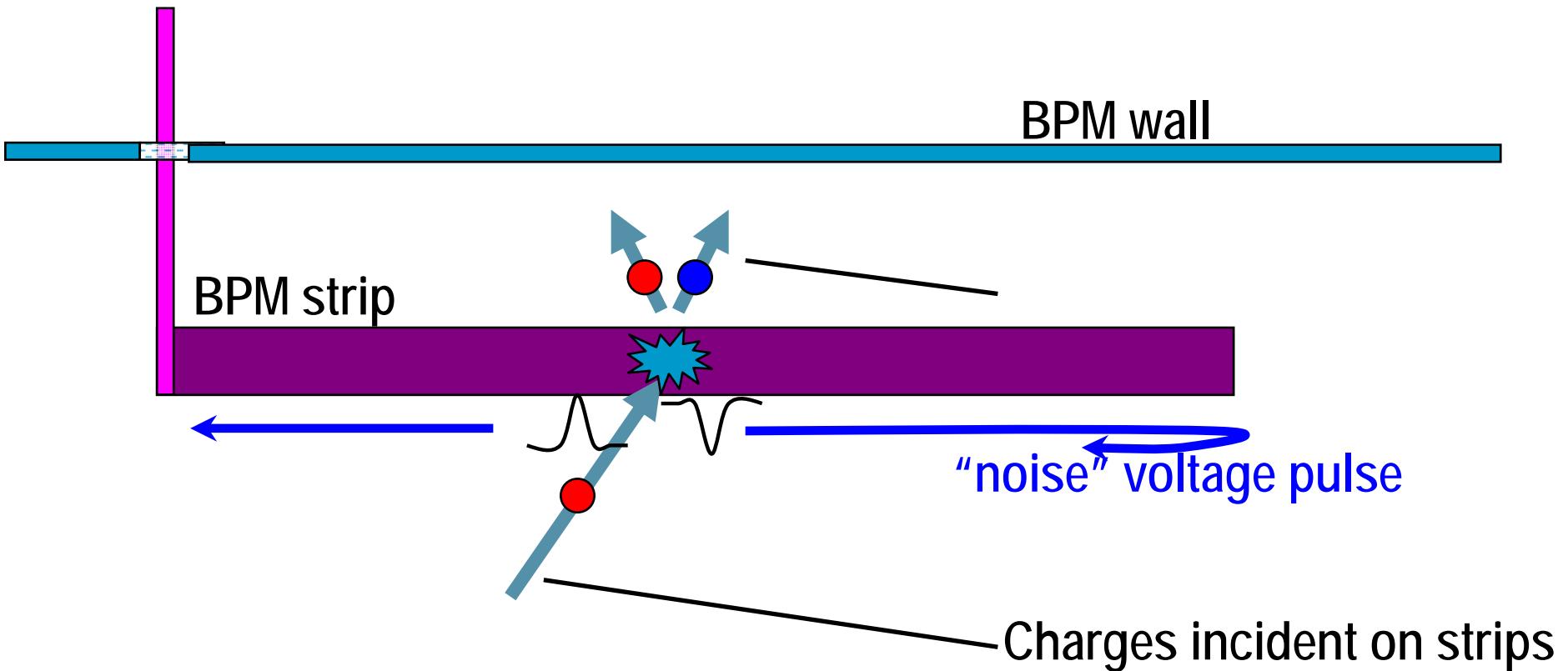
Simple time-of-flight analysis

**Primary beam signal**
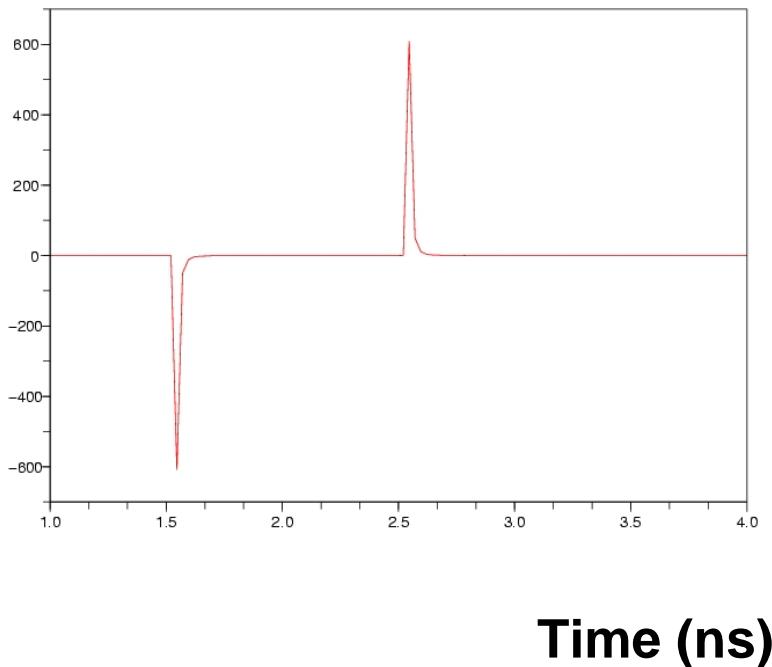
**Example of noise (for illustration only)**


Time (ns)
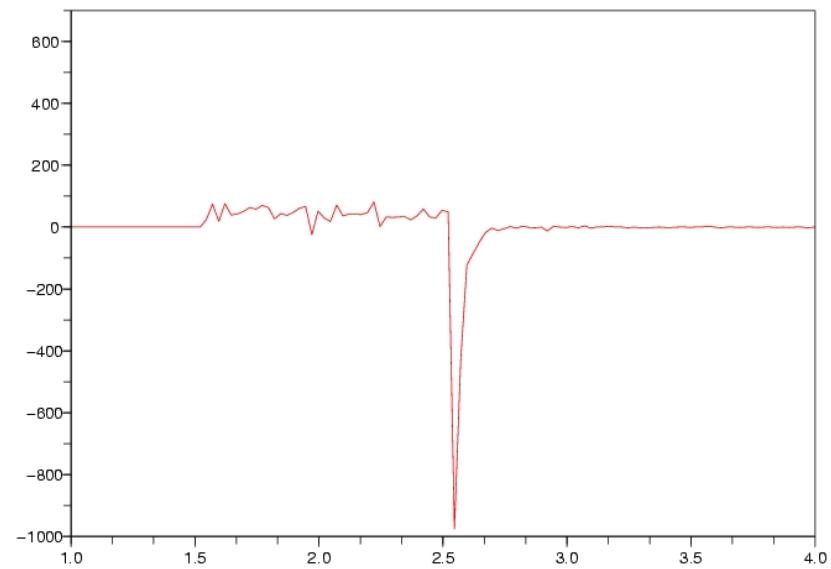
Simulated signal + noise results
## (work in progress)
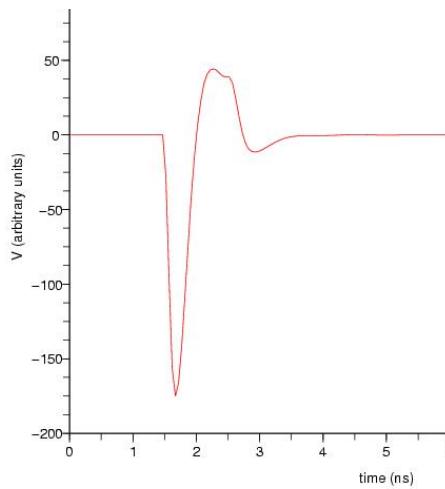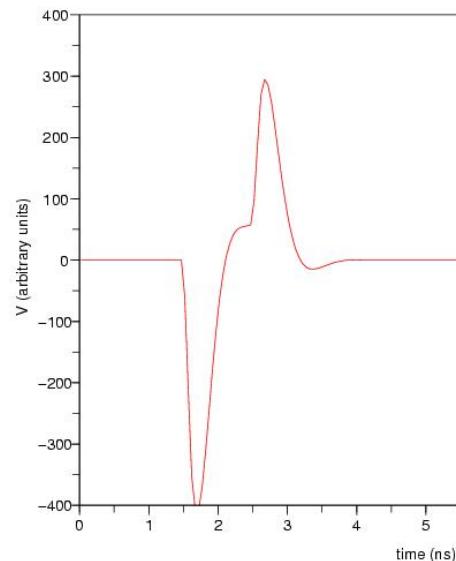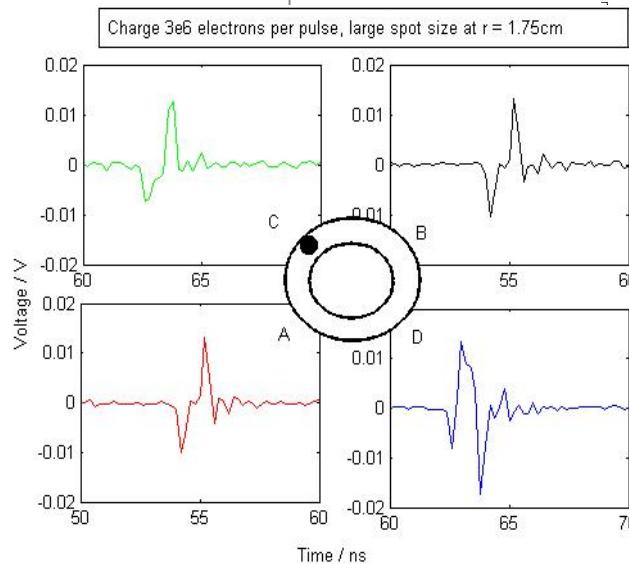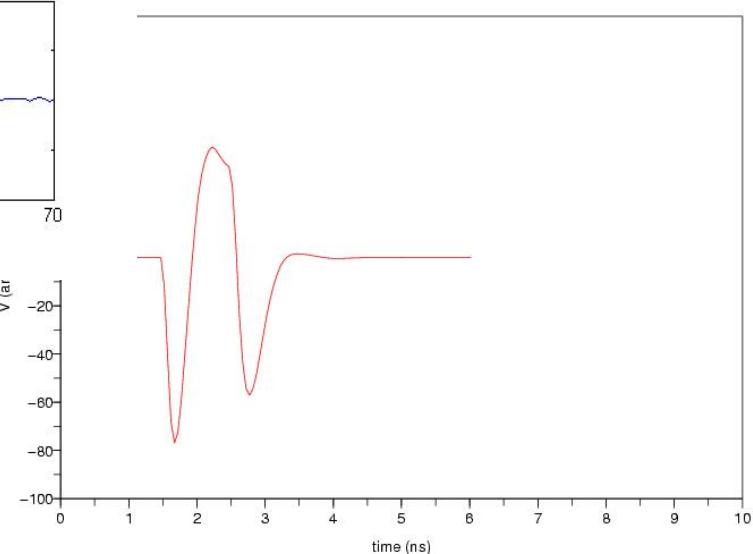
Example showing beam scan vs. data

data at x=1.75
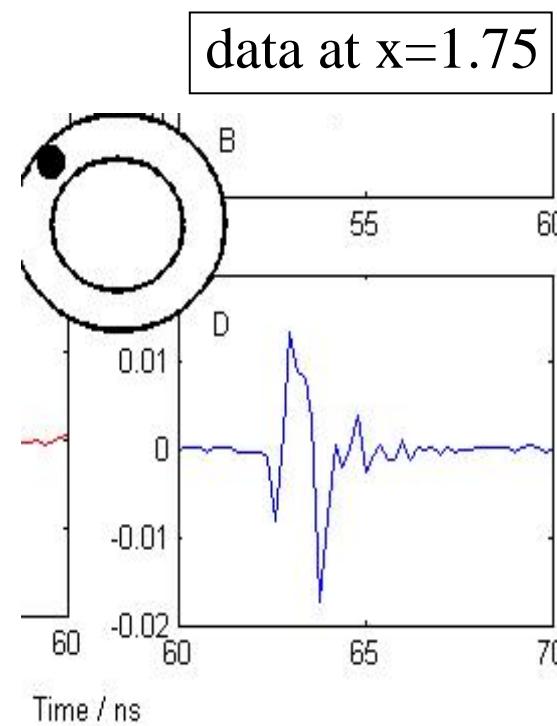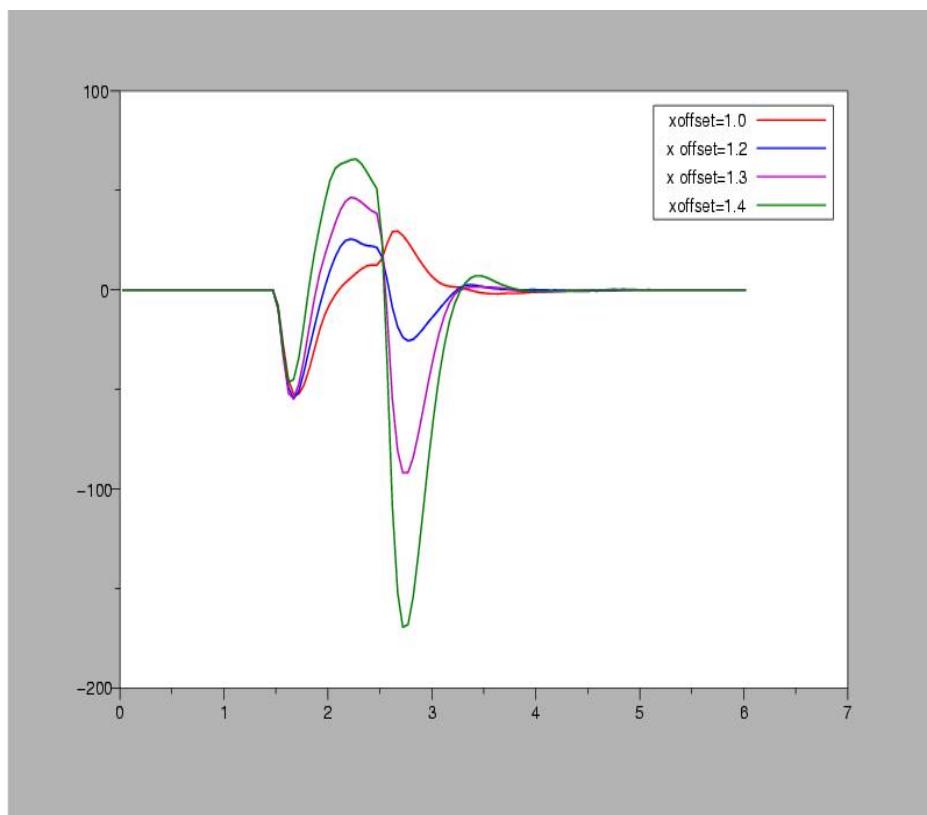
Details seem to matter
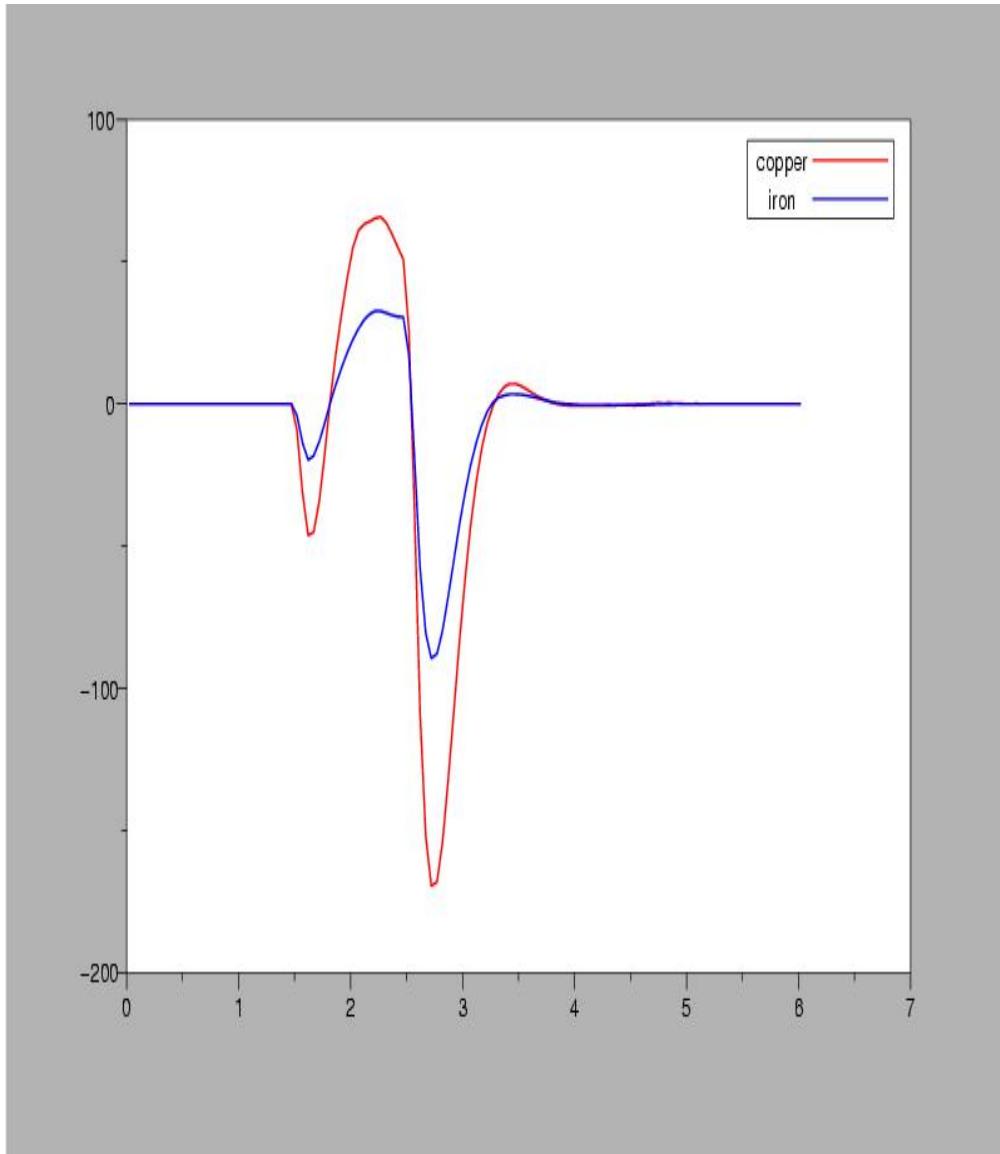
Study of copper vs steel striplines

(5000 input electrons)

Watch this space for further developments… Particle Studio code being used for better signal modelling