Review on SiLC R&D

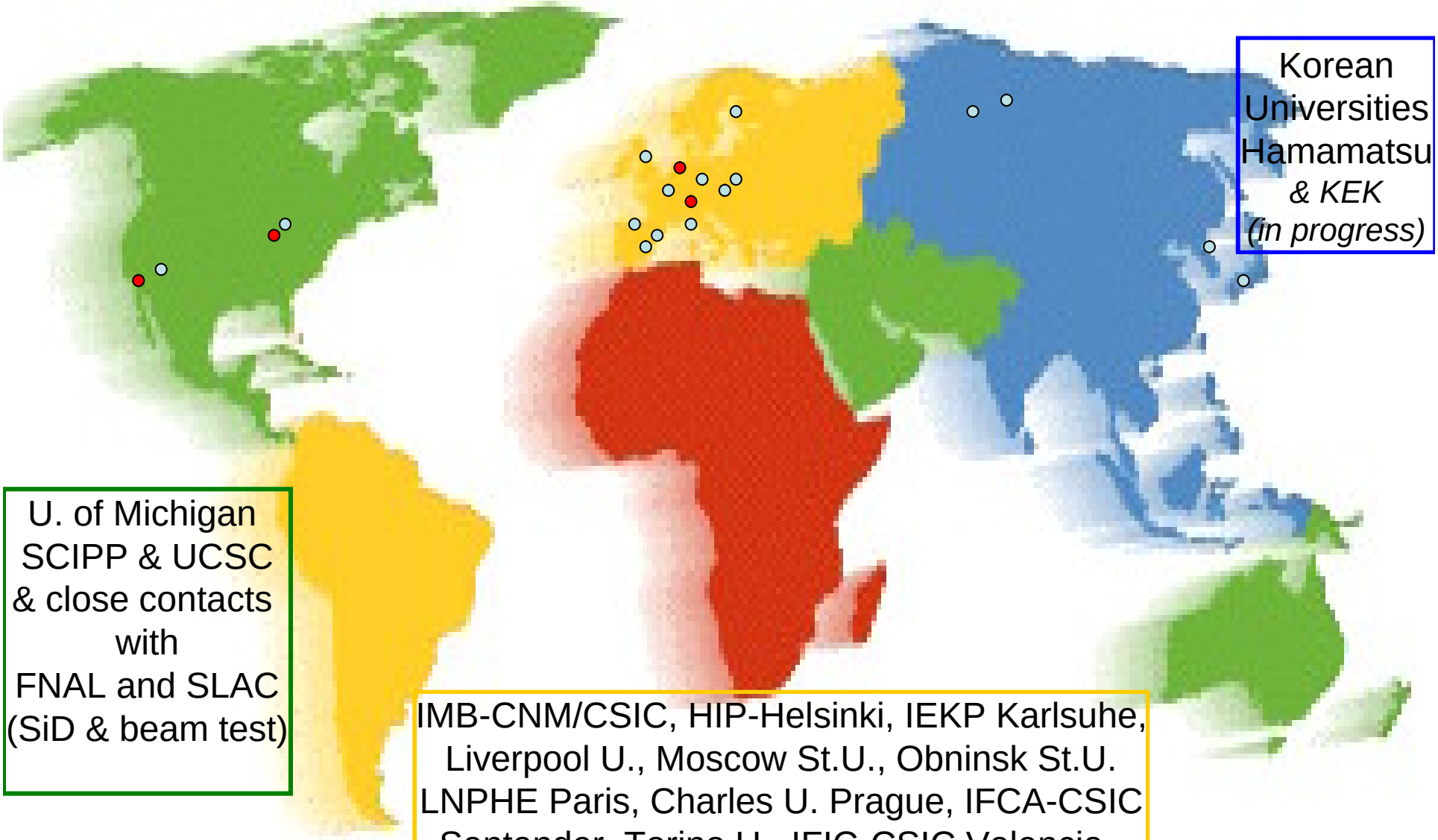
Aurore Savoy_Navarro, LPNHE, UPMC/IN2P3-CNRS

On behalf of the SiLC Collaboration

International Linear Collider Workshop

ECFA & GDE Joint Meeting, Valencia, November 6-10 2006

The SiLC Collaboration: *PRC-DESY 0503 & status report 0505*



Korean Universities Hamamatsu *& KEK (in progress)*

U. of Michigan SCIPP & UCSC & close contacts with FNAL and SLAC (SiD & beam test)

IMB-CNM/CSIC, HIP-Helsinki, IEKP Karlsuhe, Liverpool U., Moscow St.U., Obninsk St.U. LNPHE Paris, Charles U. Prague, IFCA-CSIC Santander, Torino U., IFIC-CSIC Valencia, IEHP Vienna.
& close contacts with CERN and DESY

SiLC participation to EUDET➔ SiTRA

Members

- HIP, Helsinki (Fi)
- LPNHE, Paris (Fr)
- CU, Prague (CZ)
- IFCA, Santander (Sp)

Associates

- IMB-CNM, Barcelona (Sp)
- IEKP, Karlsruhe (Ge)
- LU, Liverpool (UK)
- MSU, Moscow (Ru)
- OSU, Obninsk (Ru)
- IFIC, Valencia (Sp)

SiTRA is part of SiLC R&D project. All SiLC partners are indeed participating to the SiTRA activities (esp. beam tests)

SiLC R&D collaboration meetings

The SiLC collaboration has started to have regular meetings since the last ECFA ILC Workshop in Vienna, November'05.
proven to be quite fruitful so far.

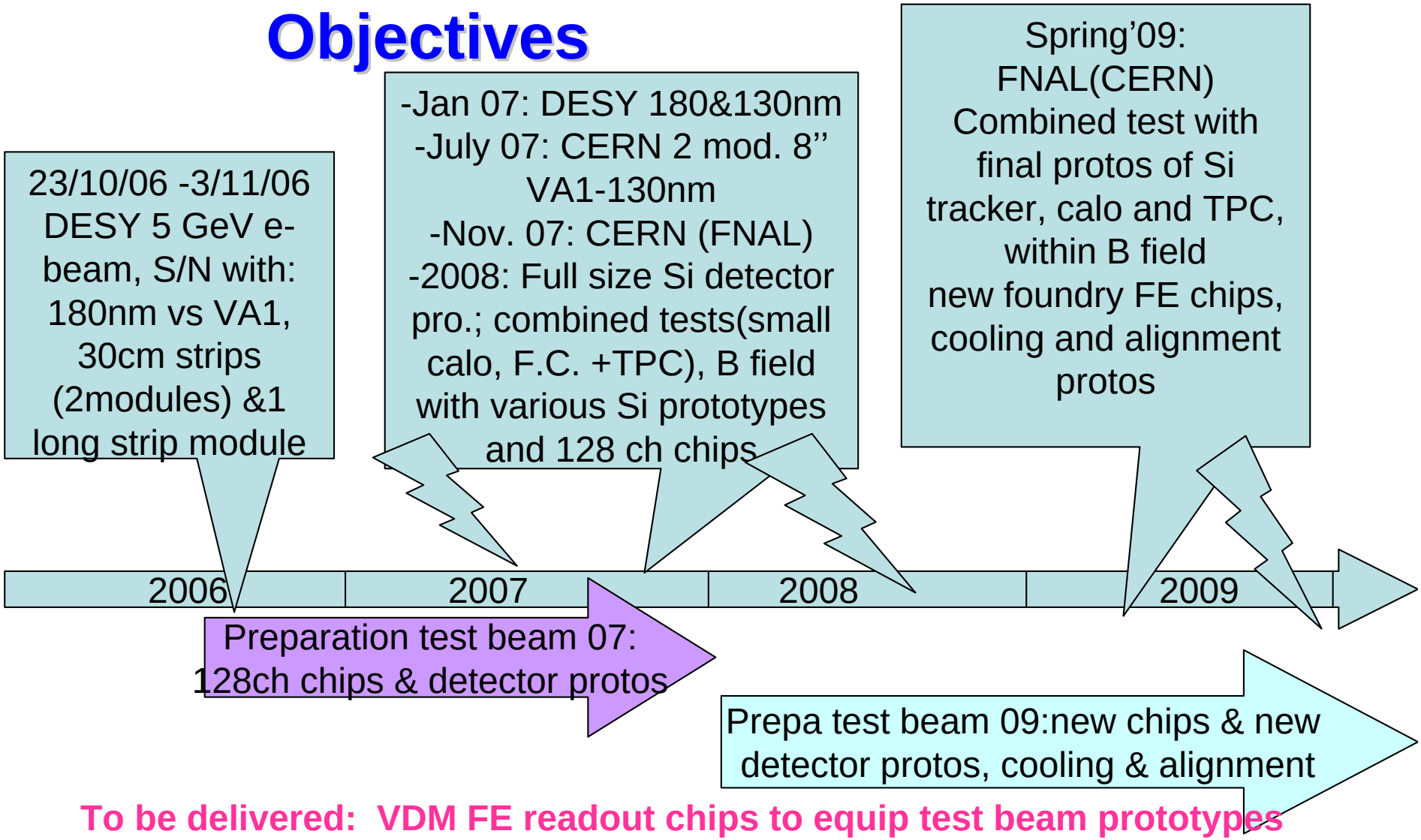
Next meeting

Barcelona, Dec 18-20 2006

Topics

- R&D on new silicon sensors
- Towards the fabrication of new modules
- R&D on the electronics front
- 2006 beam test
- Prospects for 2007
  - Preparation of new beamtests
  - Developing Alignment
  - Developing Cooling

SiLC Roadmap & Scientific Objectives



To be delivered: VDM FE readout chips to equip test beam prototypes
Large area Sllicon tracking structure prototypes
Cooling & alignment systems
Series of testbeams Si alone or combined (see Roadmap)

A. Savoy-Navarro, SiLC, Valencia, Nov'06

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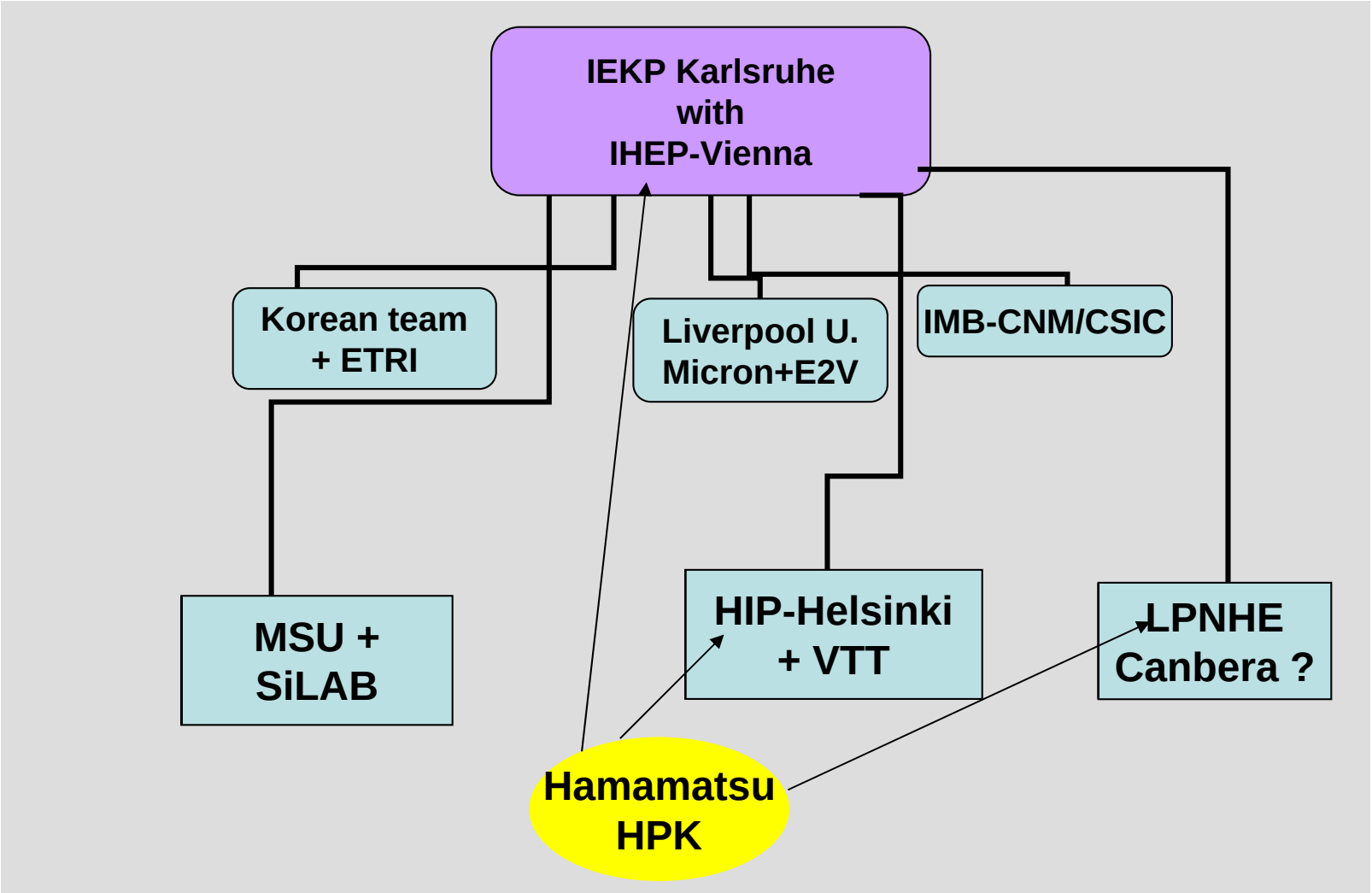
Immediate goals (prototypes in 07):

- Larger single-sided wafer **(8'')** microstrips
- Larger double-sided wafer **(6'')** microstrips
- Eventually thinned (1/2 or 3)
- Starting to develop new tech prototypes:

  -> see VTT

  -> see novel wiring

R&D on Si sensors: organisation



A. Savoy-Navarro, SiLC, Valencia, Nov'06

Helsinki-Paris proposal for new sensors

(N. Van Remortel (HIP-Helsinki) and VTT)

Helsinki (sensor devel.) & Paris (readout chip & electronics) want to combine their expertise & technology to produce and test new sensor design in next year's EUDET/SilC test beam

Planar 3D concept by Helsinki

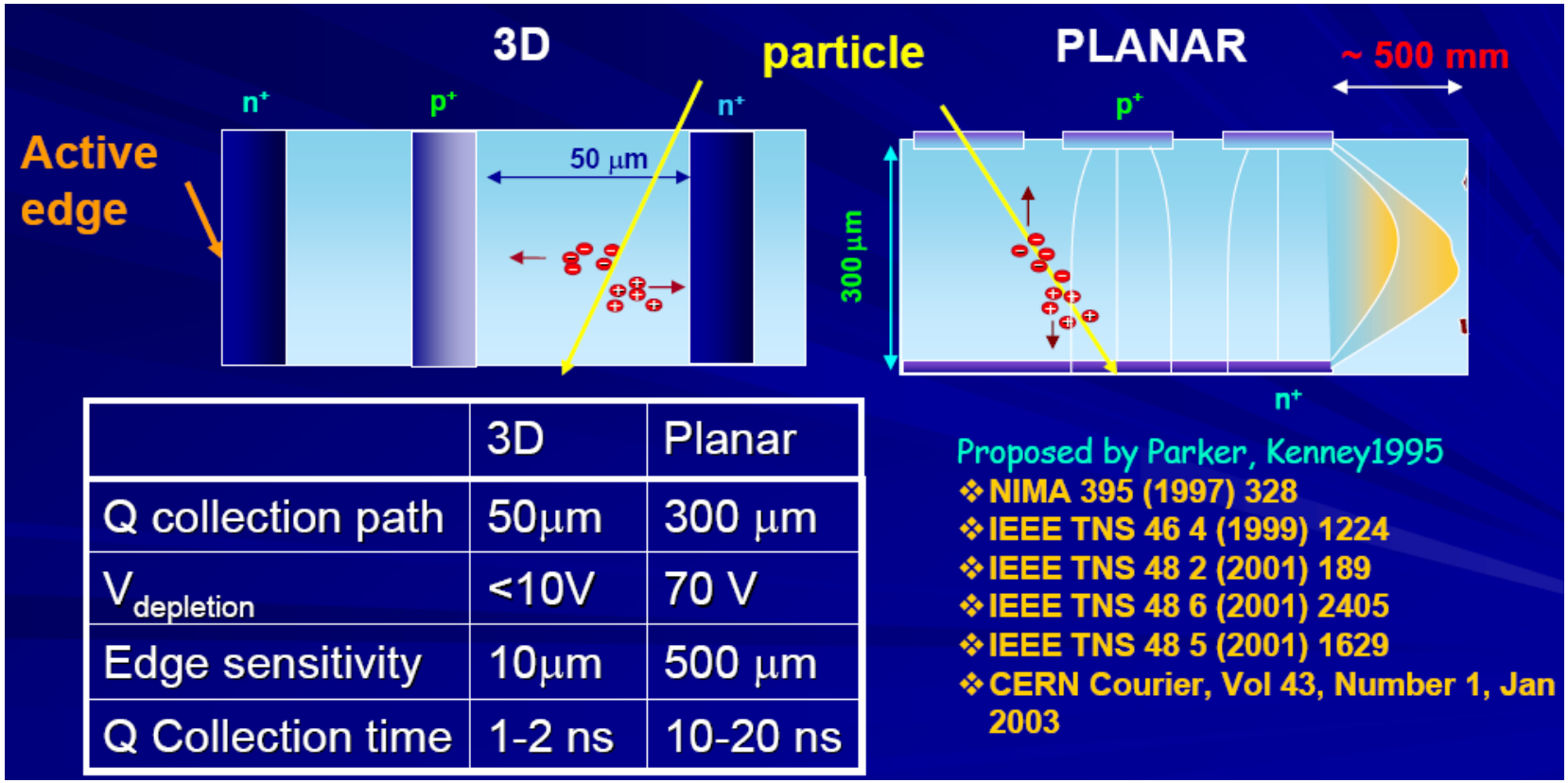
3D structures within a silicon detector offer a large amount of advantages:

- very radiation hard
- fast response
- small operating voltages
- sensitive up to the edge

Some of these are very attractive to ILC designs:

- when bonding several sensors you reduce the insensitive area between sensors.
- sensors can be made very thin, since charge collection happens along the length of the sensor, rather than the vertical thickness of the sensor.

Benefits of 3D technology



	3D	Planar
Q collection path	50μm	300 μm
$V_{depletion}$	<10V	70 V
Edge sensitivity	10μm	500 μm
Q Collection time	1-2 ns	10-20 ns

Proposed by Parker, Kenney1995

- NIMA 395 (1997) 328
- IEEE TNS 46 4 (1999) 1224
- IEEE TNS 48 2 (2001) 189
- IEEE TNS 48 6 (2001) 2405
- IEEE TNS 48 5 (2001) 1629
- CERN Courier, Vol 43, Number 1, Jan 2003

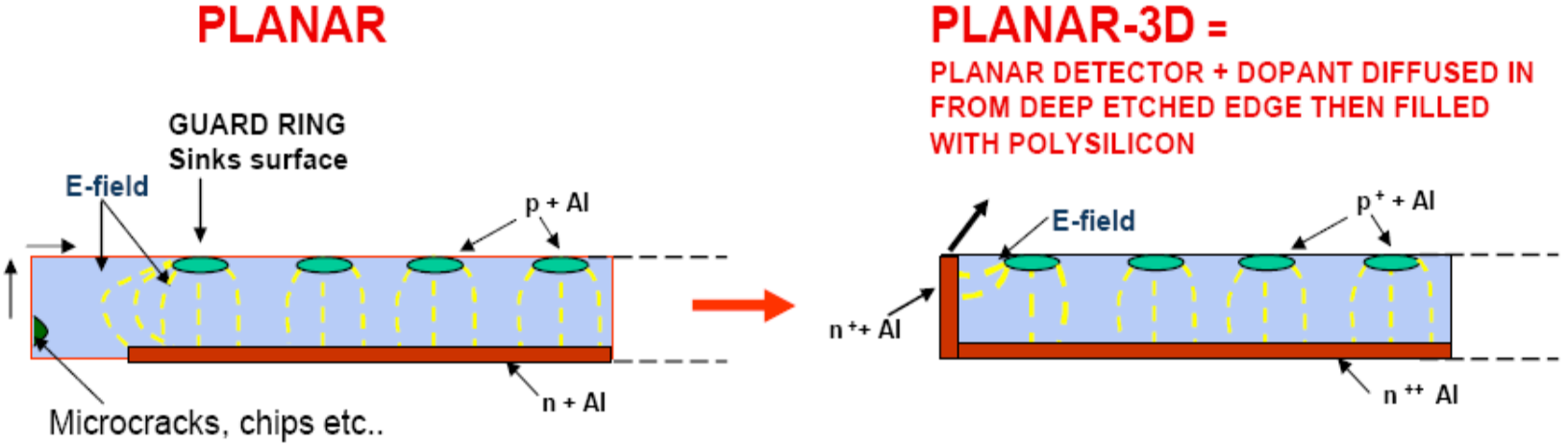
BUT:

- Full 3D sensors are not always easy to produce and handle:
  - **Uniform filling of holes with polysilicon is problematic**
  - **Sensors can become brittle and difficult to dice (cut)**

Prepared by N. van Remortel (HIP-Helsinki) and VTT

Planar-3D sensors

- Planar-3D sensors can be a new successful solution satisfying most of the good qualities from true 3D designs
  - In planar-3D detectors the n-doped active edge is done by using ICP-etching (trench that surrounds the sensor) and poly-silicon filling.
  - Active edge avoid inhomogeneous electric fields and surface leakage currents and permit large active/inactive area ratio (tiled sensors).



- Total cost chaired between VTT (50%), Helsinki+Paris(50%)
- Processing can go fast (masks etc. are available), major time factor depends on substrate material
- Sensors expected by spring 2007, if material ordered now.

Pepared by N. van Remortel (HIP-Helsinki) and VTT

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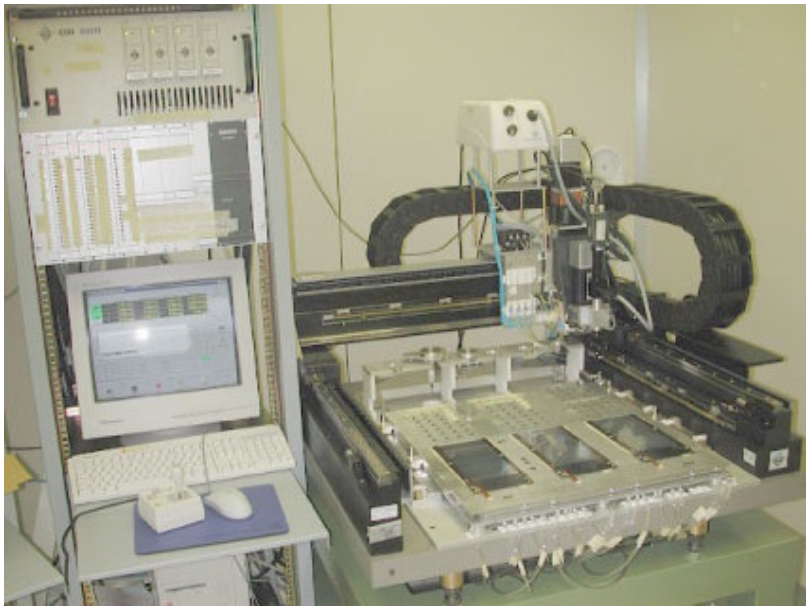
The elementary module: tile of the overall architecture

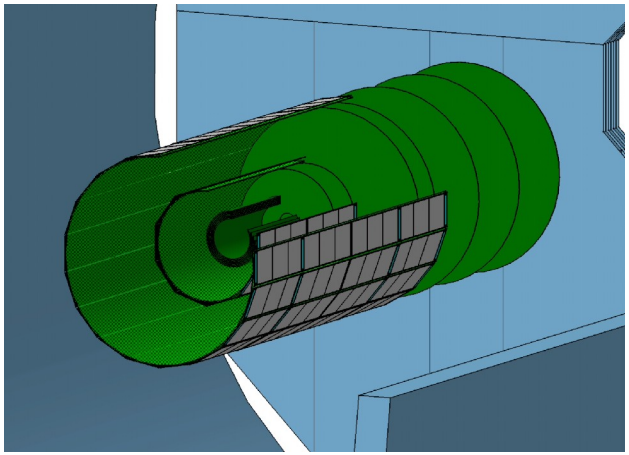
Based on present experience (LHC) must be light, precise, robust, easy to build & assemble:

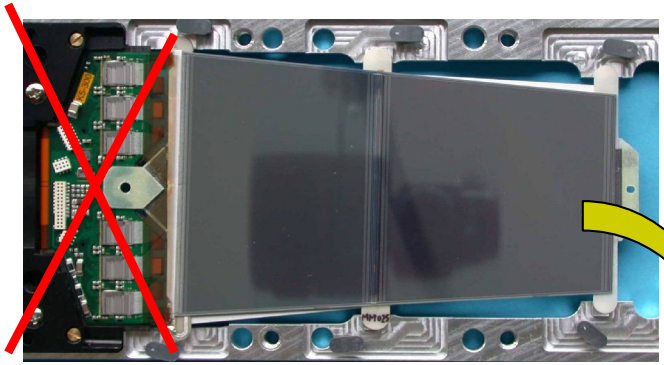


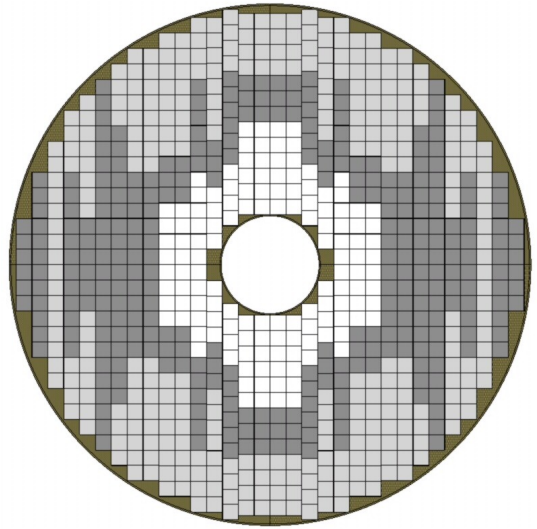
Robotic assembly (CMS)

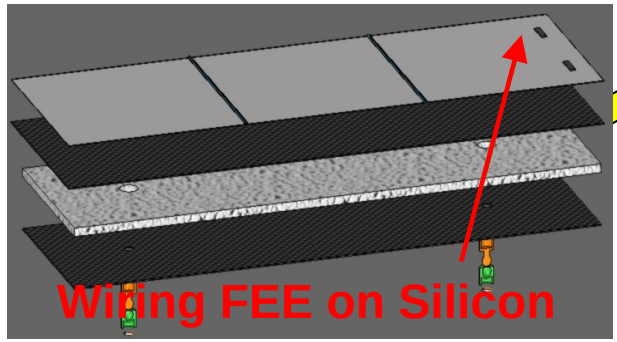
- **New sensors (next generation)**
- **Support: new material &design**
- **VDSM FE electronics & wiring**
- **Precise positioning on the module & the support structure**
- **Easy to build (robotisation ?)**
- **Industry transfer: big number**
- **Favouring a ‘’universal tile’’ (instead of different shapes)**

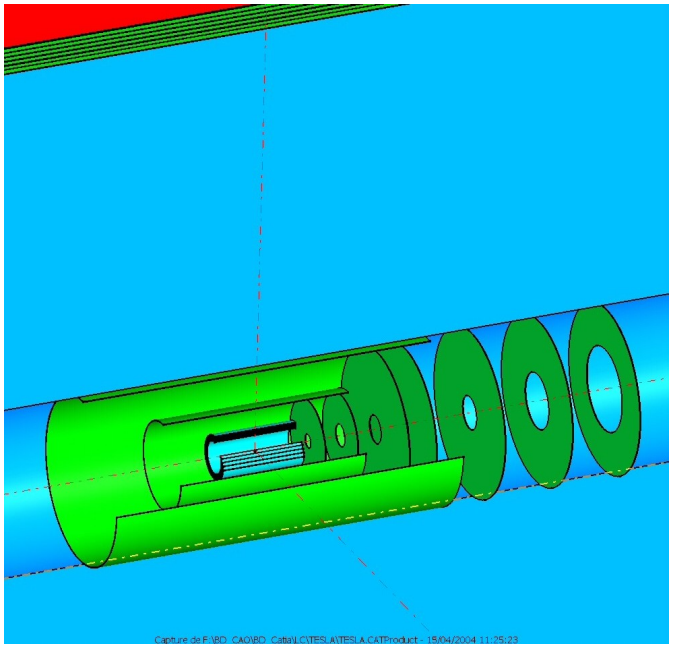
Towards the new elementary module concept



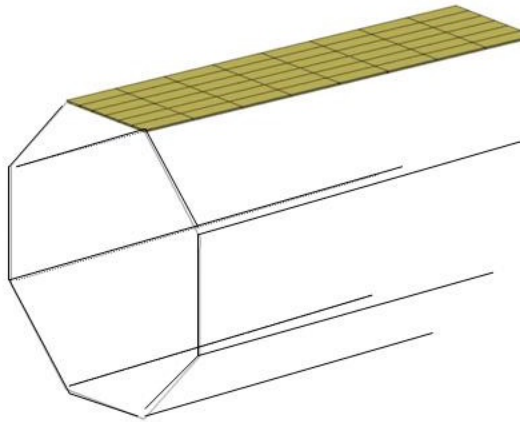


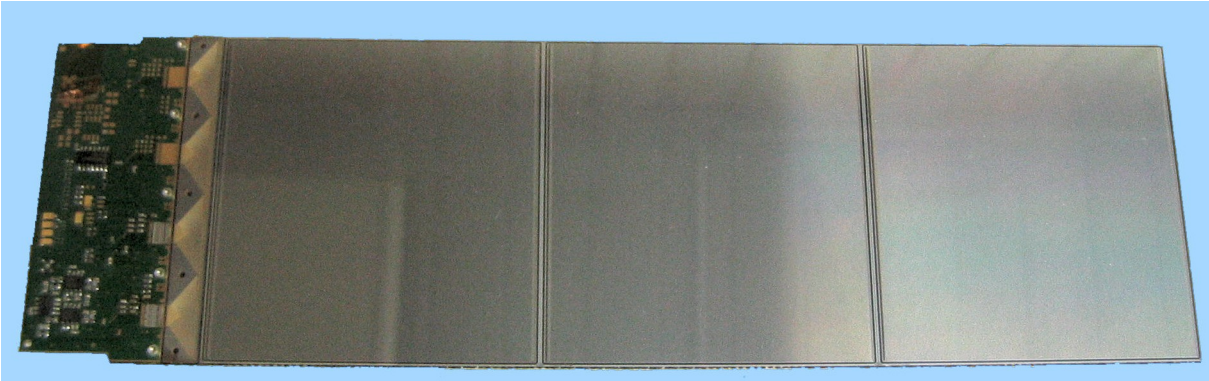


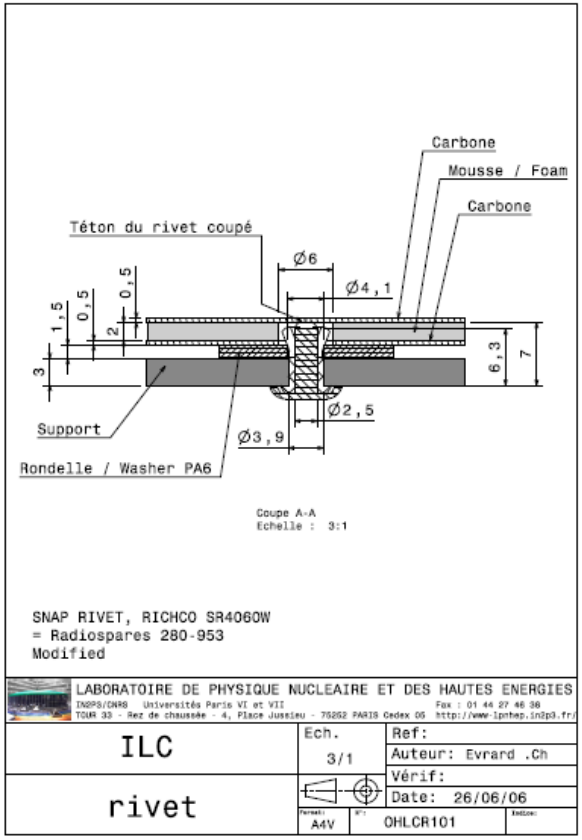


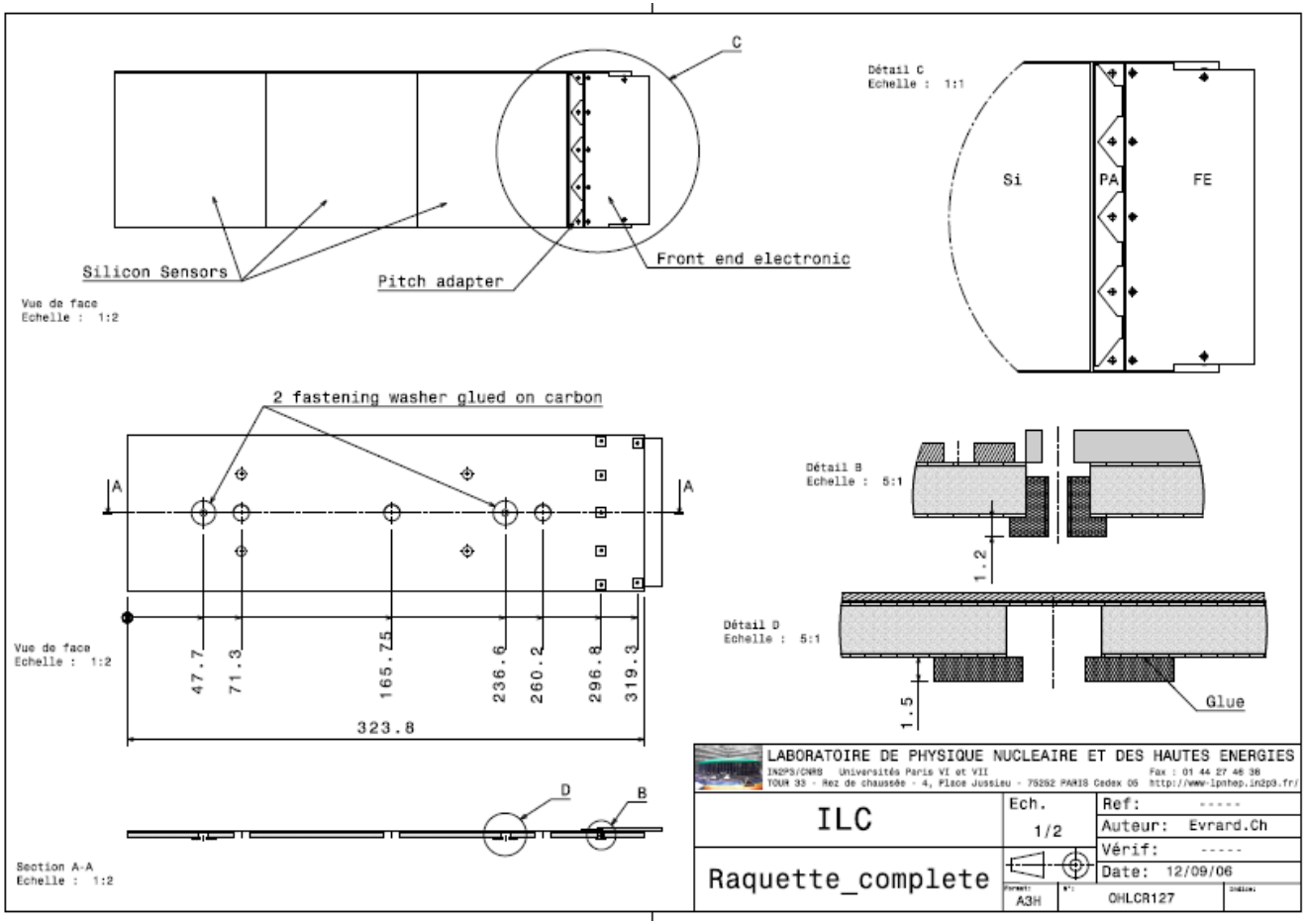


Module is made of 1,2 or 3 sensors depending the location but sensor should be of unique size if possible









LPNHE: construction of module-3CMS:
First attempts to gain expertise, thanks to . the collaboration with A. Honma et col. CERN

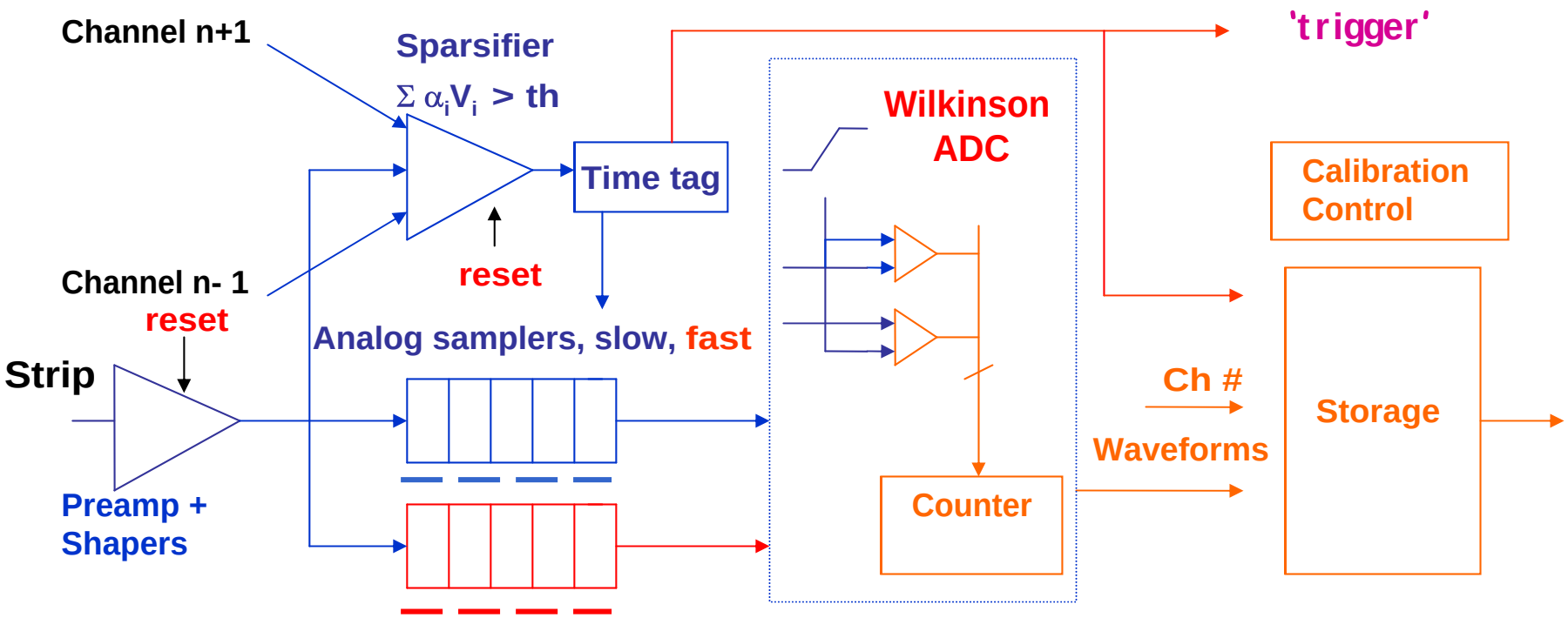
New sensors, new modules

- **New sensors**: organization with IEKP Karlsruhe as coordinator helped by IEHP Vienna.

  Need closer contacts with Industry (in progress)

  Automated fabrication line, starting to be experienced with A. Honma et al. at CERN, on very first new modules built at LPNHE.
- **New modules**: under R&D very dependent of the technology used for wiring the electronics on detector. Collaboration with industry (sensor fabs and chip foundry) is starting with various teams of SiLC.

Foreseen Front-end architecture



Charge 1- 40 MIP, Time resolution: BC tagging 150- 300ns, fine: ~ 1ns

Technologies: Deep Sub-Micron CMOS 180-130nm
Future: SiGe &/or deeper DSM

Topics

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- **R&D on the electronics front**
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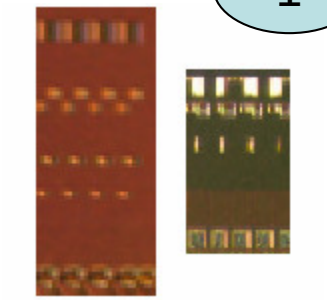
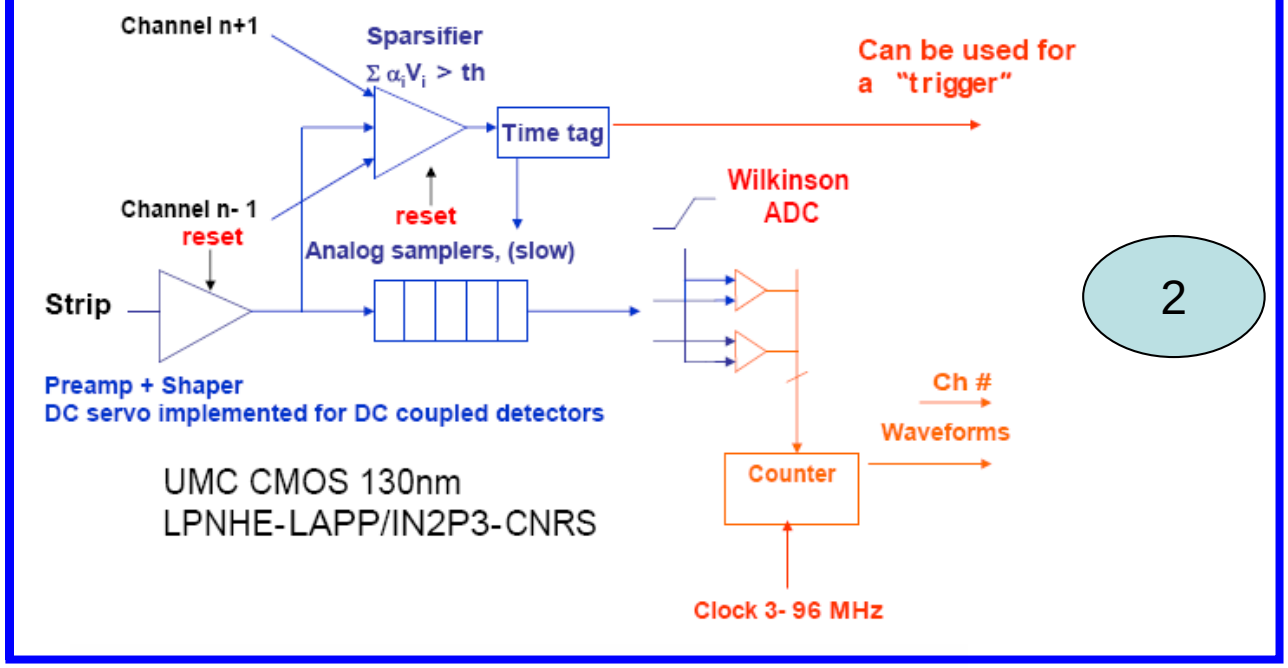
FE readout Electronics main achievements in 2006

Going from:
180nm to 130nm

1





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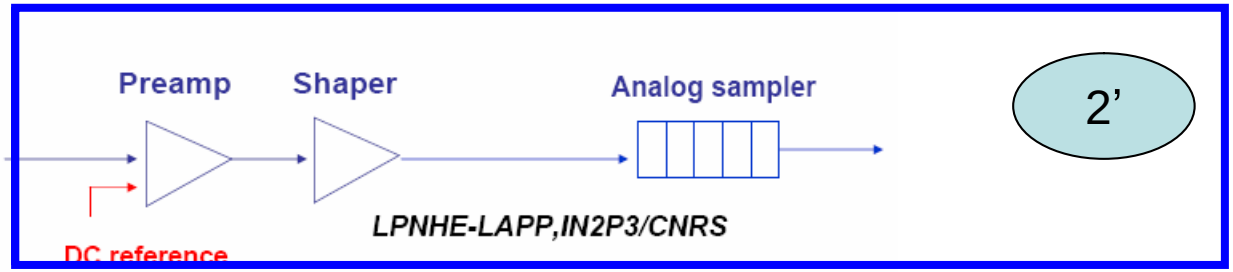


2'

Starting now:

3

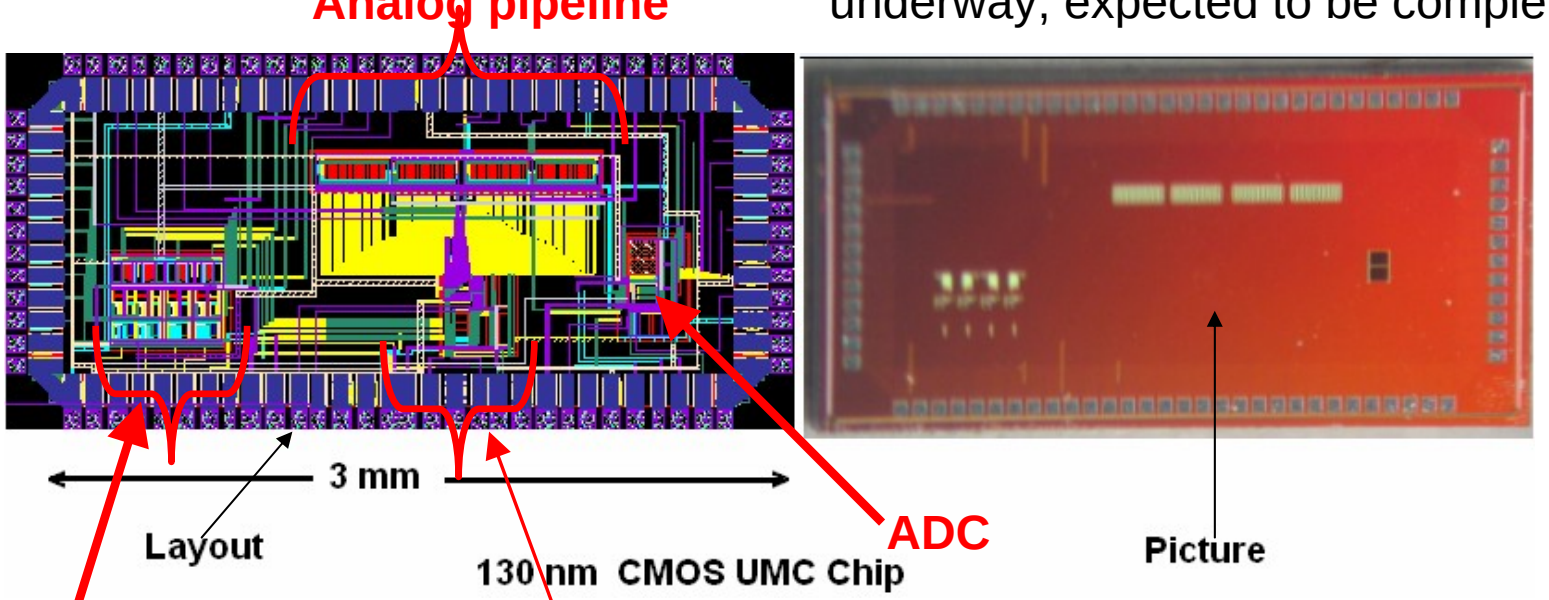
Test of the first chips UMC-180nm and later UMC-130nm connected to a Si module at the Lab test bench and then at the DESY beam test; ***from chip to demonstrator***

Development of the VDMS FE and r.o. chip to equip EUDET beam tests

❖**First prototype in 130nm UMC techno and with full FE+ RO chain:**

LPNHE+LAPP+IMEC

submitted April 19 2006 received August 15 2006, the tests are underway; expected to be completed end 06.



Tests of first 130nm prototypes:

An intensive test work on the analog part is undertaken at LPNHE. First results are expected soon on analog part (noise?). Followed by tests on digital part.

VDMS FE+r.o. chip to equip EUDET t.b. (cont'd)

- 2nd prototype in 130nm UMC: F.E. only (improved) + DC servo+calib (LPNHE-LAPP-IMEC), sent to foundry October 4th.

- 3rd prototype in 130nm IBM, analog part only: CERN+LPNHE Meeting/Decision on the technology for 1st production (128 ch)

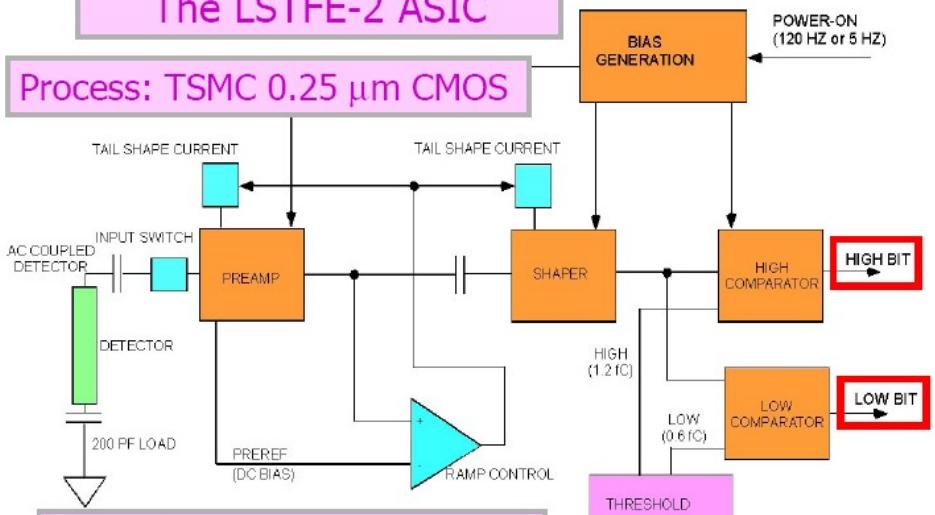
- Full Prototype with 32/64 channels, before production of 128 channels. To be sent next (or go right away with 128 ch?)

- Packaging, detector wiring and r.o. cards (HIP+VTT, IMB-CNM Barcelona + LPNHE + Industrial firms): starting…
  New groups interested in electronics (ex: IFCA, IMB,CERN, IHEP…)

Actions are conducted in parallel

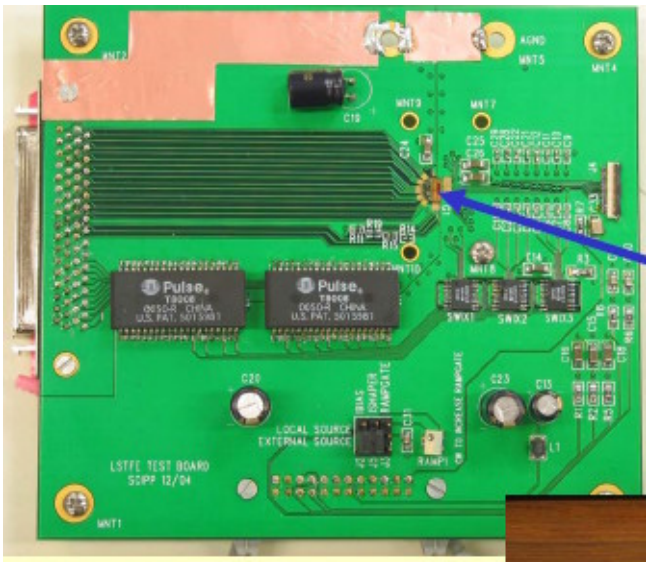
The LSTFE-2 ASIC

Process: TSMC 0.25 μm CMOS



1 μs shaping time; analog readout it Time-Over-Threshold with 400 nsec clock

F.E. Electronics developed by SCIPP&UCSC (Bruce Schumm et al)



Noise vs. Capacitance (at τ_{shape} = 1.2 μs)

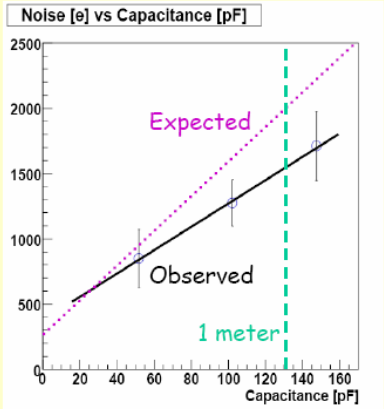
Measured dependence is roughly (noise in equivalent electrons)

$$\sigma_{noise} = 375 + 8.9*C$$

with C in pF.

Experience at 0.5 μm had suggested that model noise parameters needed to be boosted by 20% or so; these results suggest 0.25 μm model parameters are accurate

➔ Noise performance somewhat better than anticipated.



B. Schumm Talk at ALCPG 2006

LSTFE SUMMARY

The LSTFE readout system is:

- Universally applicable (long strips, short strips, central, forward, SiD, LDC, GLD)
- Specifically and carfully optimized for ILC tracking
- Relative simple (reliability, yield)
- In a relatively advanced stage of development
  - Amplifier/comparator looks functional
  - Headway being made on fast power cycling
  - Digital architecture soon available on FPGA
- Hoping to join SiLC testbeam run in late 2007

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- Towards the fabrication of new modules
- R&D on the electronics forefront
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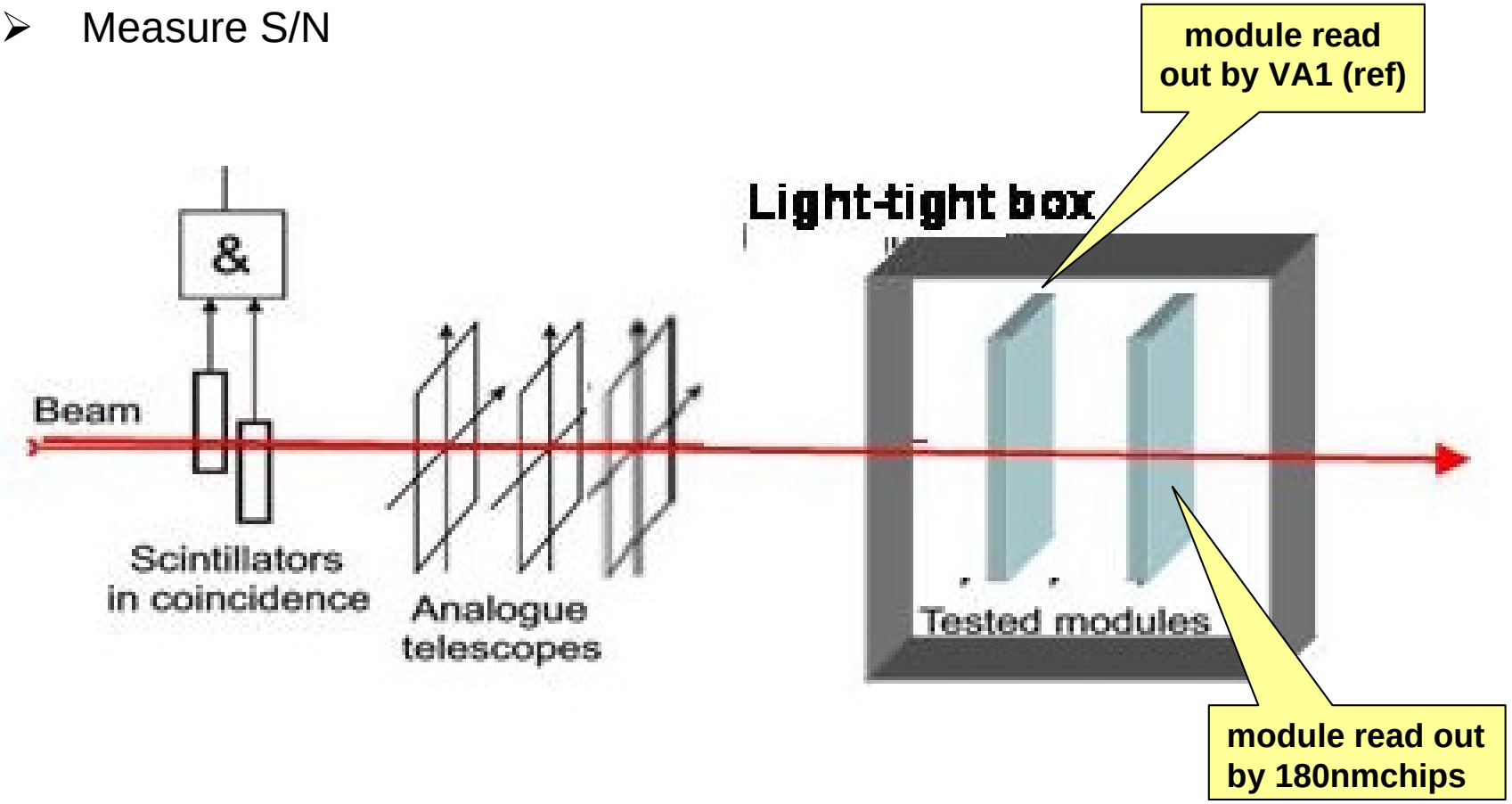
EUDET Test beams @DESY in 2006

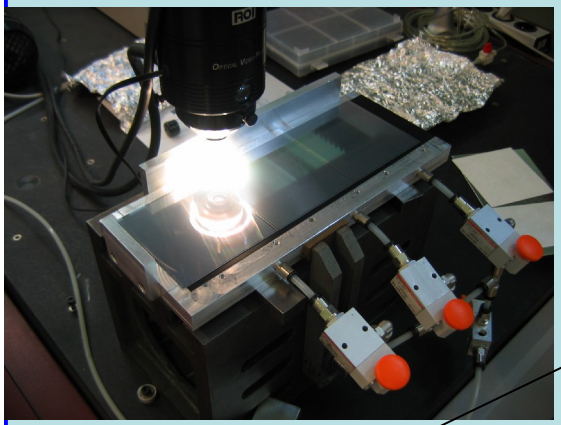
First tests at the DESY e- test beam, no magnetic field, performed from October 23 to November 3; this will be pursued end January 07, goals:

- Test the complete new test set-up (modules, read out electronics, DAQ)
- Compare new first FEE prototypes (180nm UMC, eventually 130nmUMC) wrt to reference, i.e.: VA1 chips
- Measure S/N



Detector prototypes

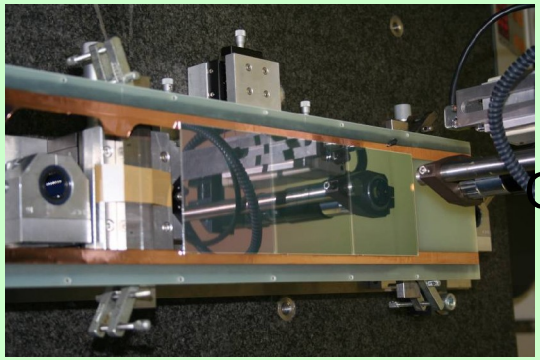
CERN(A.Honma), IEKP-Karlsruhe, LPNHE-Paris, IEHP-Vienna, Hamamatsu



Assembly

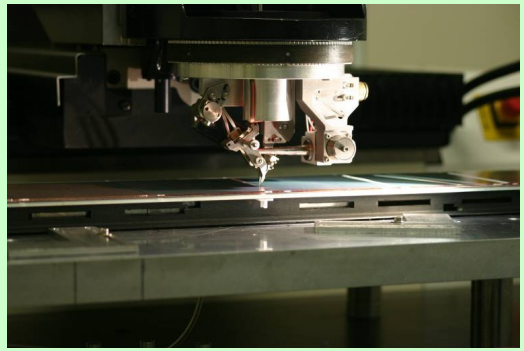
3 CMS sensors 28 cm strip long
Read out:
VA1+180UMC r.o
and all VA1 r.o.

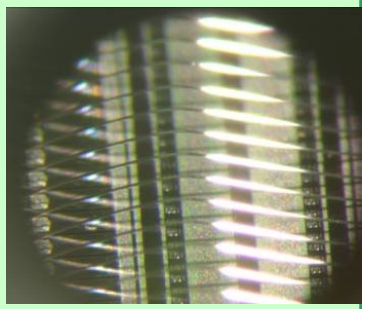
2 modules fabricated in Paris,
bonding CERN on automated CMS system
(Collab CERN-LPNHE)



Assembly:
Module = 10
GLAST sensors
90 cm strip long

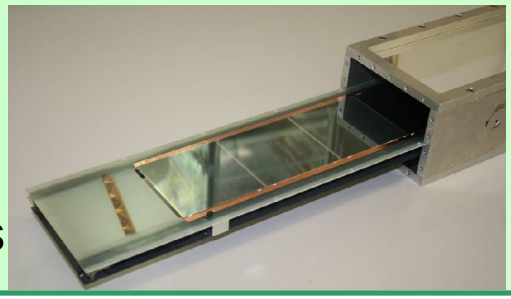
Bonding





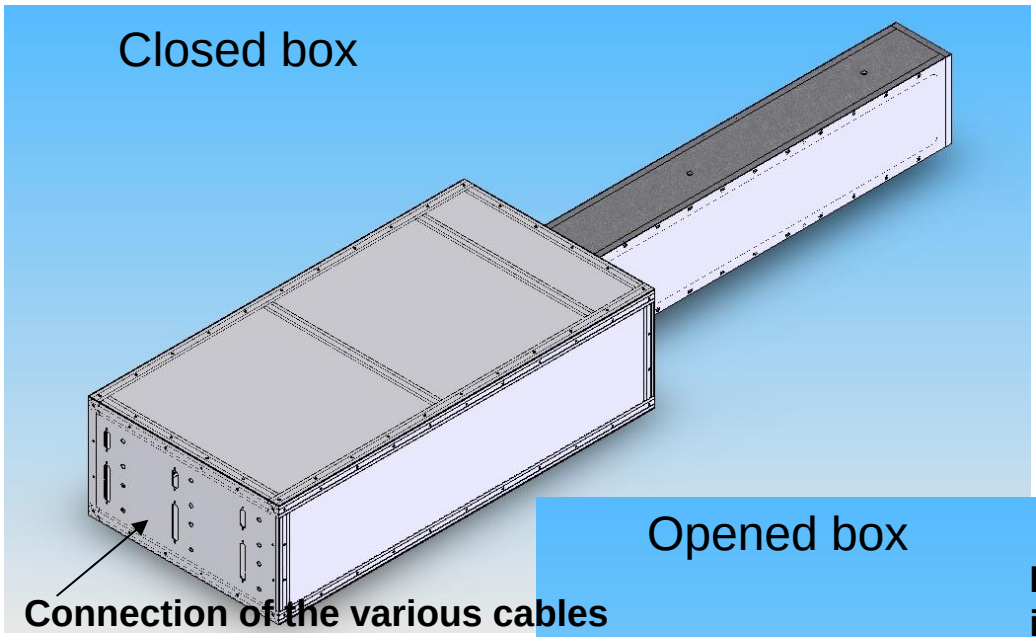
The full construction done at IEKP

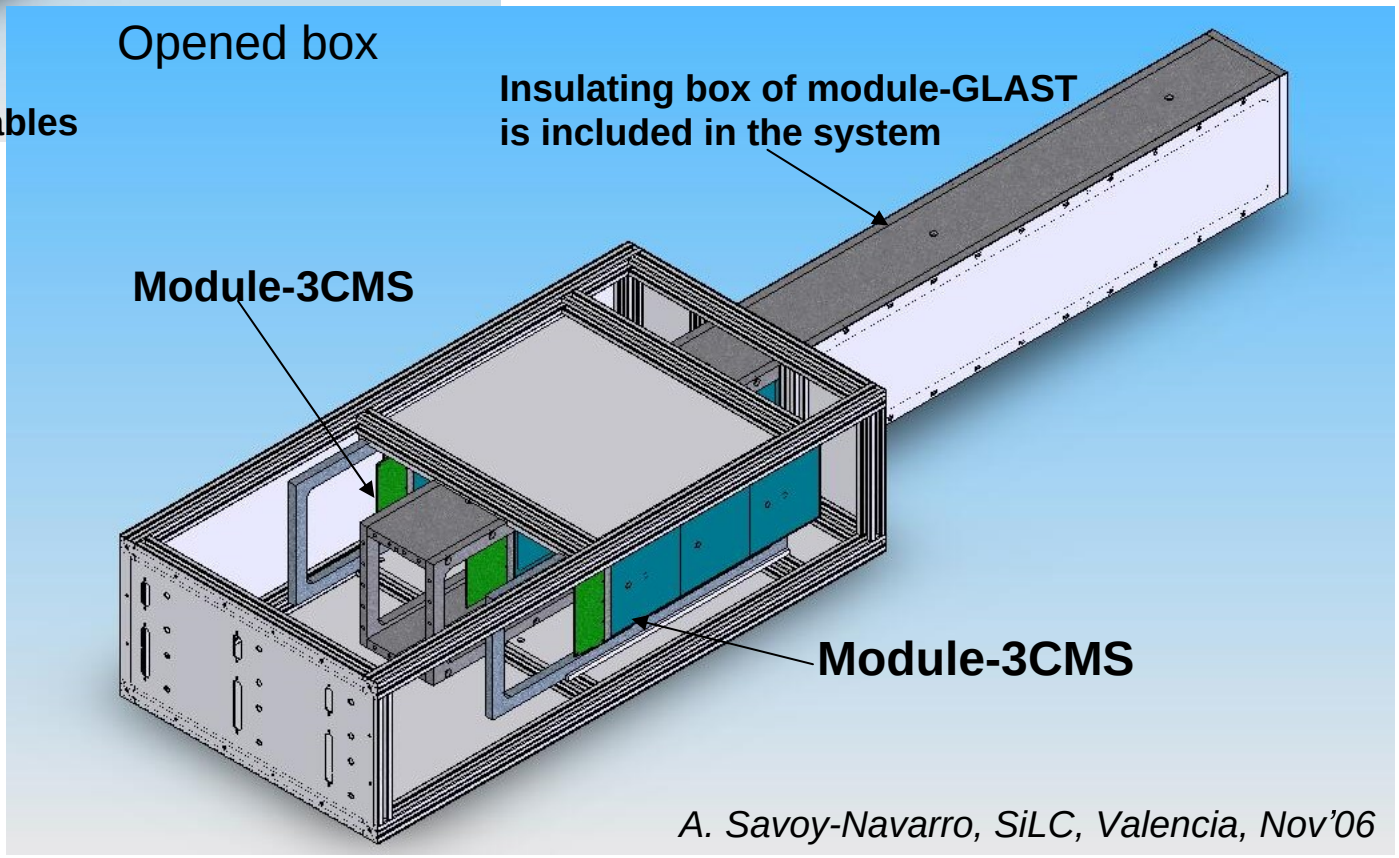
R.O.
Pitch adapter +
VA1 + 180UMC
provided by Paris



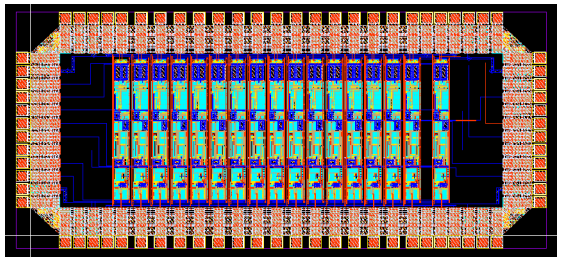
Insulating box for the 2 modules-3CMS and module-10GLAST

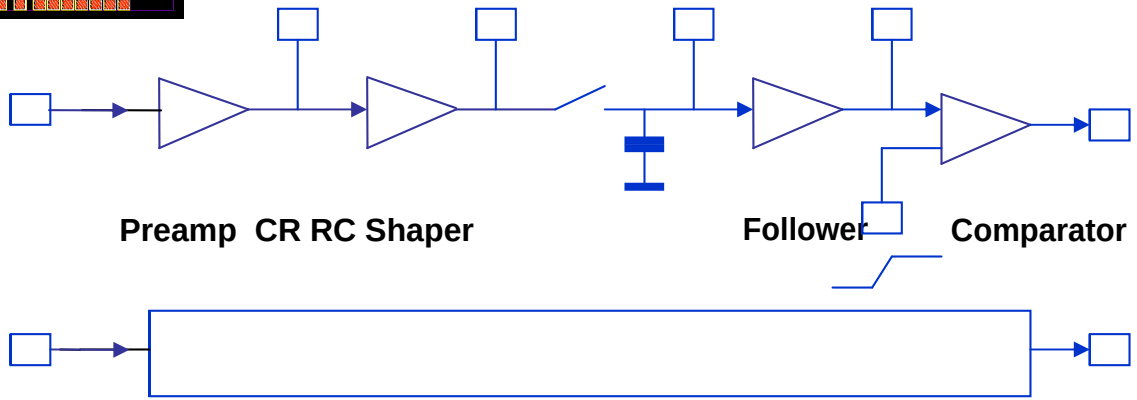
P. Modesto (IFIC-Valencia)

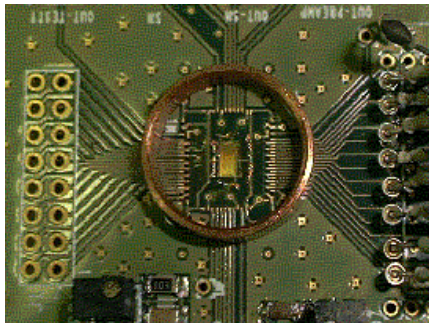




Front-end test chip in CMOS 180nm



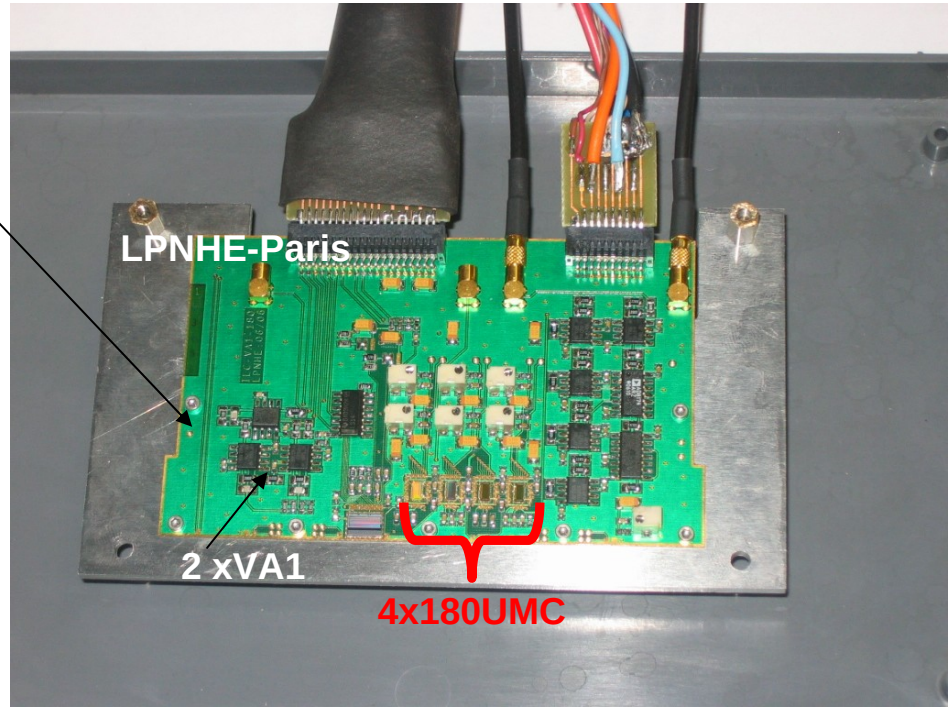




- Low noise amplification + pulse shaping
- Sample & hold
- Comparator

Readout Electronics: LPNHE Paris

2 VA1 + 4x 180UMC channels: hybrid R.O. card under test

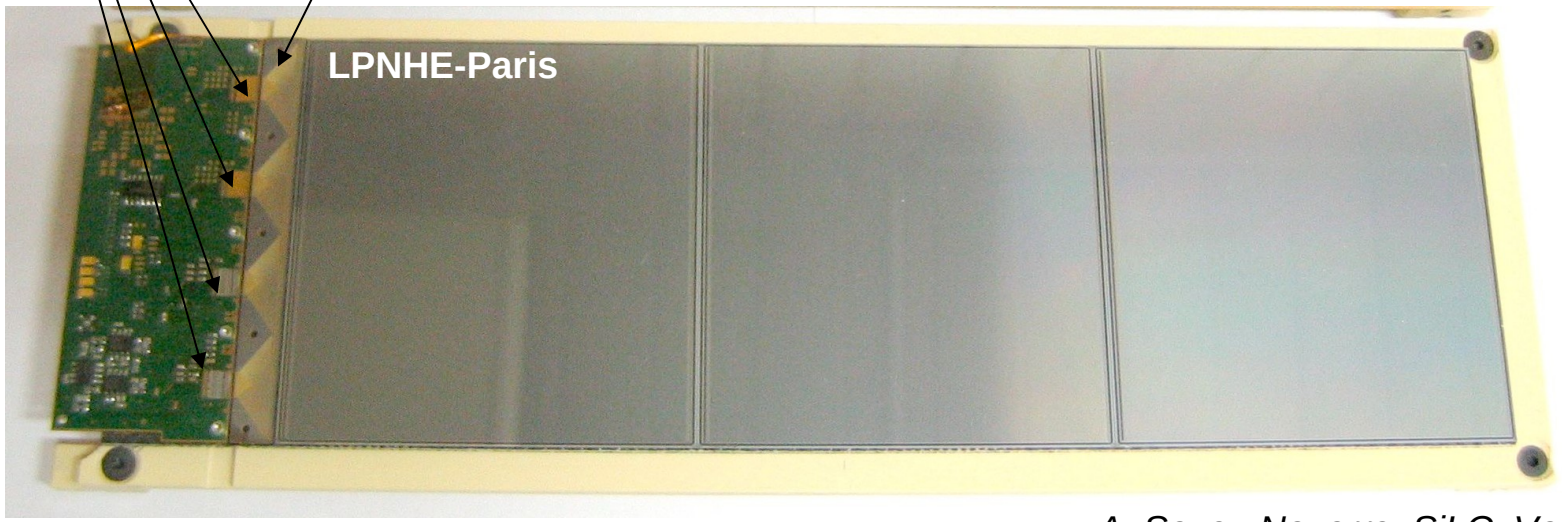


4 VA1 r.o card

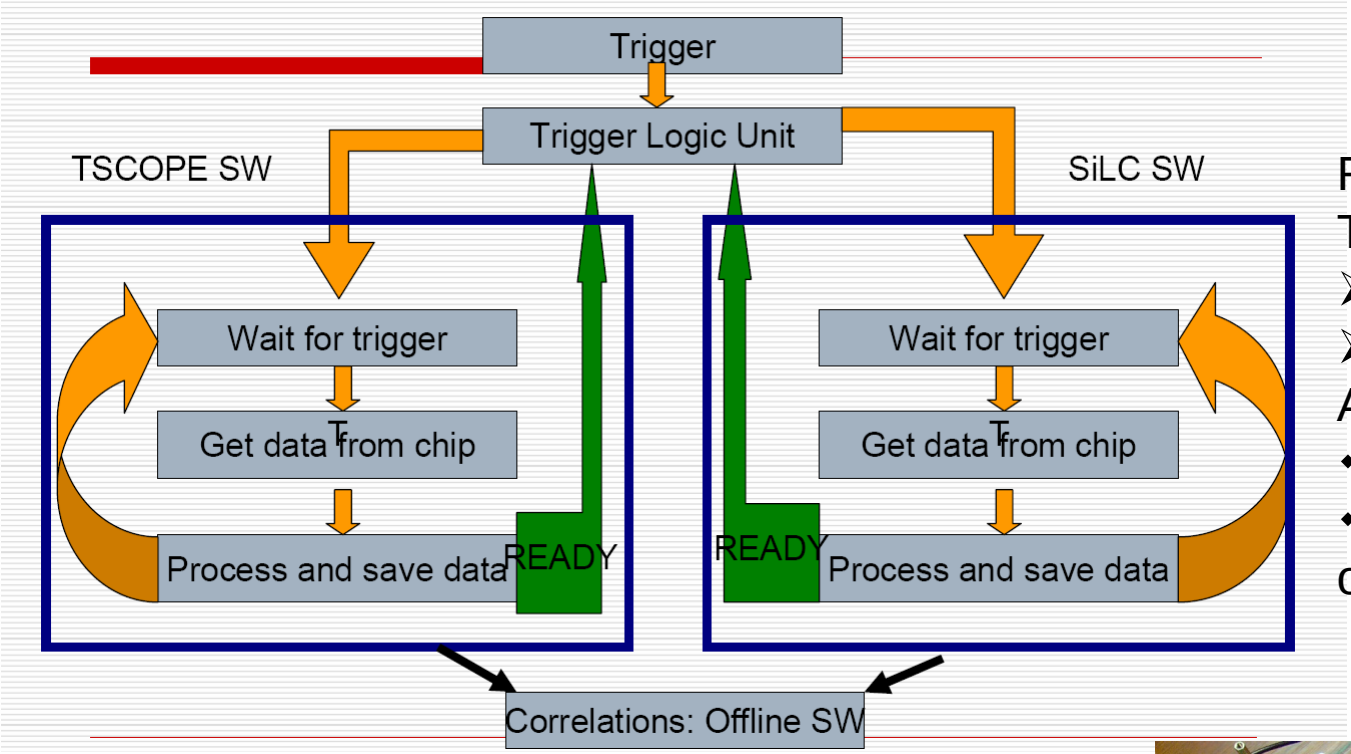
- VA1 r.o. card ready
- 2 hybrid r.o. cards: VA1+180UMC ready

Both being tested at Paris Lab test bench

Pitch adapter



DAQ: hardware & software

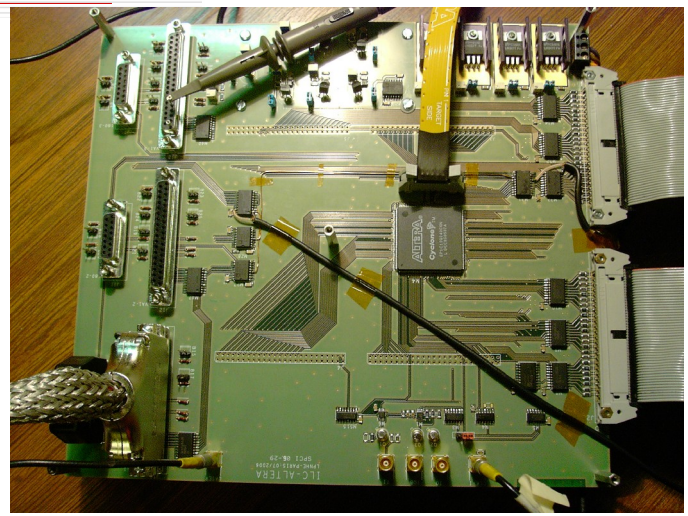


LPNHE-Paris:
Rebuilt its DAQ test bench
To be used both for
- Tests @ Lab t.b. before
- Tests @DESY t.b.

Adapted to
- new R.O. electronics
- and to be linked to DAQ

of the beam telescopes.

DESY and CU-Prague:
Use of the existing hardware and software developed by DESY for the beam telescopes implementing a very basic trigger logic for connecting the two DAQ systems.

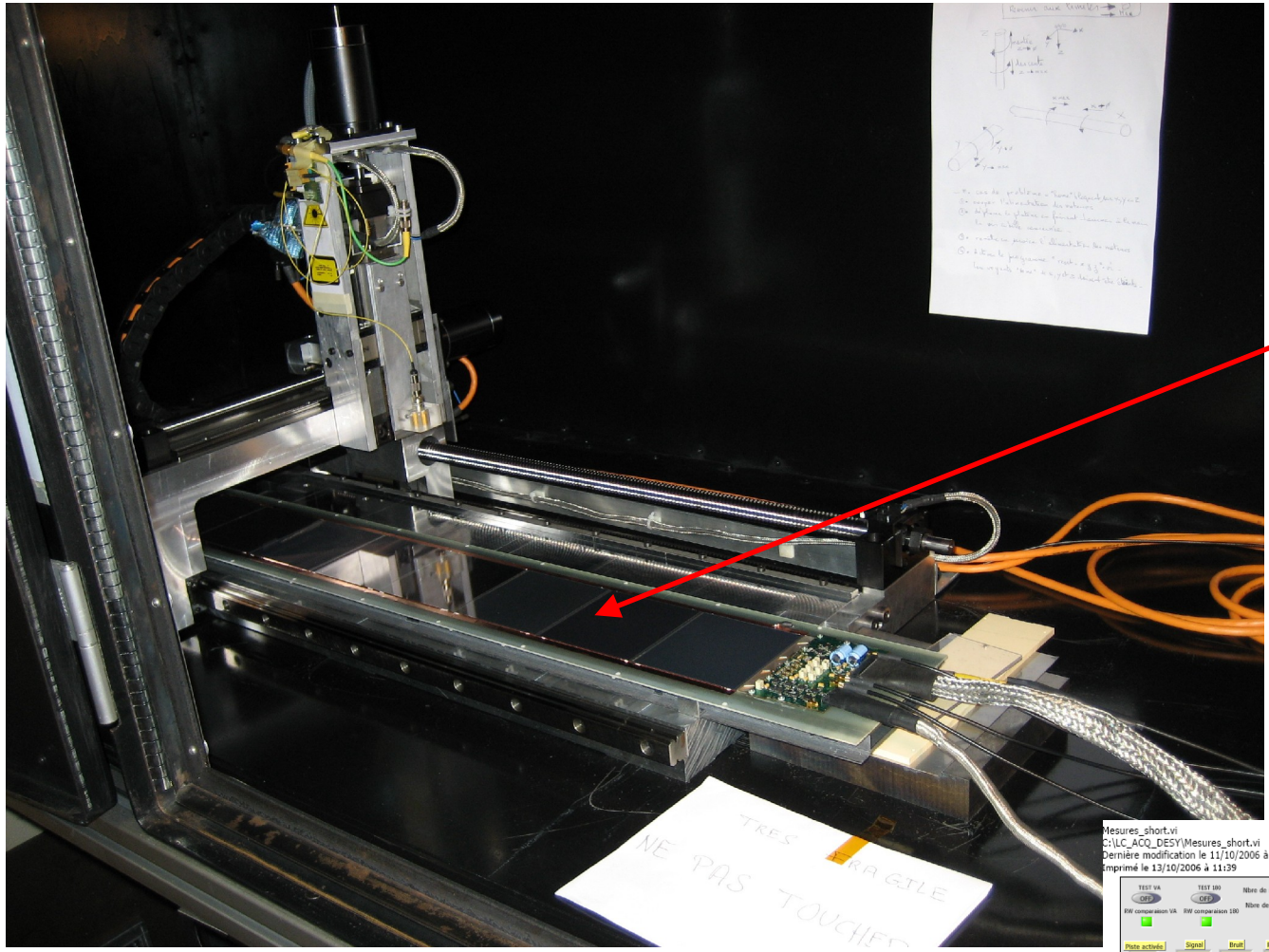


Tests at the Lab Test bench before DESY

- **Complete upgrade of the Paris Lab test bench**
- **Characterization of the new readout chips (VA1 and 180UMC)**
- **Characterization of the new Si modules:**
  - **→ 2 x 3CMSmodule**
  - **→ One long strip module**
- **Test of the functioning of the new DAQ hardware**
  - **→ New command card**
  - **→ New Altera card**
  - **→ Effect of 15 m long cable between Altera & detector R.O.**
- **Test 2 DAQ's running in parallel (beam telescope and Si detector R.O.)**
- **Test analysis packages with Lab test bench runs**

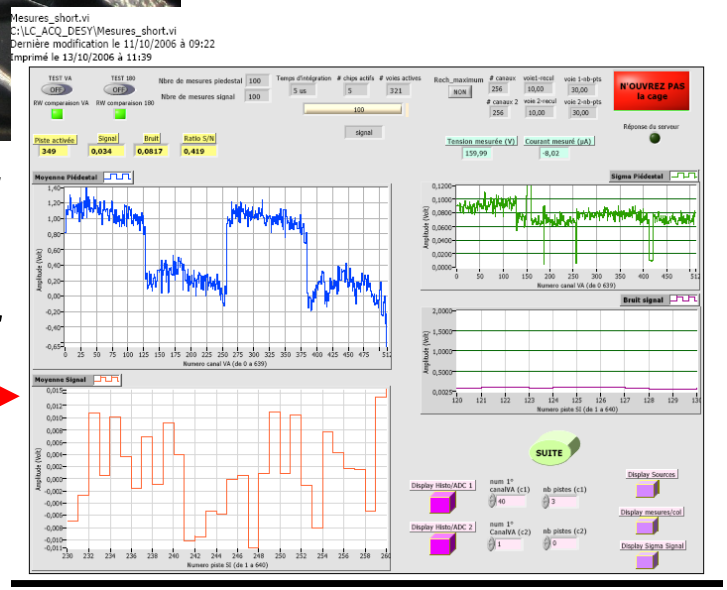
All these tests were performed at the Paris Lab test bench since end of September till October 20.

Tests are going to be pursued at the Lab test bench after the first round at the DESY test beam for further investigations and completion of the achieved measurements.



GLAST module sitting on the Lab test bench

Modules and readout electronics were tested on Lab test bench in Paris, before going to DESY., as for example, the GLAST module or the CMS-4VA1 module



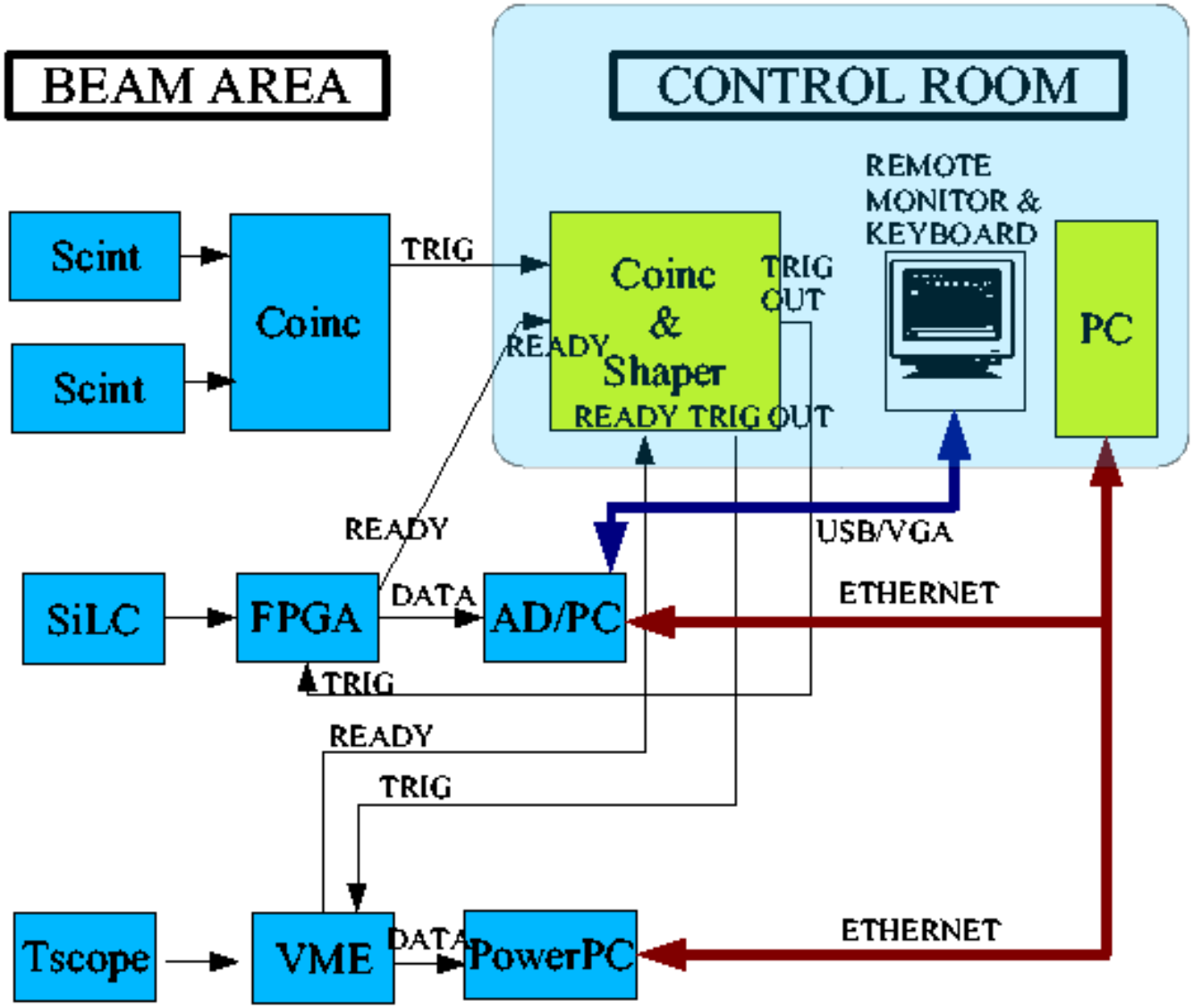
Preparation for the DESY test beam

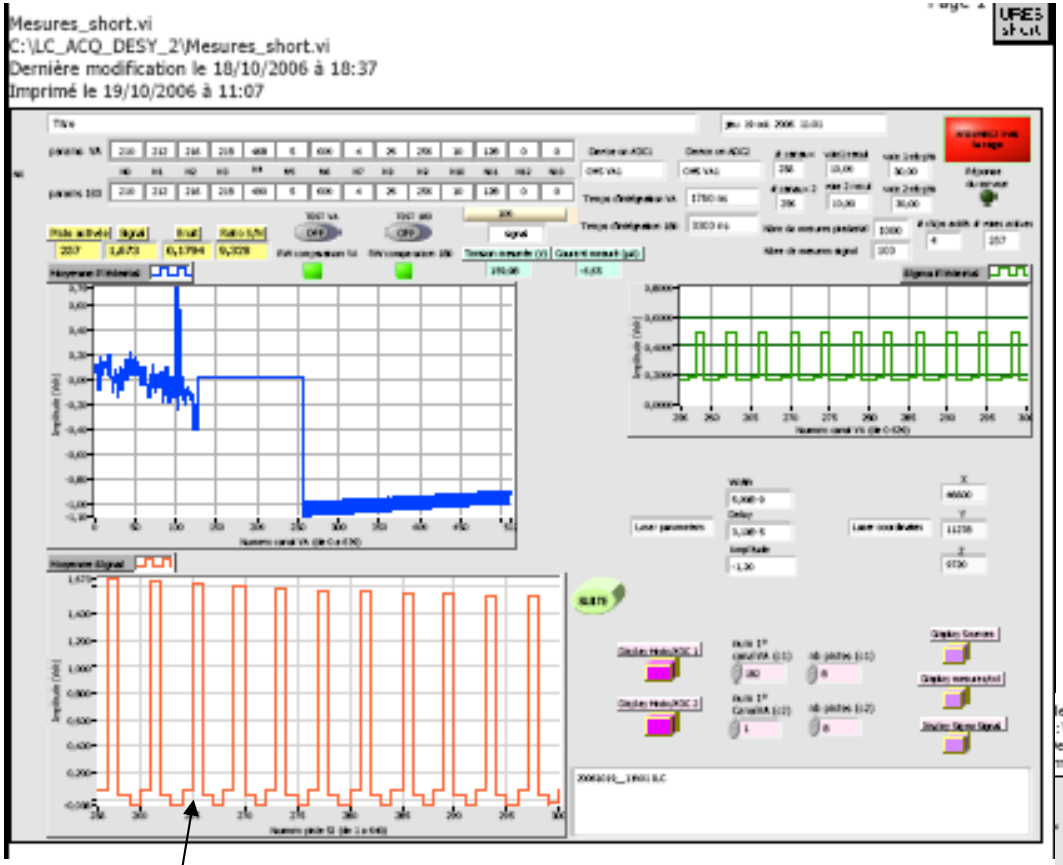
October 23 to Nov 5, 2006

Sharing of tasks

- Construction of the detector prototypes: **CERN, IEKP-Karlsruhe, LPNHE-Paris &** IHEP Vienna, Hamamatsu providing the sensors)
- Mechanics: DESY,LPNHE Paris, **IFIC Valencia**
- FE and readout electronics: **LPNHE-Paris**
- DAQ hardware: **DESY for beam telescopes, LPNHE-Paris for SiLC**
- DAQ software: **DESY, LPNHE-Paris, CU Prague**
- Test in test bench prior to go to test beam: **LPNHE-Paris,** IEKP Karlsruhe, CU Prague,
- Beam Telescopes and Beam infrastructures: DESY, OSU Obninsk, **CU Prague**, **IFCA**.
- Analysis tools: **CU Prague**, OSU Obninsk, LPNHE Paris
- Participation to the run: HIP Helsinki, IEKP Karlsruhe, OSU Obninsk, LPNHE Paris, CU Prague, IFIC Santander and contribution of DESY (beam & telescopes)

Test beam DAQ system in DESY for SiLC

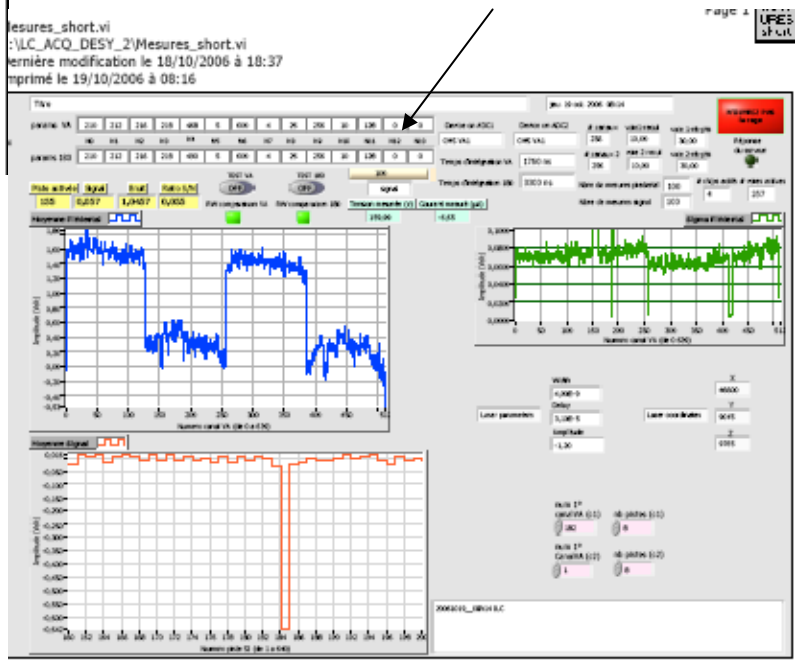




180nm UMC channel attached to CMS sensor module: response to LD1060 signal

<u>Before leaving for DESY</u>: the 4VA1 readout card and the 180UMC+VA1 card are working fine when reading out LD1060 signal at the Lab test bench

CMS-4VA1 response to LD1060

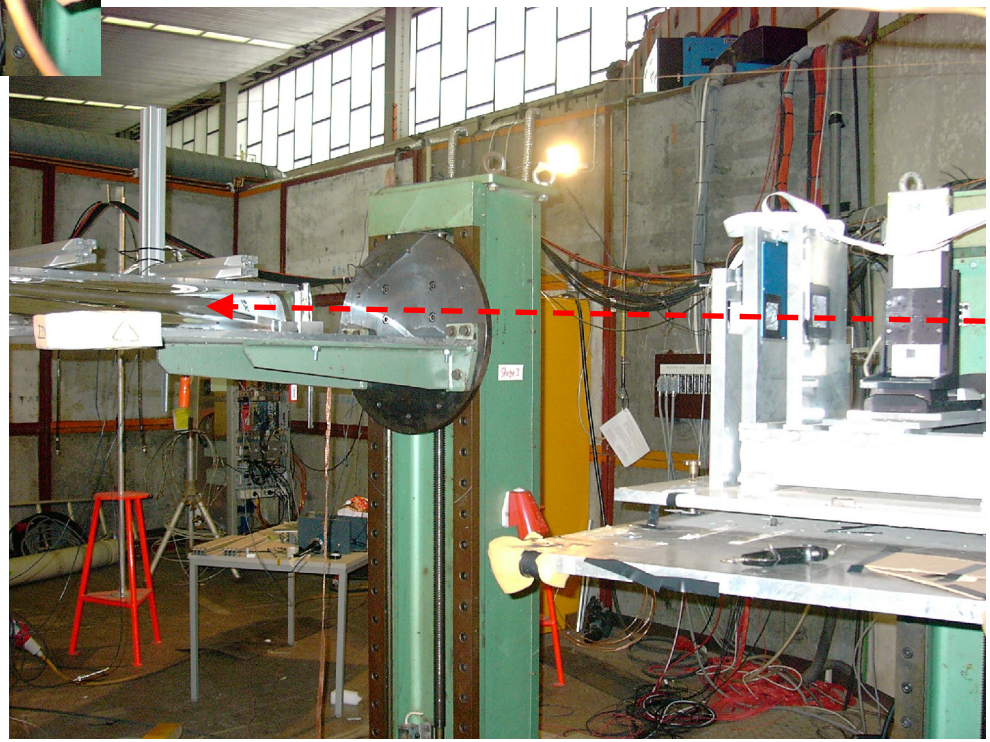



October 23 to November 3 2006
SiLC test beam at DESY
On line

First test beam achieved by the SiLC collaboration within also the EUDET framework
Using the test beam 22 in DESYElectron beam with beam energies 1 to 6 GeV
performed by:
HIP Helsinki, IEKP Karlsruhe, Obninsk State University, LPNHE- Paris,
Charles University Prague, IFCA Santander, IFIC Valencia
and the cooperation of:
IEHP Vienna (CMS sensors) Hamamatsu (GLAST sensors), CERN
for mounting and bonding the CMS modules) , DESY for the beam
infrastructure and telescopes (hardware & software)

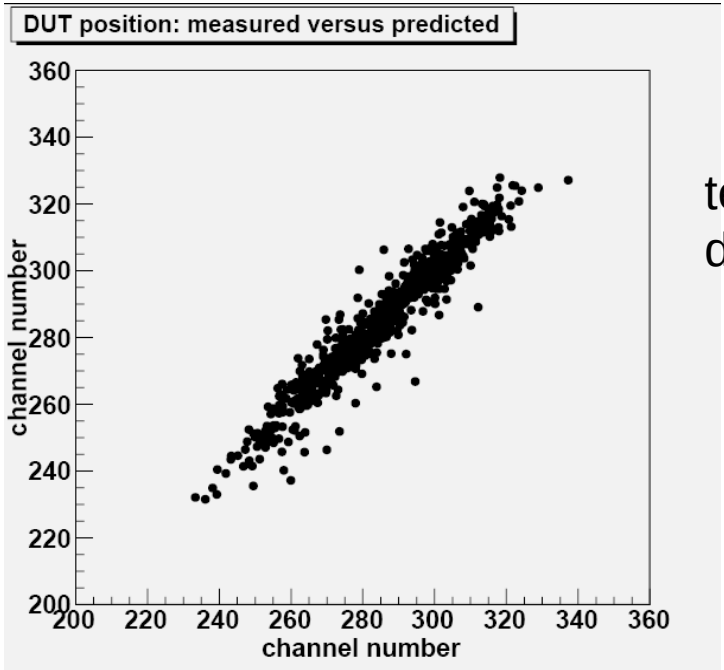
List of people:
Nick Van Remortel and Risto Orava (HIP-Helsinki)
Martin Frey, Frank Hartmann, Thomas Muller (IEKP Karlsruhe)
Valeri Saveliev (OSU)
Philippe Bailly, Wilfrid Dasilva, Jacques David, Guillaume Daubard, Marc Dhellot,
Jean François Genat, Patrick Ghislain, Jean François Huppert, Didier Imbault,
Frédéric Kapusta, Hervé Lebbolo, Tranh Hung Pham, Philippe Repain,
François Rossel, Aurore Savoy-Navarro, Rachid Sefri (LPNHE-Paris)
Zbynek Drasal, Peter Kvasnicka, Peter Kodys, Zdenek Dolezal (CU Prague)
Marcos Fernandez, Celso Martinez Rivero, Alberto Ruiz, Ivan Vila (IFCA-Santander)
Juan Fuster, Carlos Lacasta, Pablo Modesto (IFIC-Valencia)
Thomas Bergauer, Manfred Krammer, Winfred Mitaroff (IEHP-Vienna)
Alan Honma et al. (CERN)
Telescope and test beam DESY teams
(in red people having taken part to the shifts)

Test set-up 1: Two CMS modules
First one read out by 4VA1
Second one read out by
VA1&180nmUMC

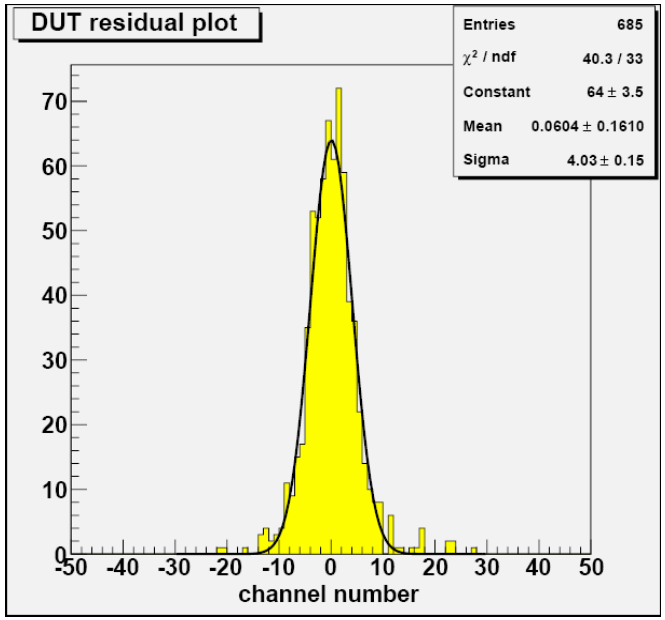


Test set-up 2: one GLAST module
read out by VA1&180nmUMC

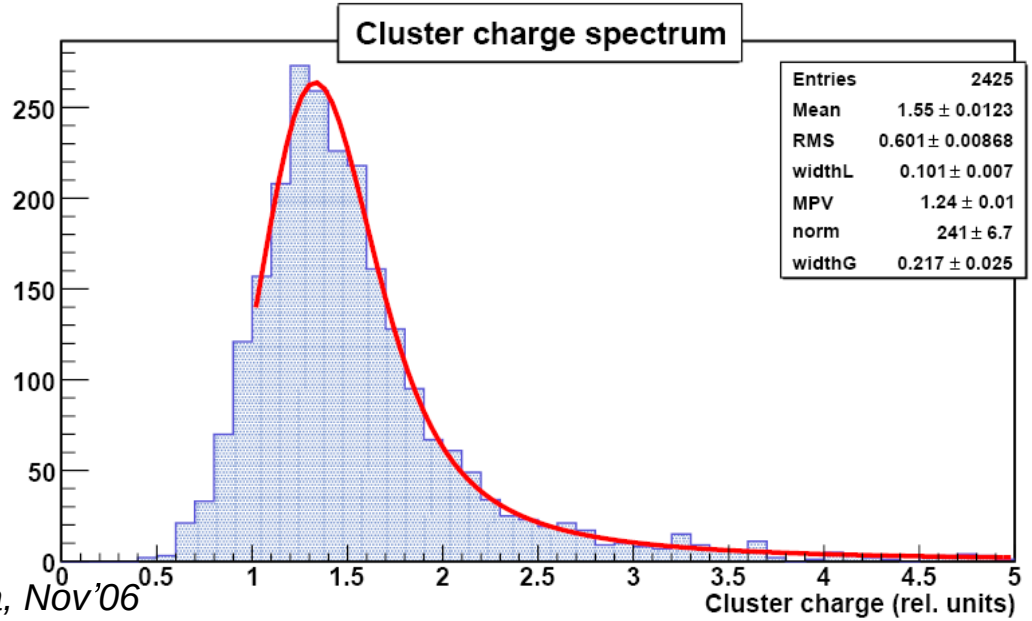
First hint to the data



Correlation beam telescopes & Silicon detector, based on the CMS-4VA1 module



Signal from the CMS-4VA1 module



Still two crucial challenges ahead of us before the end of the year:

- Beam test at DESY :
  - ► Analyse the collected data at the beam test.
  - ► Complete them by LD & radioactive source measurements.
- Test of the new chip 130nm
- Prepare next round at DESY (probably end January)

Topics

- R&D on new silicon sensors
- Towards the fabrication of new modules
- R&D on the electronics forefront
- 2006 beam test
- Prospects for 2007
  - Preparation of new beamtests
  - Developing Alignment
  - Developing Cooling

2007 Workpackages for SiLC/EUDET

WKP 0: Beam test in DESY (January-February 2007)
Pursuing the forthcoming test with 180nm and 130nm preprototypes.

WKP 1: Beam tests at CERN (July 2007)
« Rehearsal » for the November run:
- 2 modules made of 2 **new** 8'' single-sided sensors
readout: VA1(ref)+ **130nm-32ou64v (preproto128v)**
wiring chip-on-detector, new insulating box (related to cooling issue)
- 3D-planar module test

WKP2: Beam test at CERN or FNAL (?) (Nov. 2007)
- Prototype 60x60cm2, 8'' single-sided sensors
lecture VA1+130nm-128v, connectique chip/détecteur

Two times 2 weeks are requested to the CERN SPS coordinator

- *Other SiLC collaborators SiLC will join these beam tests and foresee to bring other detector prototypes. The hosting labs: CERN and FNAL (providing beam test 'infrastructure': DAQ, beam telescopes, mechanics…)*

- *December 2006 SiLC meeting in Barcelona: decisions on the baseline for 2007*

Work on all mechanical aspects including alignment, cooling,on developing further the FE-readout electronics and on addressing the associated DAQ will go on in //.

A. Savoy-Navarro, SiLC, Valencia, Nov'06

Workpackage 2, in 2007 is

Going from demonstrator to mini series for performing beam tests…

- Big step forward, new issues to be addressed on all the aspects of the project:
  Electronics, Mechanics, On-line & DAQ, data analyses.

- Strategy for tasks dispatching between collaborators (to be defined for 2007)

- Collaborations with Industrial firms (fabrication => quality tests)

- Importance of estimating the related risks (tasks dispatching, quality tests on Silicon sensors, chips, wiring or readout cards, industrial transfers, realistic cost evaluation)

Topics

- R&D on new silicon sensors
- Towards the fabrication of new modules
- R&D on the electronics forefront
- 2006 beam test
- Prospects for 2007
  - Preparation of new beamtests
  - Developing Alignment
  - Developing Cooling

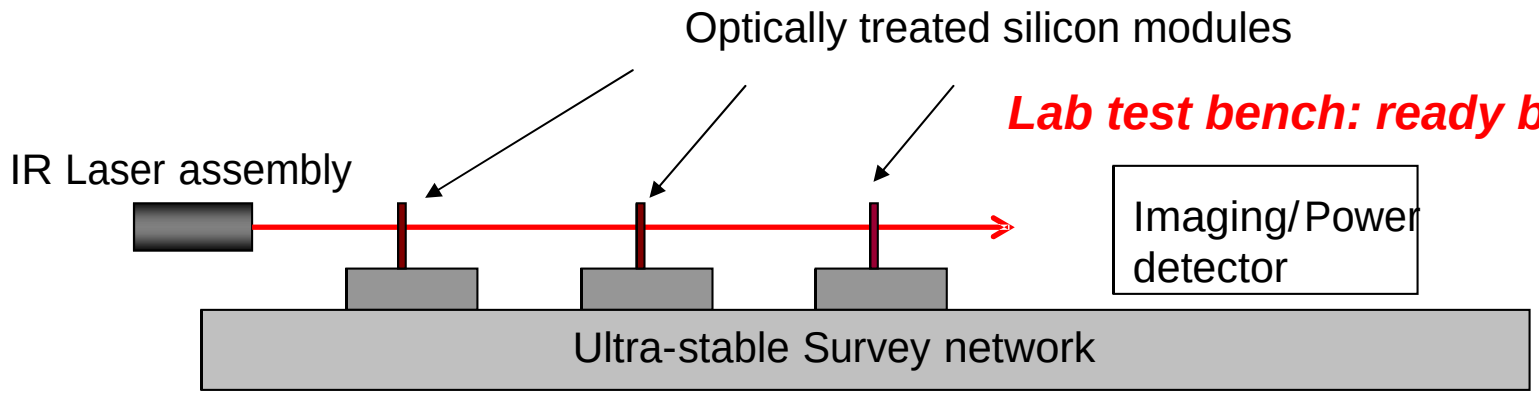
ALIGNMENT SYSTEM (IFCA)

Usage of collimated laser beams (IR spectrum) going through silicon detector modules . The laser beams would be detected directly in the Si-modules. This requires:

- Silicon module surface requires special treatement to improved its optical quality/transmitance
- Dedicated ultra-stable test stand for “optical” characterization of the modified silicon modules: reflectivity, transmitance, absorption, polarization sensitivity, wedge effect, response uniformity...

Main advantages:

Particle tracks and laser beam share the same sensors removing the need of any mechanical transfer.
Minimum interference with Silicon support structures
No precise positioning of the aiming of the collimators. The number of measurements has to be redundant enough



Lab test bench: ready by April 07

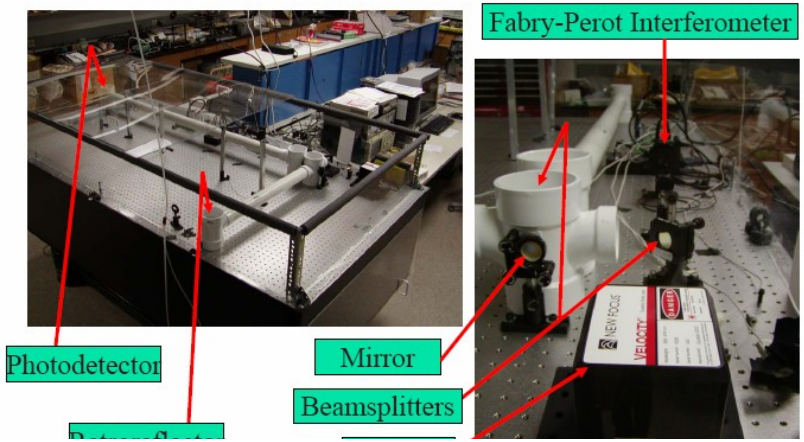
A. Savoy-Navarro, SiLC, Valencia, Nov’06

Frequency Scanned Interferometry for ILC Tracker Alignment

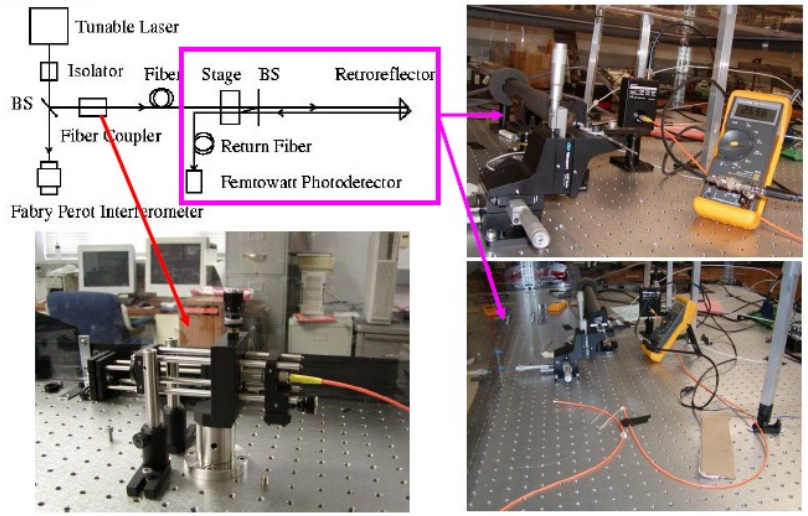
University of Michigan ILC Group

(Hai-Jun Yang, Eui Min Jung, Sven Nyberg, Keith Riles)

FSI Demonstration System (I)



FSI with Optical Fibers (II)



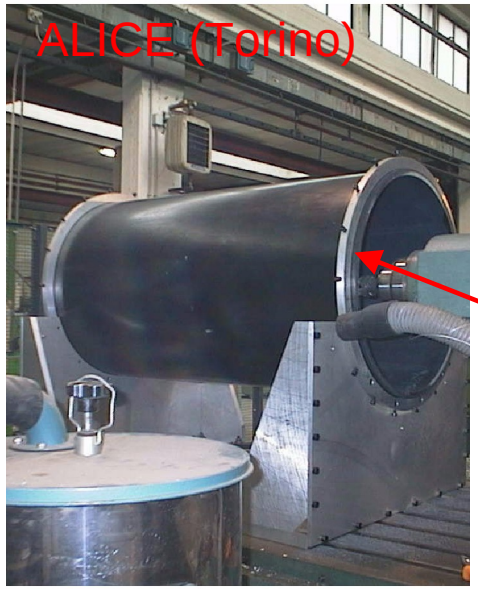
Summary and Outlook

- Several FSI demonstration systems with increasing realism have been implemented
- Results on achievable measurement precision are quite promising (~0.2 μ m with dual-laser scanning)
- Plans:
  - Miniaturization
  - Multiple channels
  - Simulation (not discussed today)

COOLING SYSTEM

A cooling system prototype must be provided for next year (EUDET). Various studies were performed with mechanical prototypes in Paris.
In the actual ILC environment for the Silicon tracking system the cooling system is defined by the following conditions:

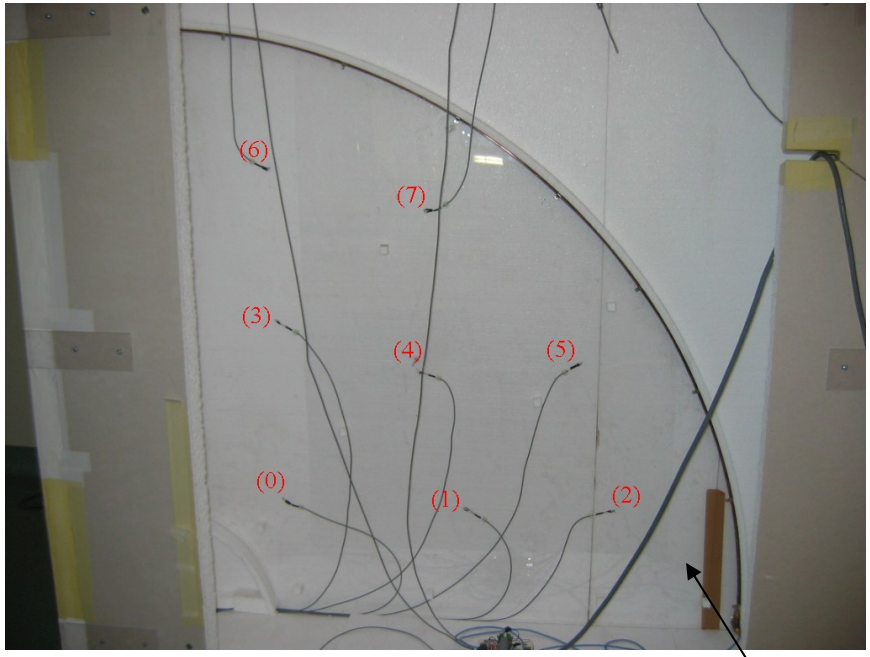
- Taking as hypothesis that the relatively low radiation level allows to reach up to 30 degrees maximum temperature
- And a temperature gradiant of 10 degrees C,
- With a power dissipation per electronic channel of no more than 1mW
- The main need for cooling is to preserve the detector from the environmental conditions, i.e. the heat provided by the other devices.
- Plus the need for a Faraday envelope.
- Reducing the material budget for this envelope is a prerequisit.

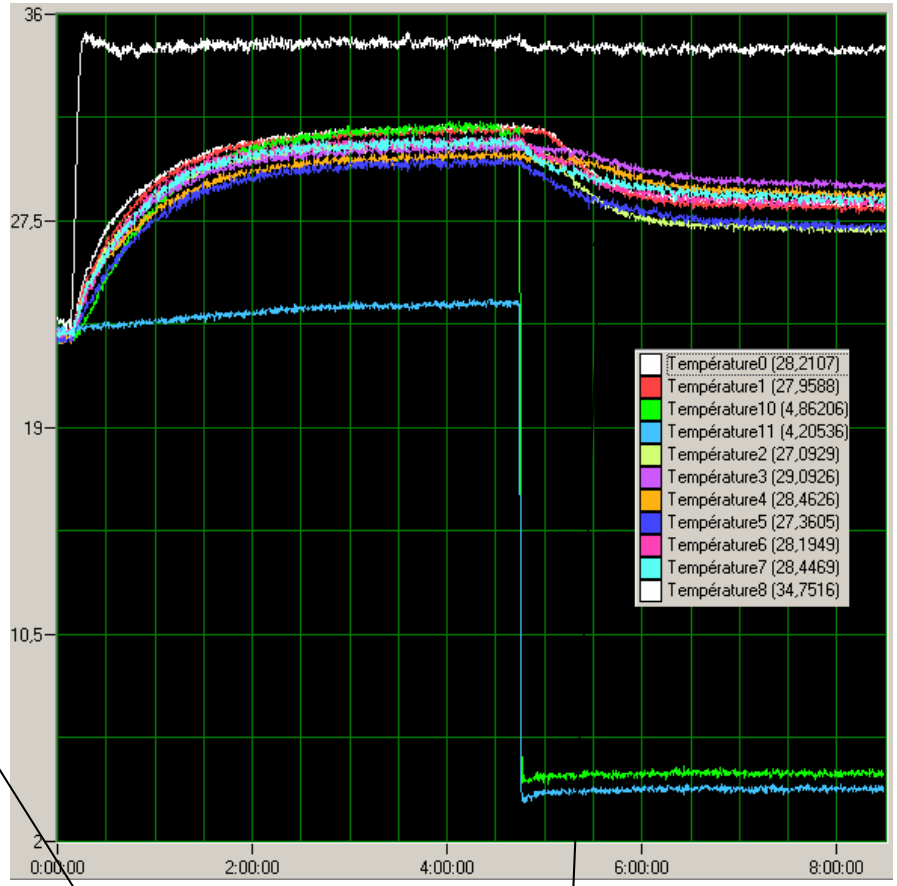


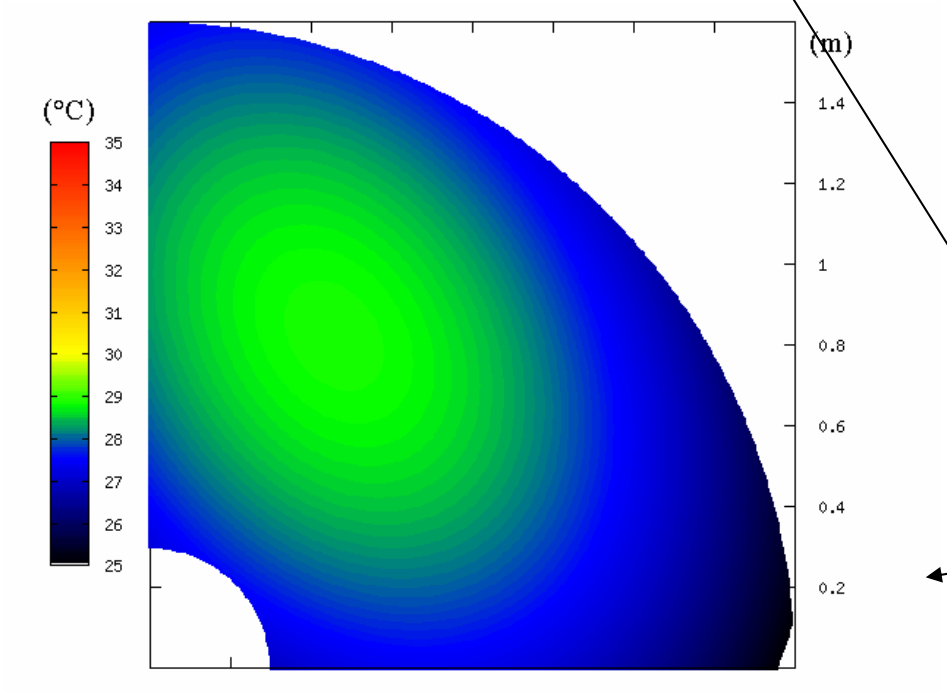
Studies are underway profiting for the expertise acquired at LHC, example:

Cylinder: 1.2m length
by 0.62 diameter
4+4 PLIES => 1,2 mm
ROHACELL => 5 mm
0,5% X0
WEIGHT = 10 kg

Example of thermo mechanical studies for the End Cap Si tracker (LPNHE-Paris)

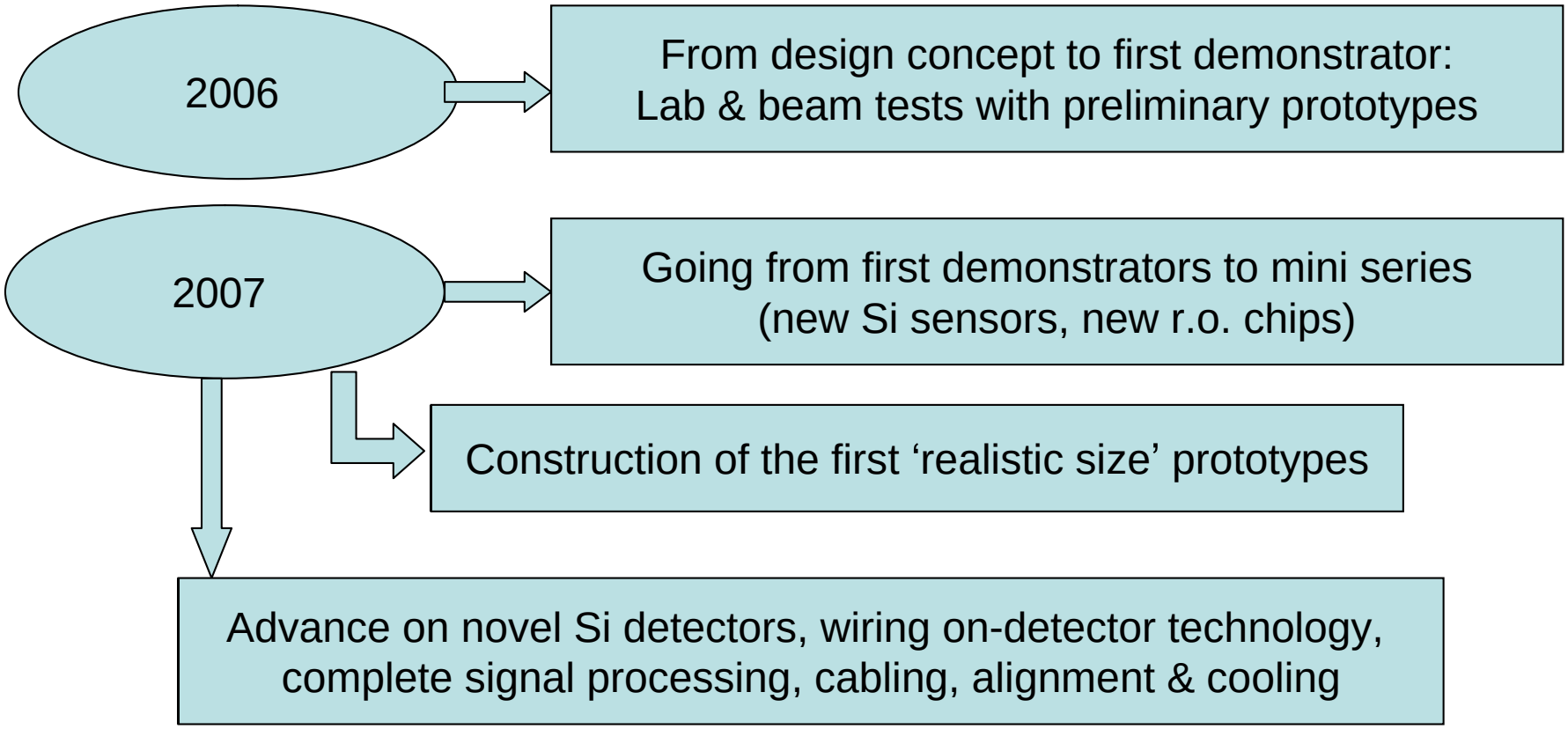






Measurements, results and modelling

Transitions of phase:



In 2006, the first SiLC test beam has triggered the unification of the European collaborative efforts.
The 2007 SiLC beam tests will include the contributions of Asia and US

A. Savoy-Navarro, SiLC, Valencia, Nov’06