LCFI Status Report: Vertex Detector R&D

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- **Brief introduction**
- **Vertex Detector R&D**
  - **Column-Parallel CCDs**
  - **In-situ Storage Image Sensors**
- **Mechanical support studies**
- **Plans**

Introduction

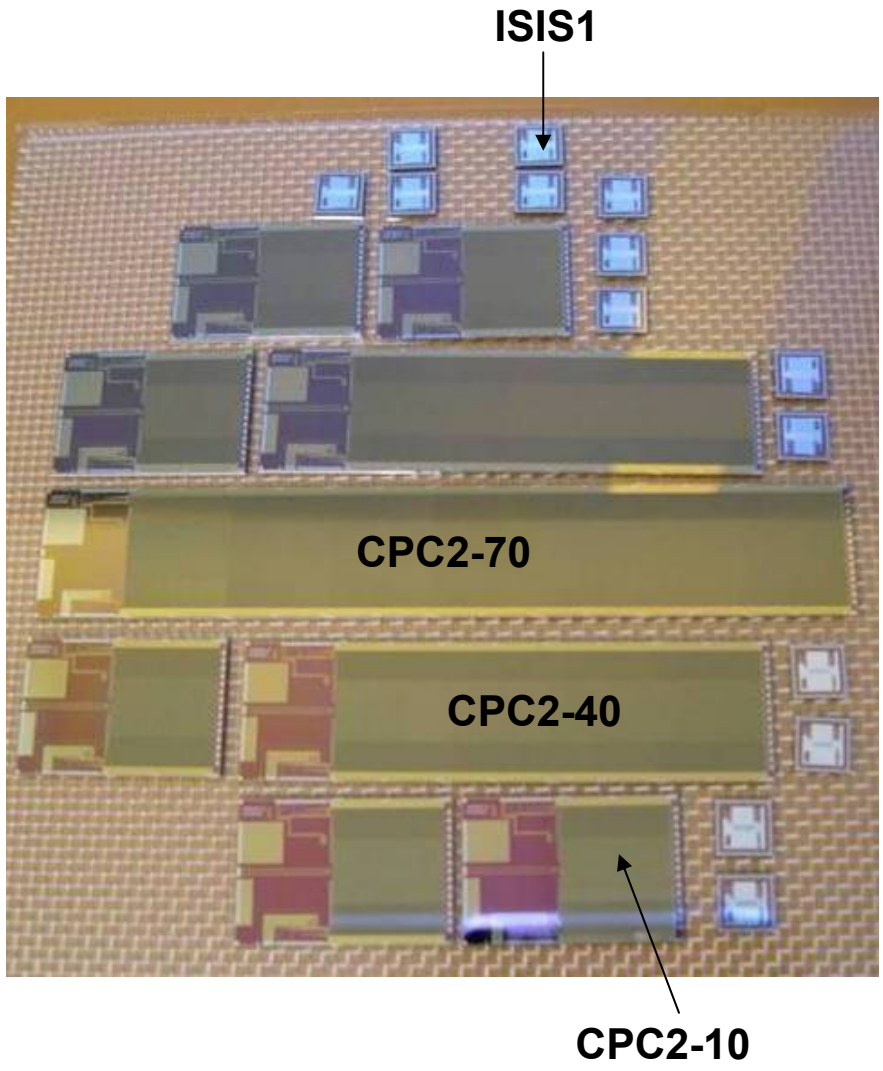
What is required for the vertex detector at ILC:

- Excellent point resolution (3.5 μm), small pixel size = 20 μm, close to IP
- Low material budget (≤ 0.1% X_0 per layer), low power dissipation
- Fast (low occupancy) readout – challenging, two main approaches
- Tolerates Electro-Magnetic Interference (EMI)

What LCFI has done so far:

- Made 2 generations of Column Parallel CCDs: CPC1 and CPC2
- In-situ Storage Image Sensor – proof of principle device ISIS1 designed and tested
- CMOS readout chips for CPC1/2: 2 generations, bump bonded to the CCDs
- Driver chip for CPC2 designed and manufactured
- Built lots of electronics to support the detectors
- Extensive tests of stand-alone devices and hybrid bump-bonded assemblies

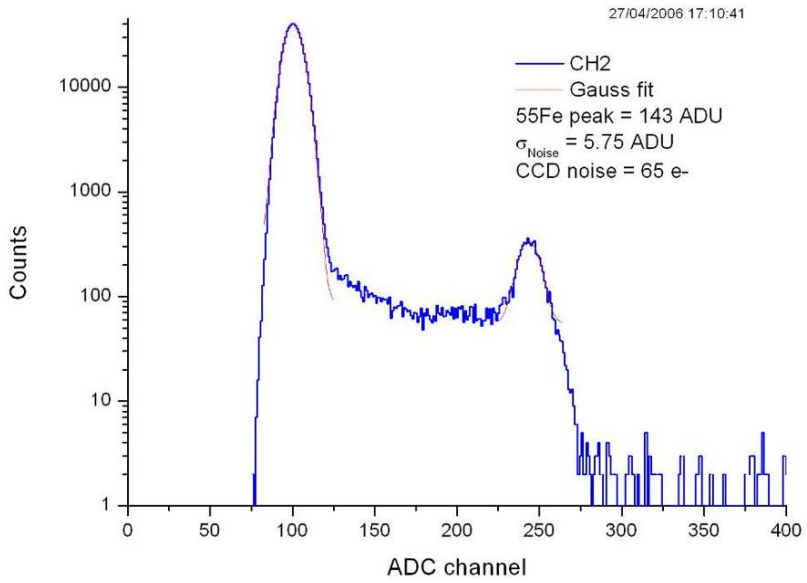
Second Generation CPCCD : CPC2



- 6 wafers with single level metal:
  - ❖ Four CPC2 wafers (3 × 100 Ω.cm/25 µm epi and one 1.5kΩ.cm/50 µm epi)
  - ❖ Two 100 Ω.cm wafers sent to VTT for bump bonding
- 2 CPC2 wafers with 2-level metal (busline-free CCD) delivered
  - ❖ Designed to reach 50 MHz operation
  - ❖ Important milestone for LCFI
- We have another 12 wafers to be processed after evaluation of the present variants

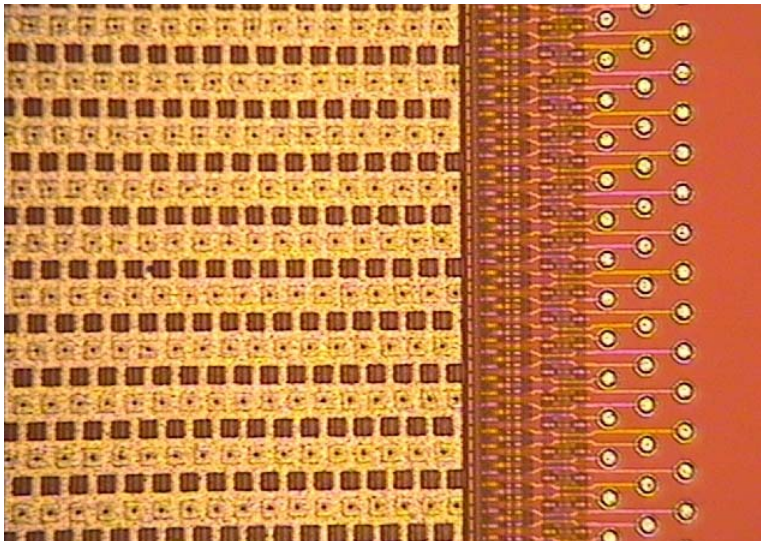
Yield from 4 CPC2 wafers: 71% for CPC2-10, 63% for CPC2-40, 25% for CPC2-70

CPC2



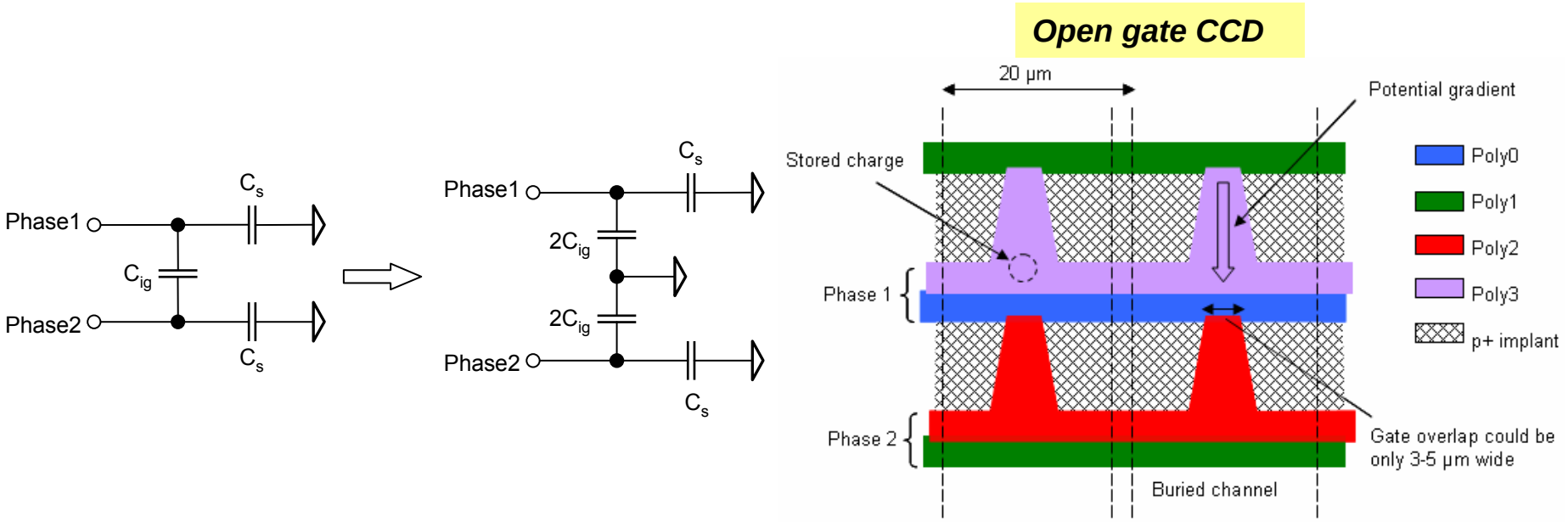
- CPC2-10 (low speed version) works fine, here at 1 MHz clock
- ^{55}Fe spectrum at -40 °C and 500 ms integration time
- Noise is a bit too high, external electronics is suspected

Busline-free CPC2



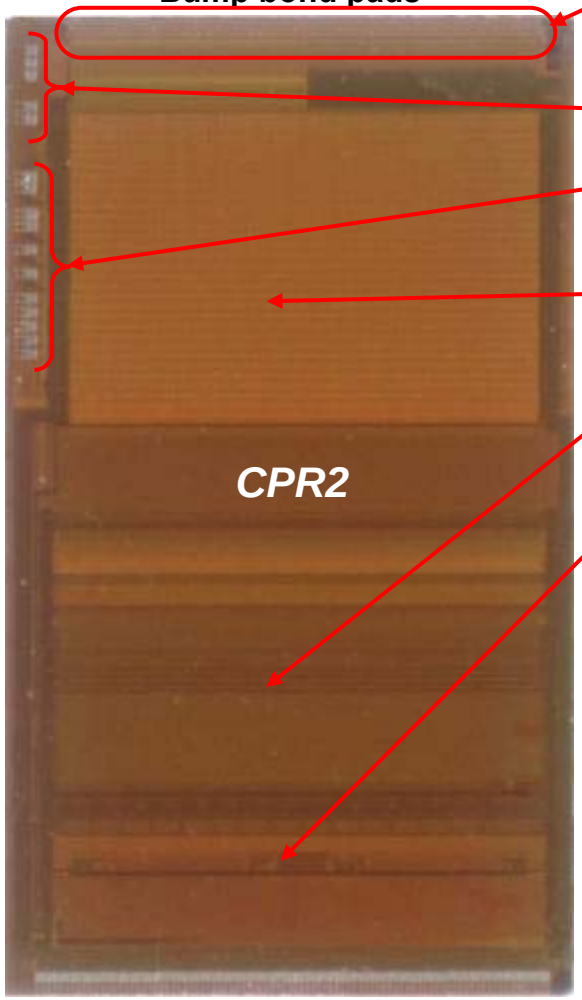
- Devices with 2-level metal clock distribution for high speed (busline-free) have been received
  - ❖ The whole image area serves as a distributed busline
- CPC2 chips bump-bonded to CPR2 have also been received
- Tests will follow immediately

New Ideas: CCDs for Capacitance Reduction



- **High CCD capacitance is a challenge to drive because of the currents involved**
  - **Can we reduce the capacitance? Can we reduce the clock amplitude as well?**
  - **Inter-gate capacitance C_{ig} is dominant, depends mostly on the size of the gaps and the gate area**
  - **Open phase CCD, "Pedestal Gate CCD", "Shaped Channel CCD" – new ideas under development, could reduce C_{ig} by ~4!**
- **Currently designing small CCDs to test several ideas on low clock and low capacitance, together with e2V Technologies**

Readout Chips – CPR1 and CPR2



Voltage and charge amplifiers 125 channels each

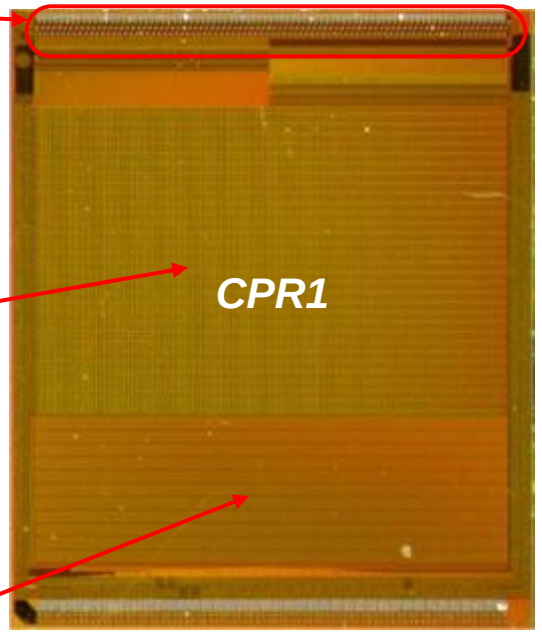
Analogue test I/O

Digital test I/O

5-bit flash ADCs on 20 μm pitch

Cluster finding logic (2×2 kernel)

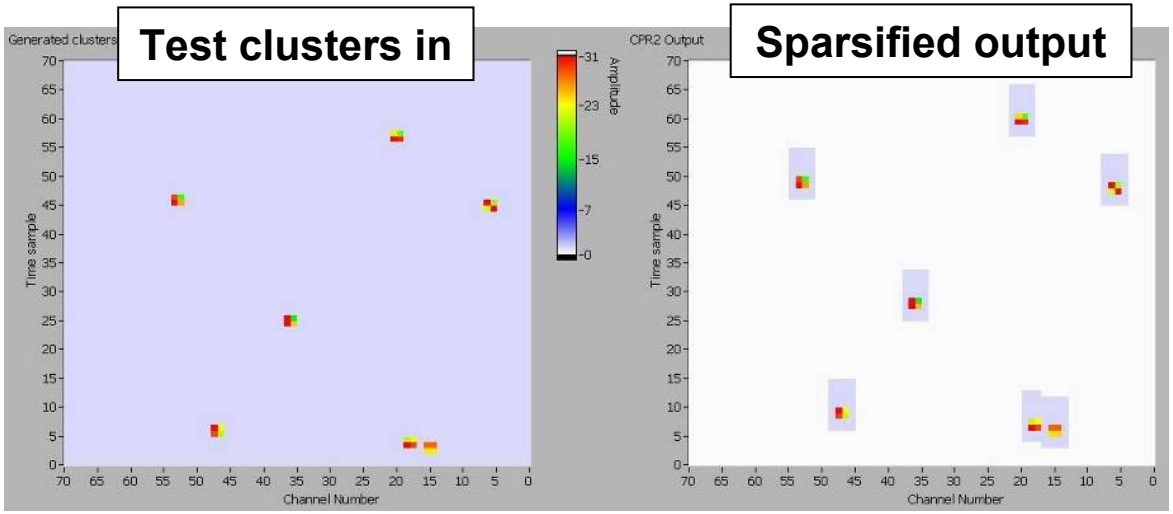
Sparse readout circuitry



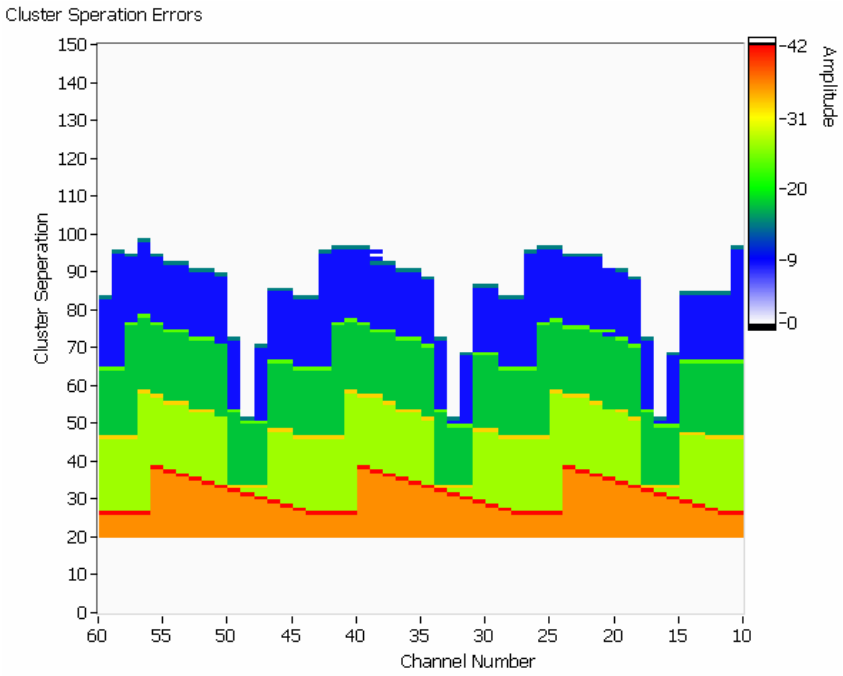
- CPR2 designed for CPC2
- Results from CPR1 taken into account
- Numerous test features
- Size : 6 mm × 9.5 mm
- 0.25 μm CMOS process (IBM)
- Manufactured and delivered February 2005

Steve Thomas/Peter Murray, RAL

CPR2 Test Results



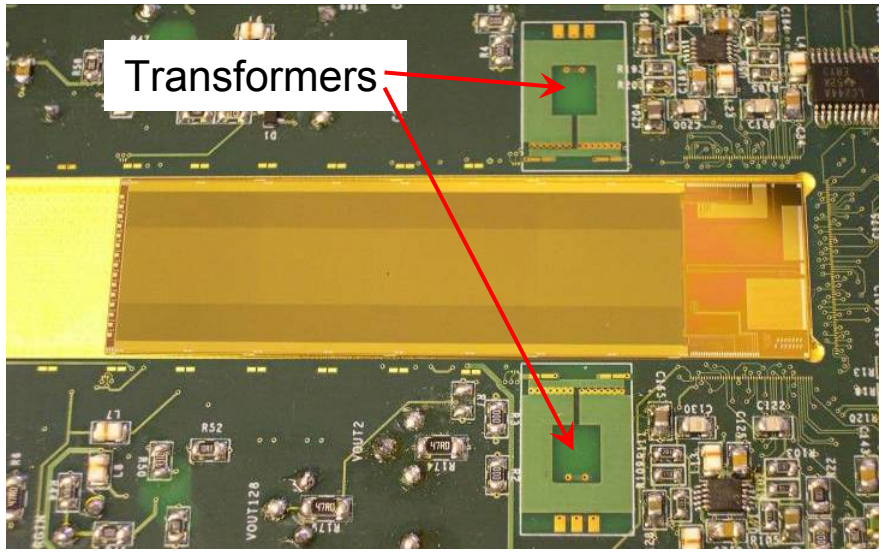
- Parallel cluster finder with 2×2 kernel
- Global threshold
- Upon exceeding the threshold, 4×9 pixels around the cluster are flagged for readout



- Tests on the cluster finder: works!
- Several minor problems, but chip is usable
- Design occupancy is 1%
- Cluster separation studies:
  - ❖ Errors as the distance between the clusters decreases – reveal dead time
- Extensive range of improvements to be implemented in the next version (CPR2A)
- CPR2A design has started

Thanks to Tim Woolliscroft, Liverpool U

Clock Drive for CPC2



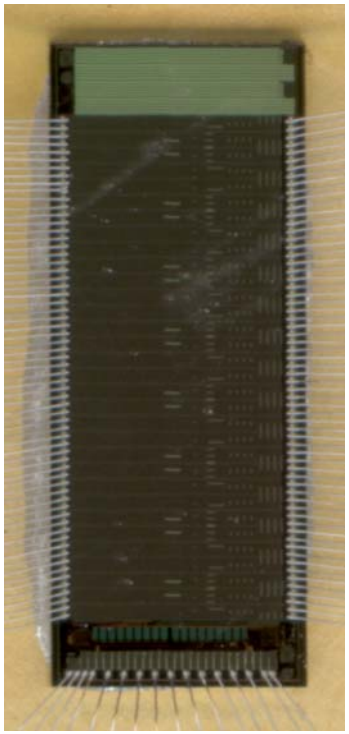
Johan Fopma/Brian Hawes, Oxford U

Transformer driver:

- Requirements: 2 $V_{pk\text{-}pk}$ at 50 MHz over 40 nF (half CPC2-40);
- Planar air core transformers on 10-layer PCB, 1 cm square
- Parasitic inductance of bond wires is a major effect – fully simulated;
- Will work with the high speed busline-free CCD

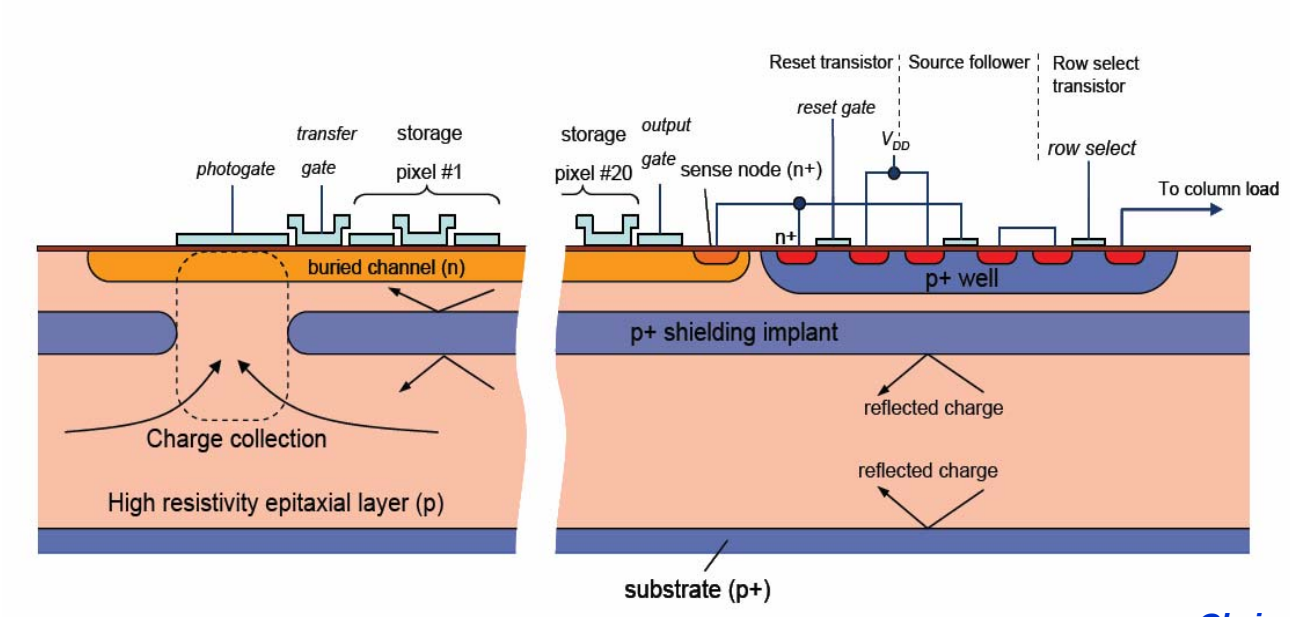
Chip Driver CPD1:

- Designed to drive the outer layer CCDs (127 nF/phase) at 25 MHz and the L1 CCD (40 nF/phase) at 50 MHz
- One chip drives 2 phases, 3.3 V clock swing
- 0.35 μm CMOS process, chip size 3×8 mm^2
- CPC2 requires 21 Amps/phase!
- Delivered in October



Steve Thomas/Peter Murray, RAL

In-situ Storage Image Sensor (ISIS)

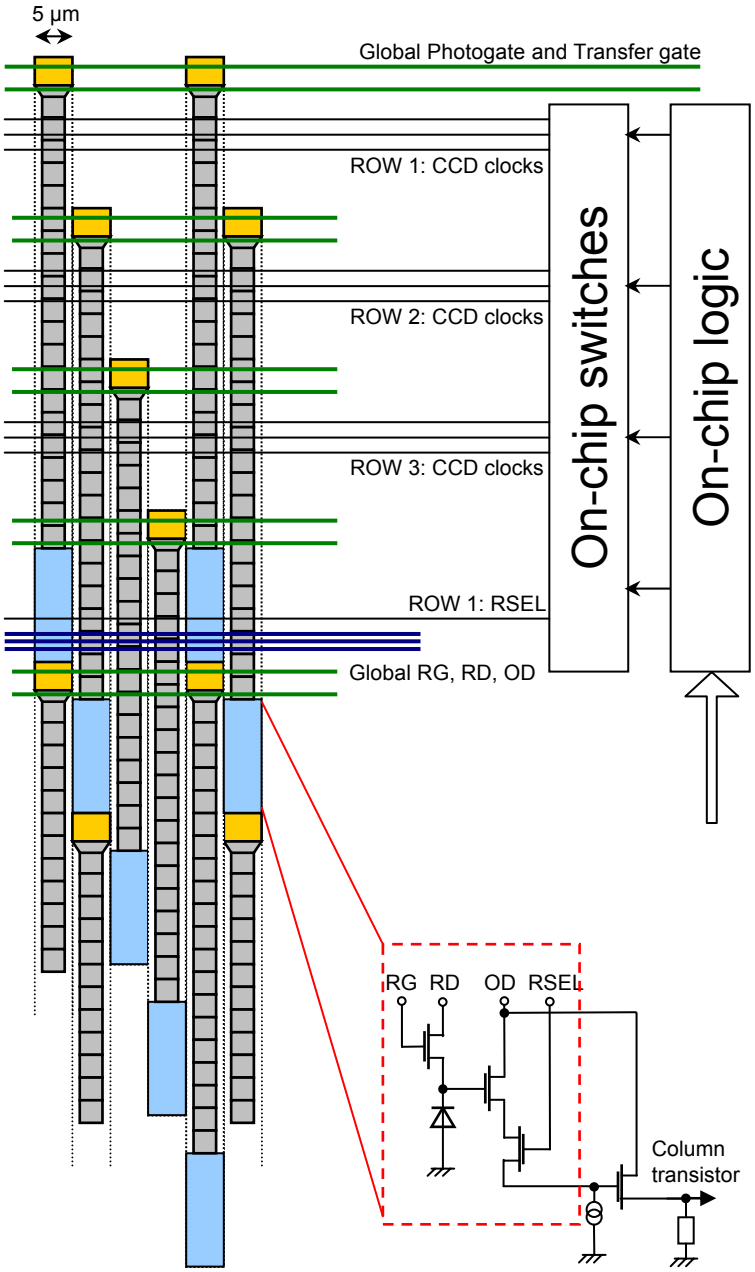


Chris Damerell, RAL

Operating principles of the ISIS:

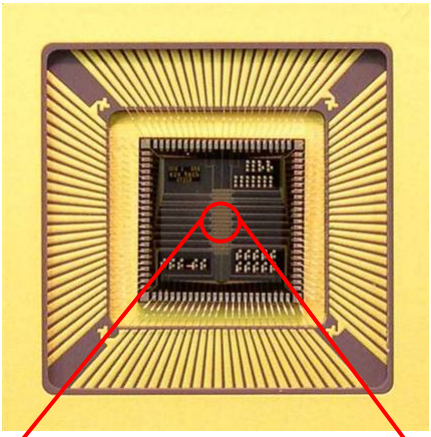
1. **Charge collected under a photogate;**
2. **Charge is transferred to 20-pixel storage CCD in situ, 20 times during the 1 ms-long train;**
3. **Conversion to voltage and readout in the 200 ms-long quiet period after the train (insensitive to beam-related RF pickup);**
4. **1 MHz column-parallel readout is sufficient;**

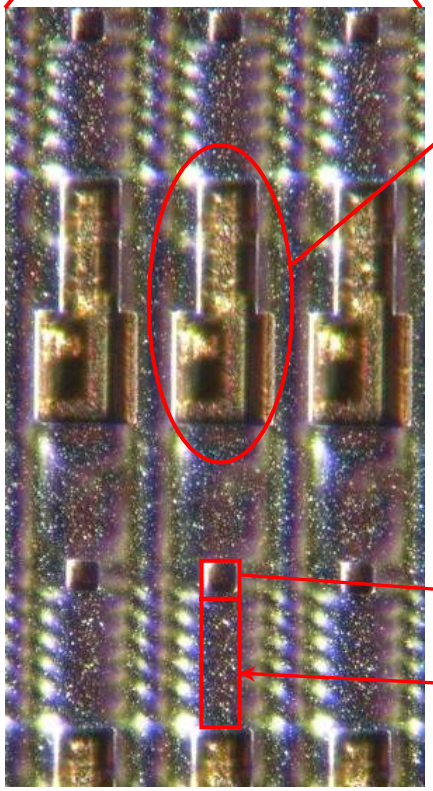
In-situ Storage Image Sensor (ISIS)



- The ISIS offers significant advantages:
  - ❖ **Easy to drive** because of the low clock frequency: 20 kHz during capture, 1 MHz during readout
  - ❖ ~100 times more **radiation hard** than CCDs (less charge transfers)
  - ❖ **Very robust to beam-induced RF pickup**
- ISIS combines CCDs, active pixel transistors and edge electronics in one device: **specialised process**
- Development and design of ISIS is more ambitious goal than CPCCD
- "Proof of principle" device (ISIS1) designed and manufactured by e2V Technologies

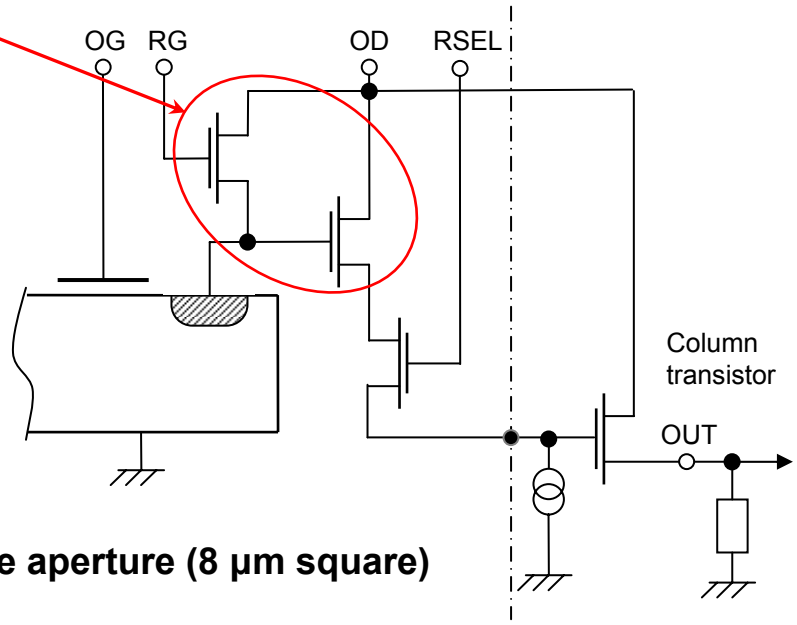
The ISIS1 Cell





- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each;
- Cell pitch 40 μm × 160 μm, no edge logic (pure CCD process)
- Chip size ≈ 6.5 mm × 6.5 mm

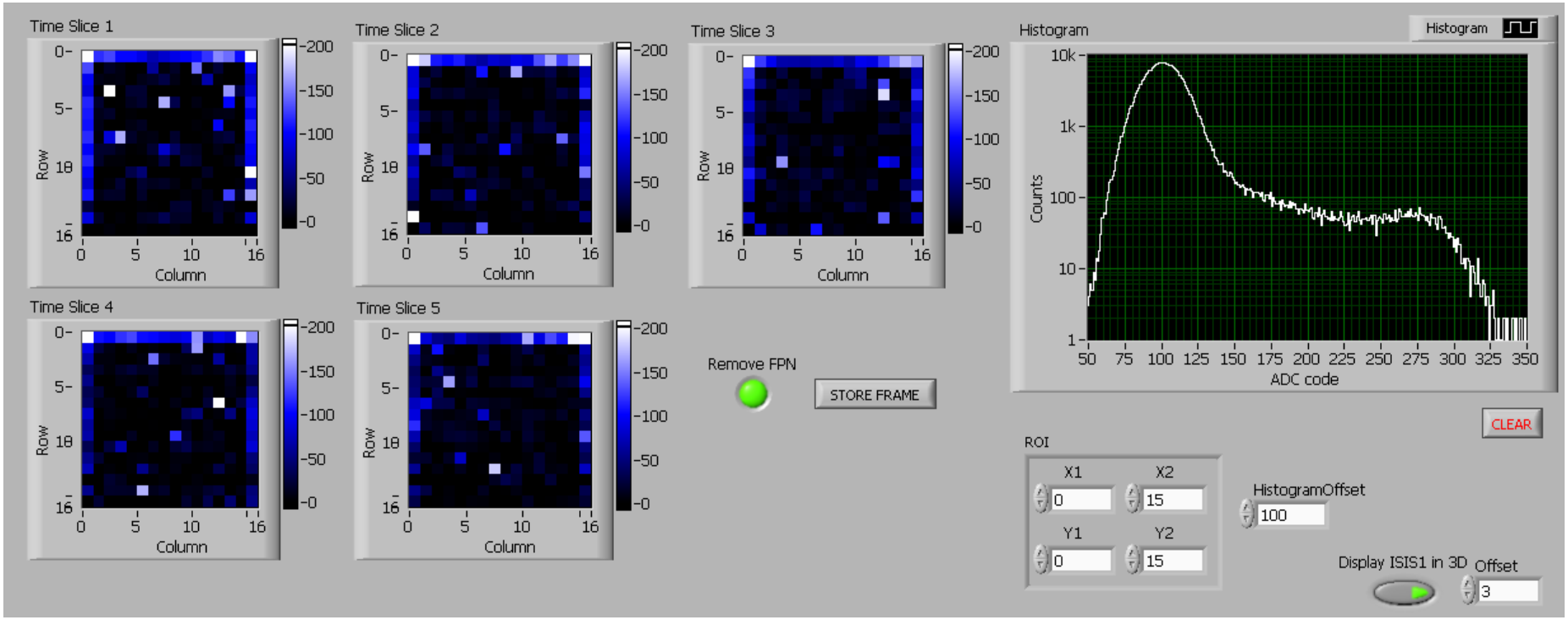
Output and reset transistors



Photogate aperture (8 μm square)

CCD (5×6.75 μm pixels)

Tests of ISIS1

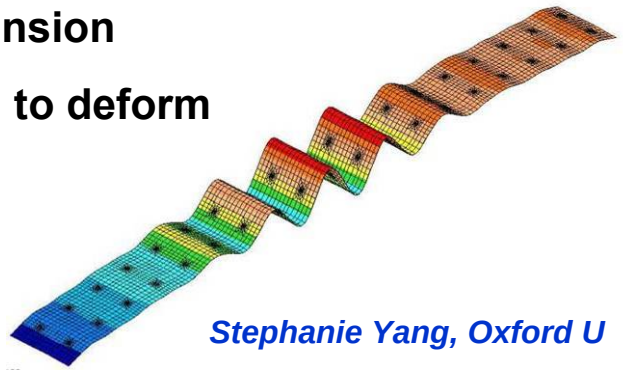


Tests with ^{55}Fe source

- The top row and 2 side columns are not protected and collect diffusing charge
- The bottom row is protected by the output circuitry
- ISIS1 without *p*-well tested first and works OK
- ISIS1 with *p*-well has very large transistor thresholds, permanently off – re-run agreed with e2V

Mechanical Support Studies

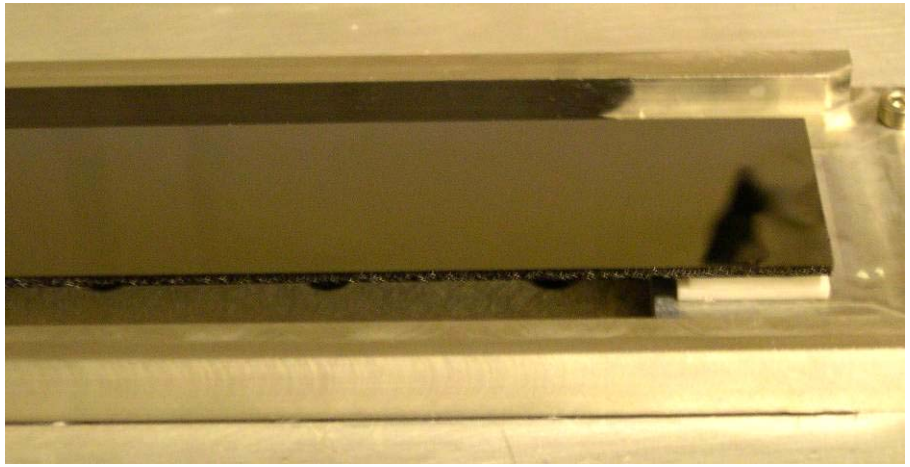
- Goal is 0.1% X_0 per ladder or better, while allowing low temperature operation (~170 K)
- Active detector thickness is only 20 μm
- Unsupported silicon
  - ❖ Stretched thin sensor (50 μm), prone to lateral deformation
  - ❖ Fragile, practically abandoned
- Silicon on thin substrates
  - Sensor glued to semi-rigid substrate held under tension
  - Thermal mismatch is an issue – causes the silicon to deform
  - Many studies done for Be substrate
- Silicon on rigid substrates
  - Shape maintained by the substrate
  - Materials with good thermal properties available
  - Foams offer low density and mass while maintaining strength



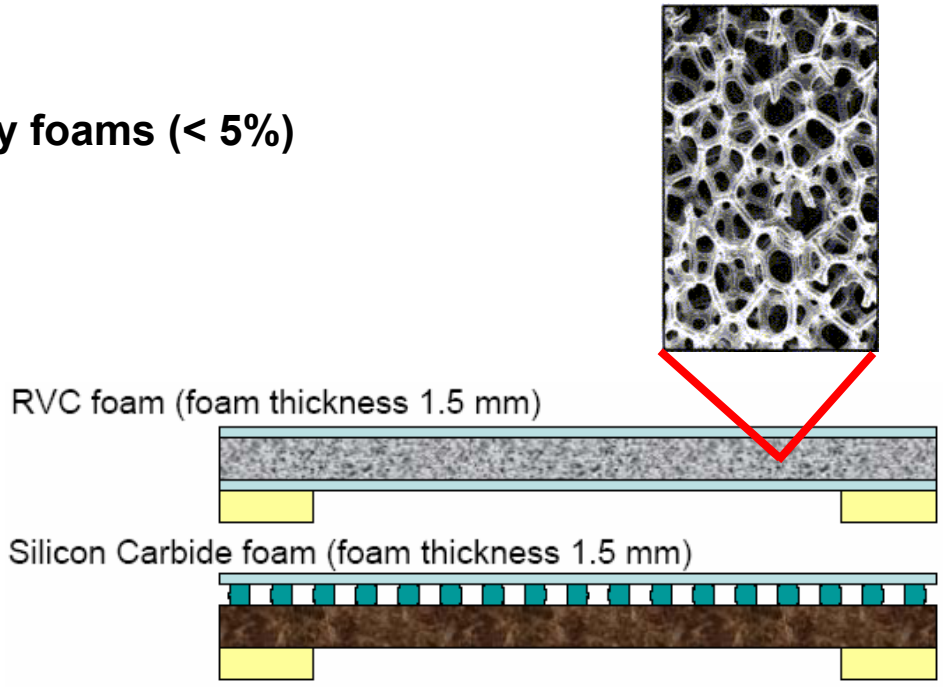
Stephanie Yang, Oxford U

Mechanical Support Studies

- RVC (Reticulated Vitreous Carbon) and silicon carbide are excellent thermal match to silicon
- Silicon-RVC foam sandwich (~ 3% density)
  - Foam (1.5mm thick), sandwiched between two 25 μm silicon pieces – required for rigidity
  - Achieves 0.09% X_0
- Silicon on SiC foam (~ 8% density)
  - Silicon (25 μm) on SiC foam (1.5mm);
  - Achieves 0.16% X_0
  - 0.09% X_0 possible with lower density foams (< 5%)



Thanks to Erik Johnson, RAL

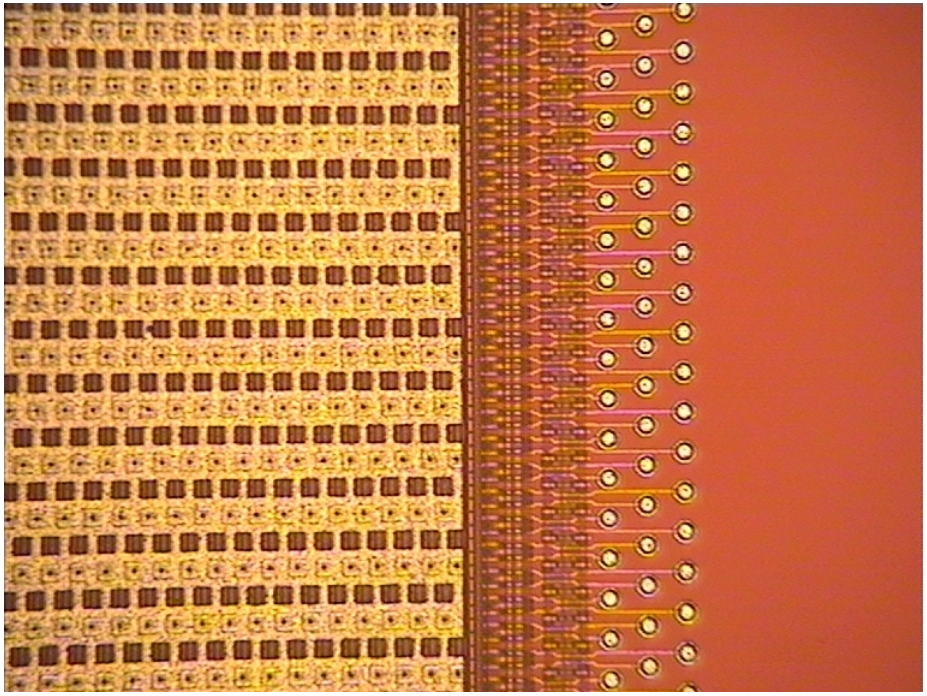


Conclusion and Plans

- Detector R&D is progressing very well
- CPCCD program most advanced:
  - ❖ Second generation high speed CPCCD will be evaluated
  - ❖ Hybrid assemblies CPC2/CPR2 delivered, tests imminent
  - ❖ Programme for capacitance and clock amplitude reduction is underway
  - ❖ Driver system under development
    - ❖ CMOS driver chip already designed and delivered
    - ❖ Transformer drive also pursued
  - ❖ Third generation CMOS readout chips for CPC1/2 in design stage
- ISIS work:
  - "Proof of principle" device works
  - Design of second generation, small pixel ISIS2 will follow next year
- Mechanical support aims at $\leq 0.1\%$ X_0 using modern materials

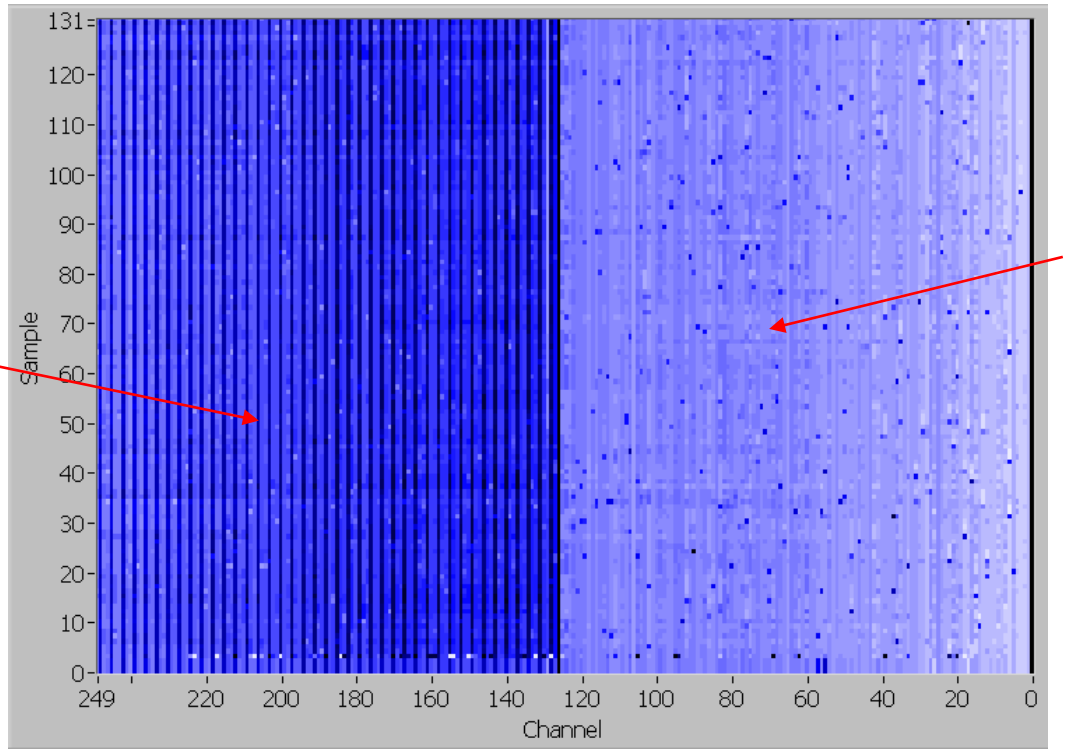
Visit us at http://hepwww.rl.ac.uk/lcfi/

Extra Slides



CPC1/CPR1 Performance

5.9 keV X-ray hits, 1 MHz column-parallel readout



Charge outputs, inverting (positive signals)

Noise ≈100 e-

Voltage outputs, non-inverting (negative signals)

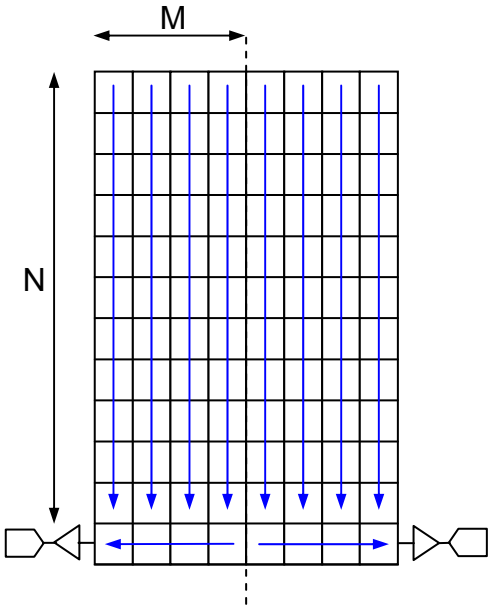
Noise ≈60 e-

- **First time e2V CCDs have been bump-bonded**
- **High quality bumps, but assembly yield only 30% : mechanical damage during compression suspected**
- **Differential non-linearity in ADCs (100 mV full scale) : addressed in CPR2**

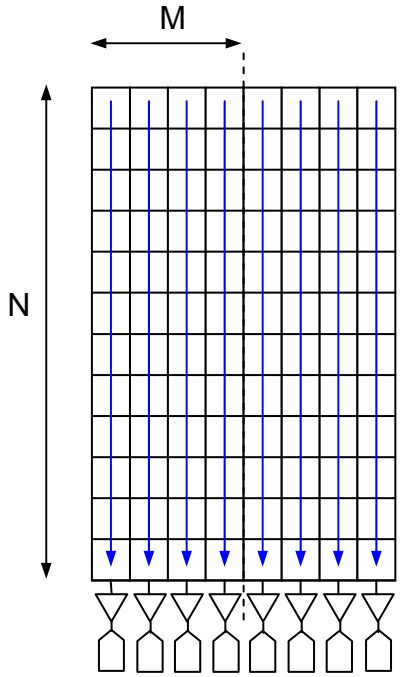
Bump bonds on CPC1 under microscope

The Column Parallel CCD

- **Main detector work at LCFI**
- **Every column has its own amplifier and ADC – requires readout chip**
- **Readout time shortened by orders of magnitude**
- **All of the image area clocked, complicated by the large gate capacitance**
- **Optimised for low voltage clocks to reduce power dissipation**



"Classic CCD"
Readout time ≈ $N \times M / f_{out}$



Column Parallel CCD
Readout time = N / f_{out}