Front-End electronics for Future Linear Collider calorimeters

IN2P3
Institut National de Physique Nucléaire et de Physique des Particules

C. de La Taille
IN2P3/LAL Orsay

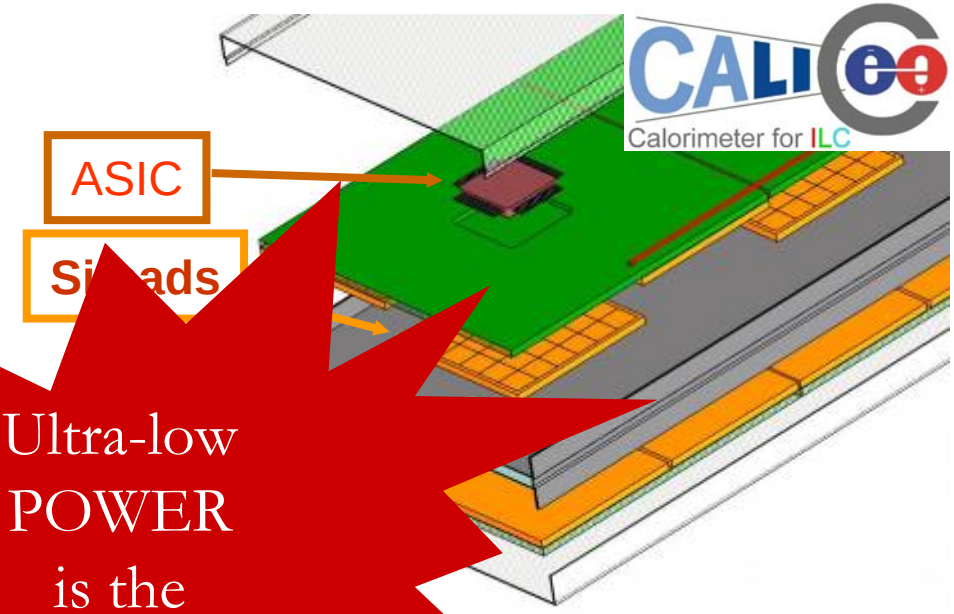
on behalf of the CALICE and EUDET collaborations

http::/www.lal.in2p3.fr/technique/se/flc

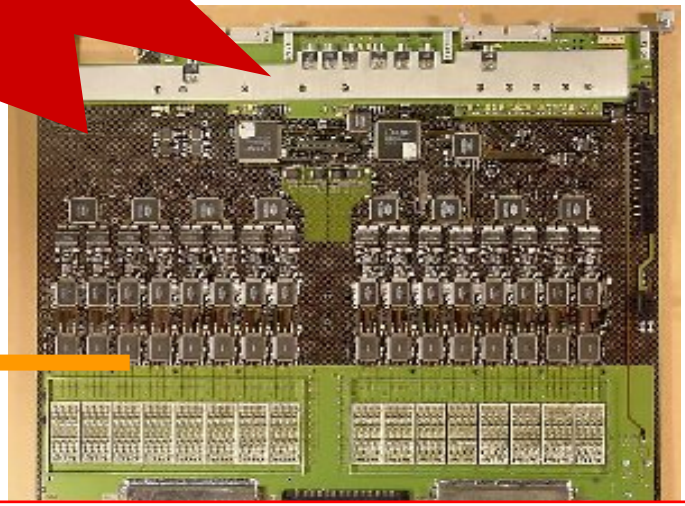
Slides from M. Anduze, J.C. Brient, S. Blin, C. Jauffret, J. Fleury, G. Martin-Chassard, N. Seguin-Moreau, L. Raux, F. Sefkow

ILC Challenges for electronics

- **Requirements for electronics**
  - Large dynamic range (15 bits)
  - Auto-trigger on ½ MIP
  - On chip zero suppress
  - Front-end embedded in detec
  - **Ultra-low power : (« 100**
  - 10^8 channels
  - Compactness
- **« Tracker electronics wi performance »**



Ultra-low POWER is the KEY issue

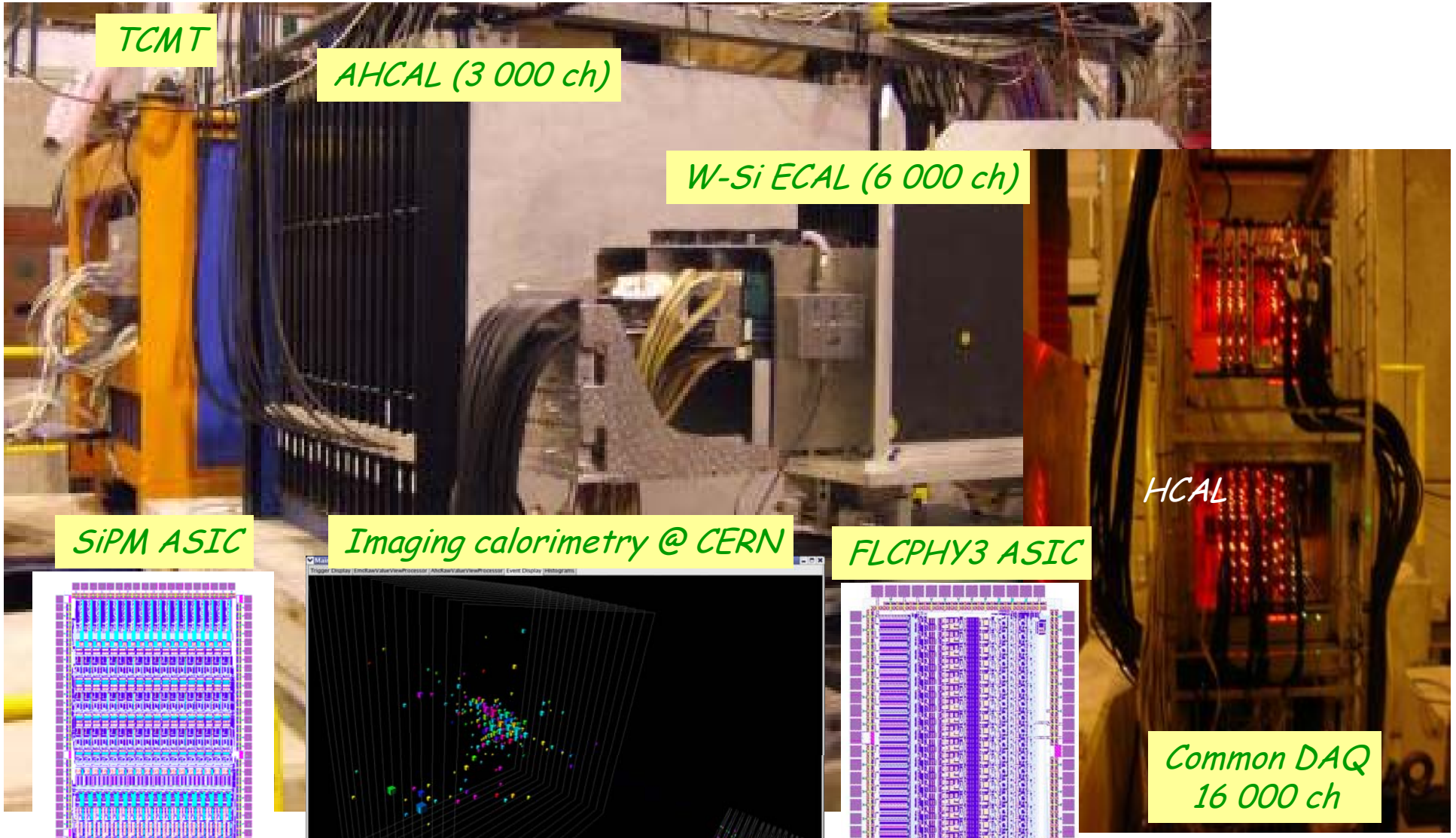


ILC : **100µW/ch**

FLC_PHY3 18ch 10*10mm **5mW/ch**

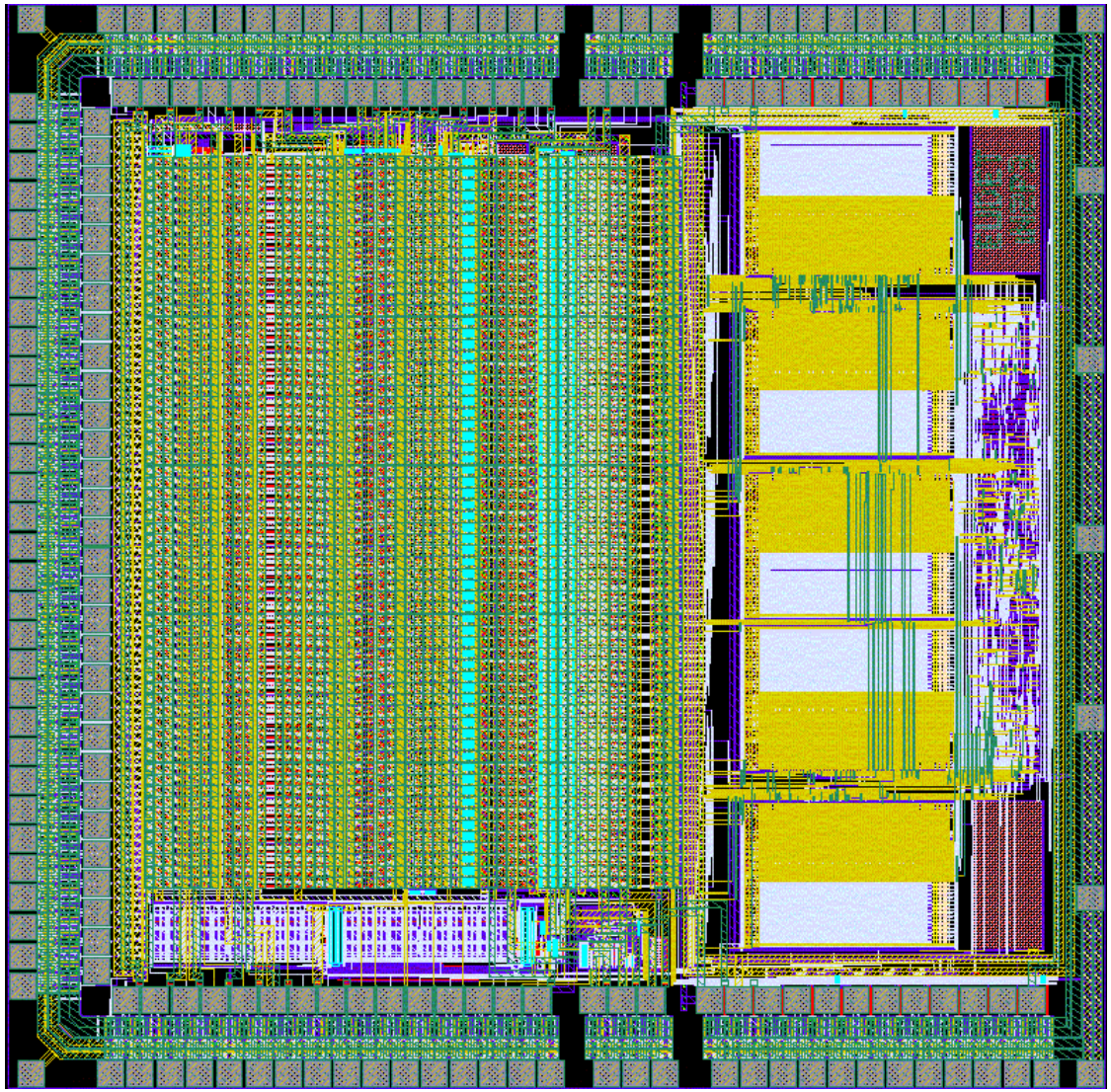
ATLAS LAr FEB 128ch 400*500mm **1 W/ch**

CALICE Testbeam at CERN SPS

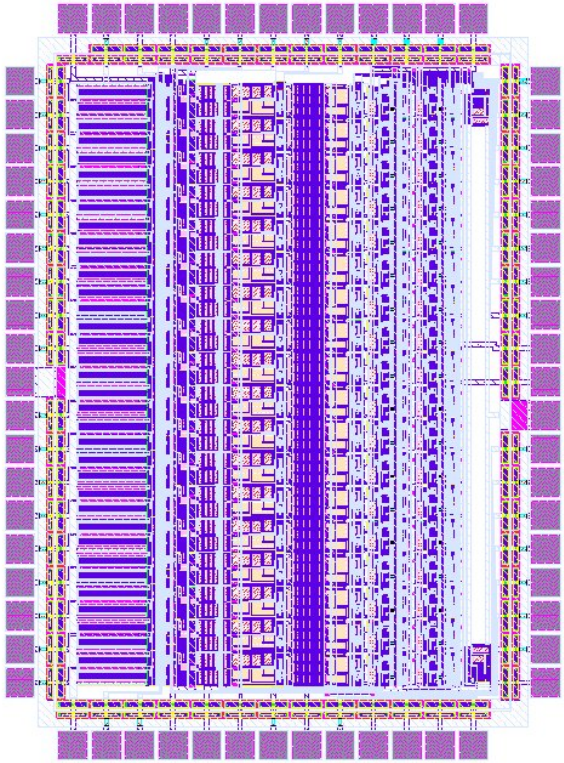


Next steps

HaRD_ROC (2006)

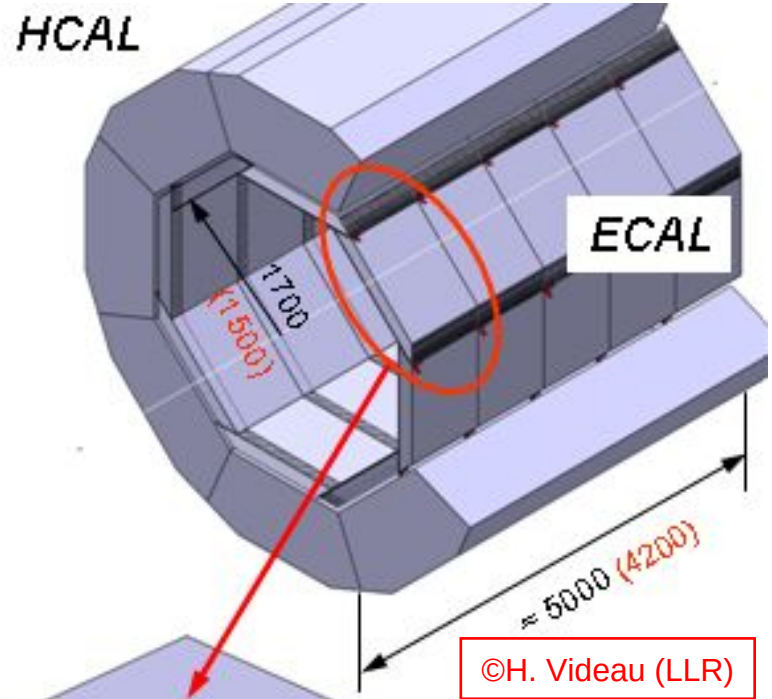


FLC_PHY3 (2003)



Technological prototype : "EUDET module"

- **Front-end ASICs embedded in detector**
  - Very high level of integration
  - Ultra-low power with pulsed mode
  - FLC_TECH1 ASIC prototype in 0.35 µm SiGe
- **All communications via edge**
  - 4,000 ch/slab, minimal room, access, power
  - small data volume (~ few 100 kbyte/s/slab)
- **« Stitchable motherboards »**



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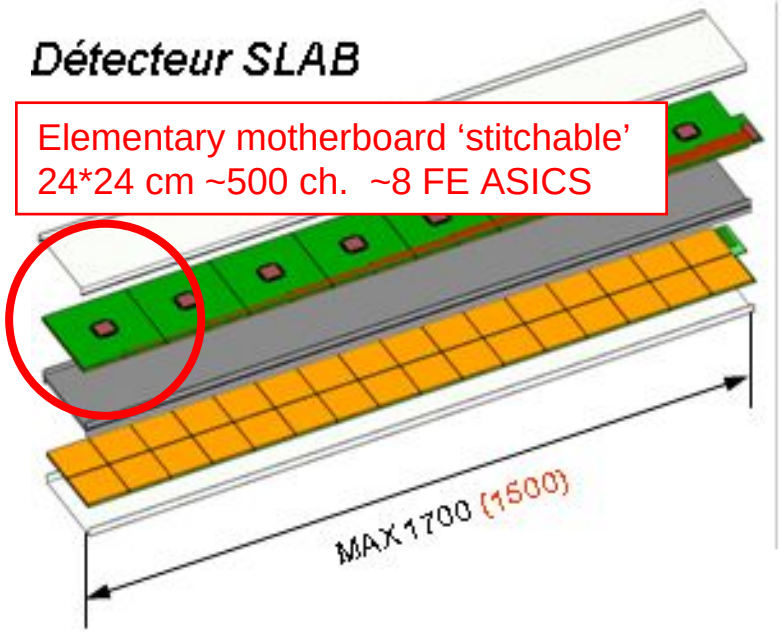
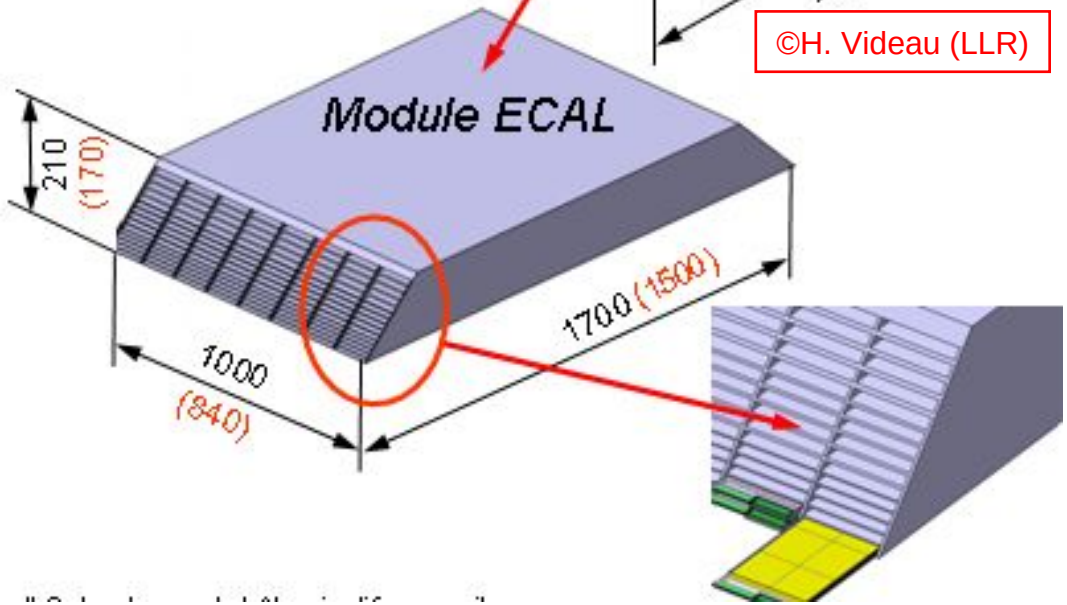
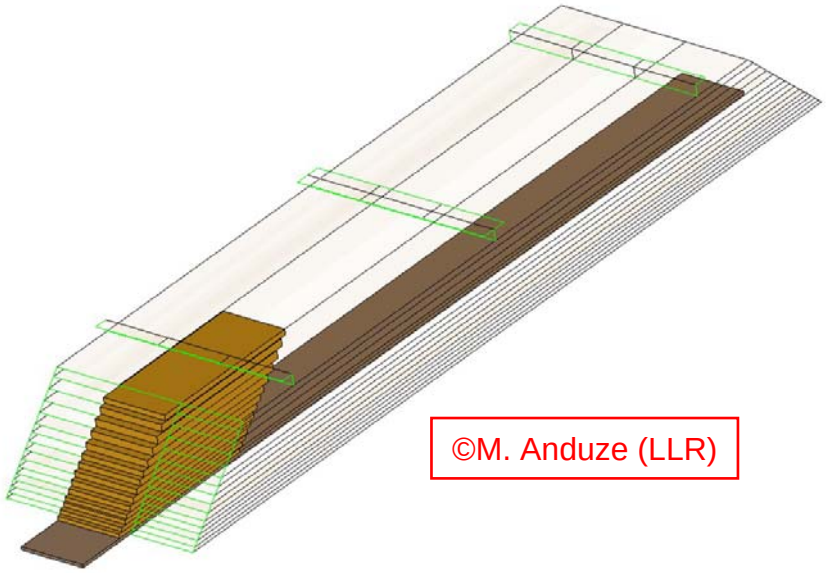




EUDET : ECAL module

- **Electromagnetic calorimeter**
  - Prototype of a (~ 1/6) module 0 : **one line & one column**
  - 150 cm long, 12 cm wide 30 layers
  - 1800 + 10800 channels
  - Test full scale mechanics + PCB
  - Can go in test beam
  - Test full integration + edge communications
- **Similar in #channels as physics prototype**



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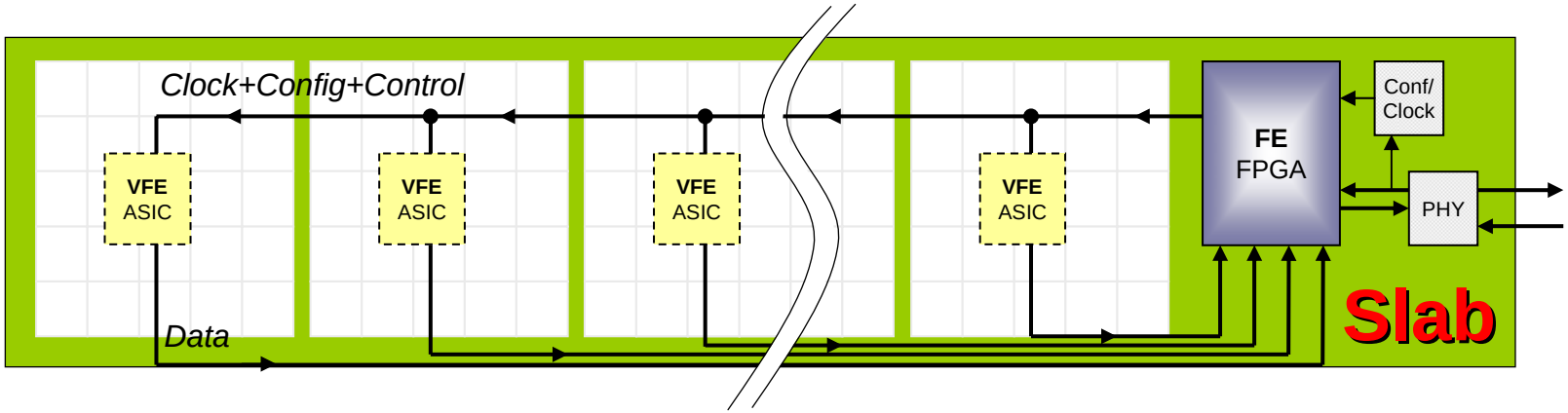
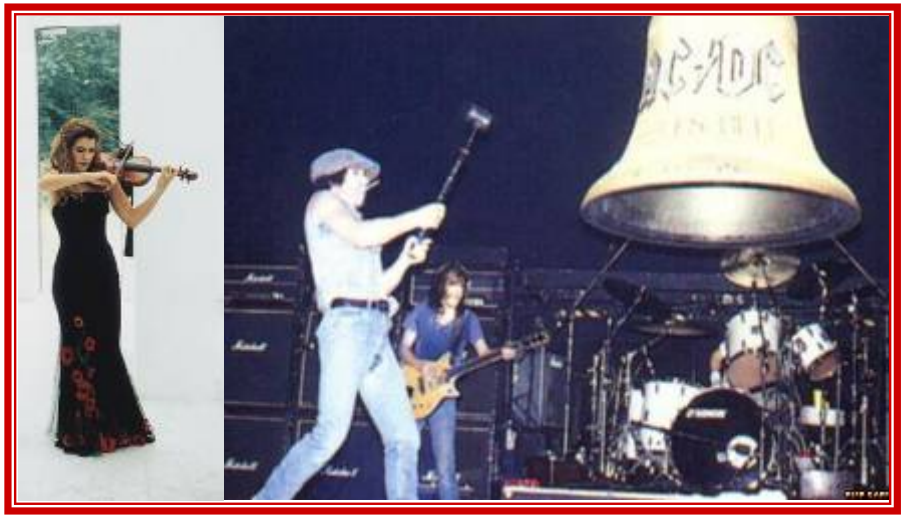


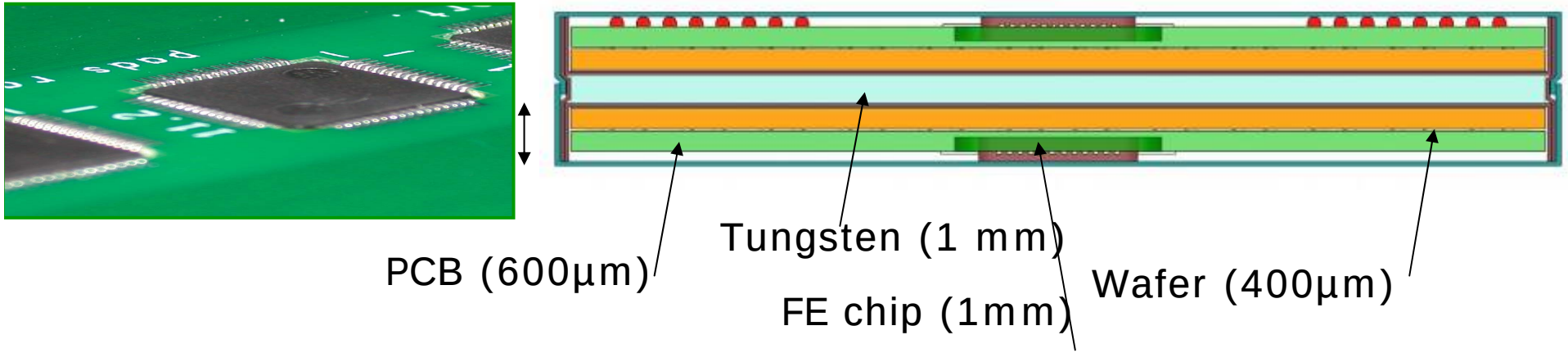
EUDET module FEE : main issues

- **Mixed signal issues**
  - Digital activity with sensistive analog front-end



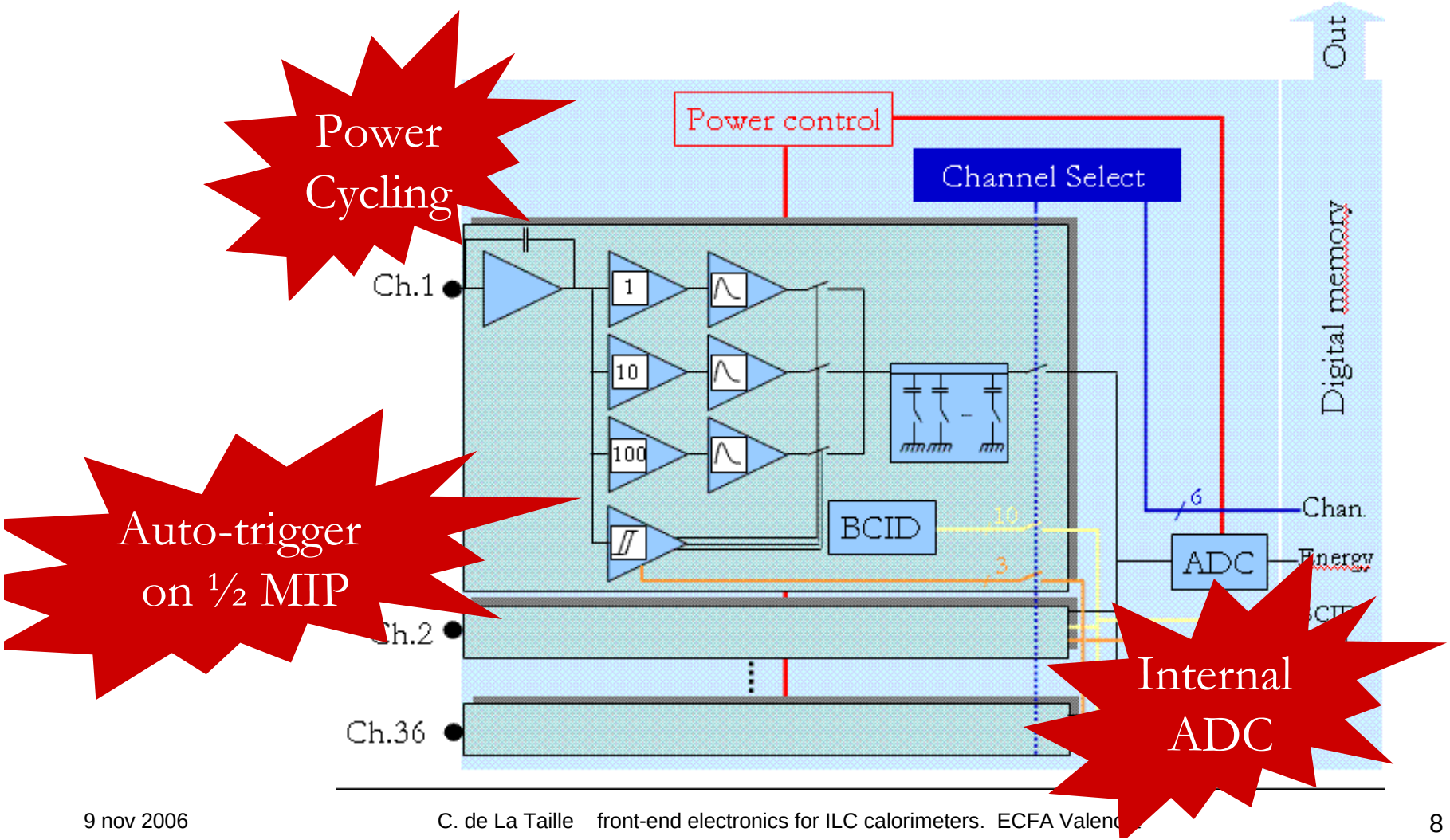
- **Pulsed power issues**
  - Electronics stability
  - Thermal effects
  - To be tested in beam a.s.a.p.

- **No external components**
  - Reduce PCB thickness to < 800µm
  - Internal supplies decoupling



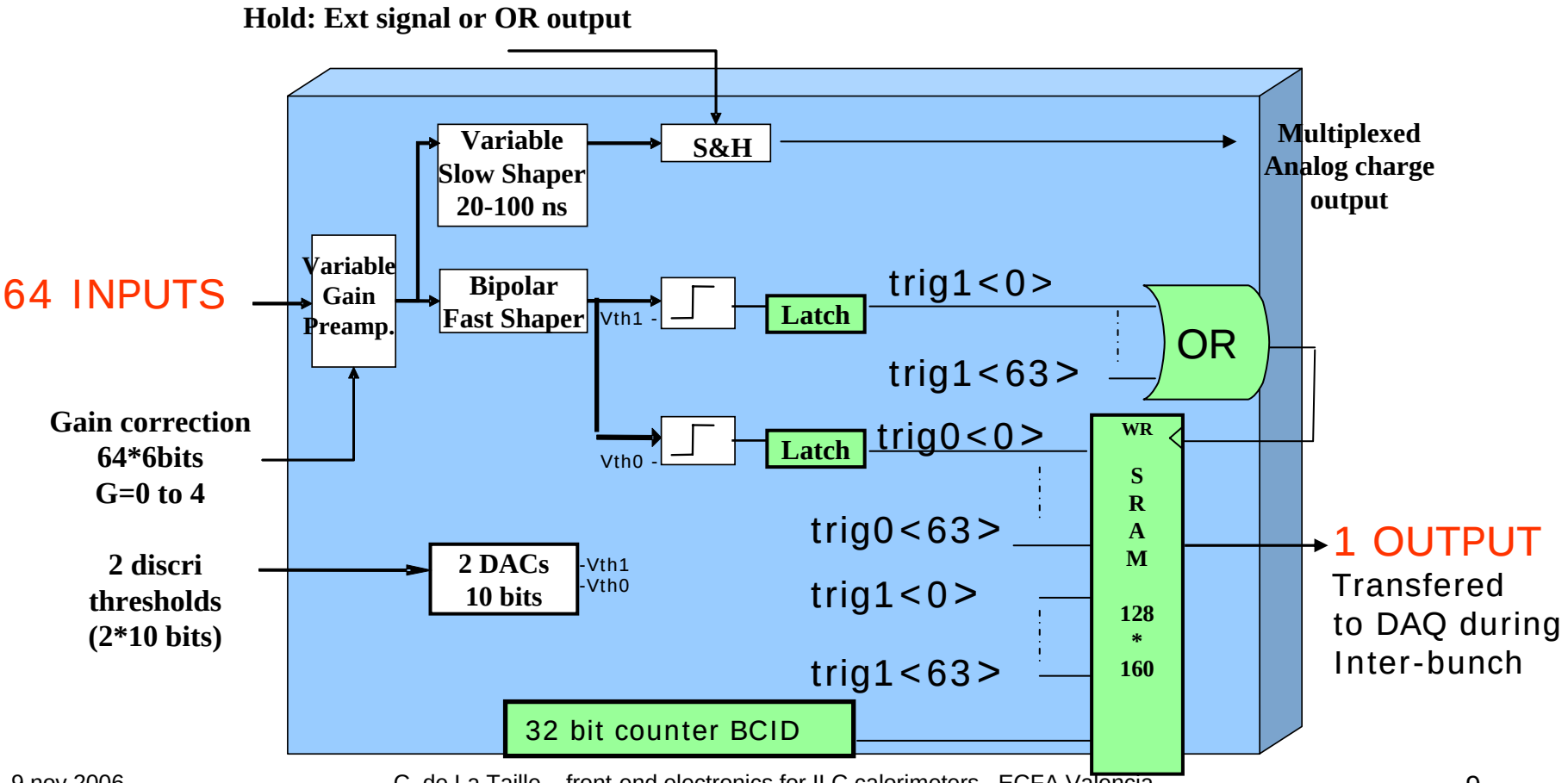
ECAL Front-End ASIC

- **Readout integration is the key element of compact detector**
  - Keep small Moliere radius for good shower separation
  - Many features have never been used before e.g. power cycling (ON 2ms OFF 200 ms)



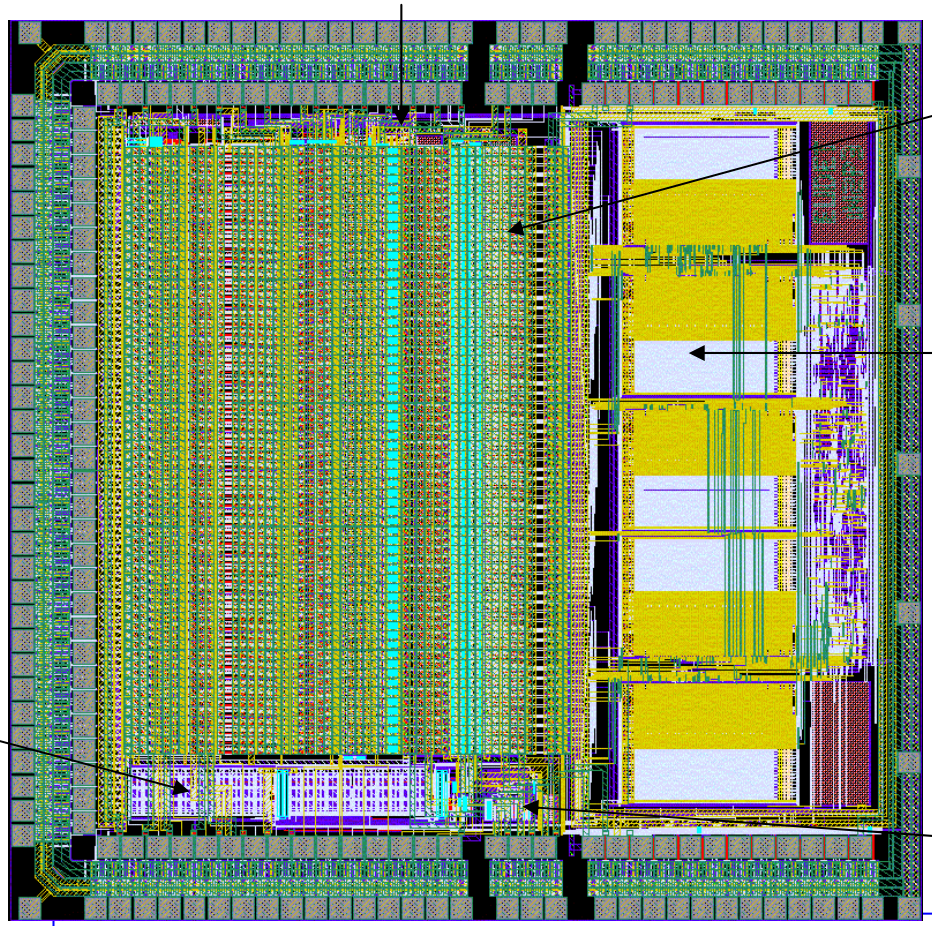
HaRDROC architecture

- Based on existing MAROC chip (ATLAS luminometry for MaPMT readout)
- Full power pulsing
- Digital memory: Data saved during bunch train. Only one serial output
- Store all channels and BCID for every hit. Depth = 128 bits

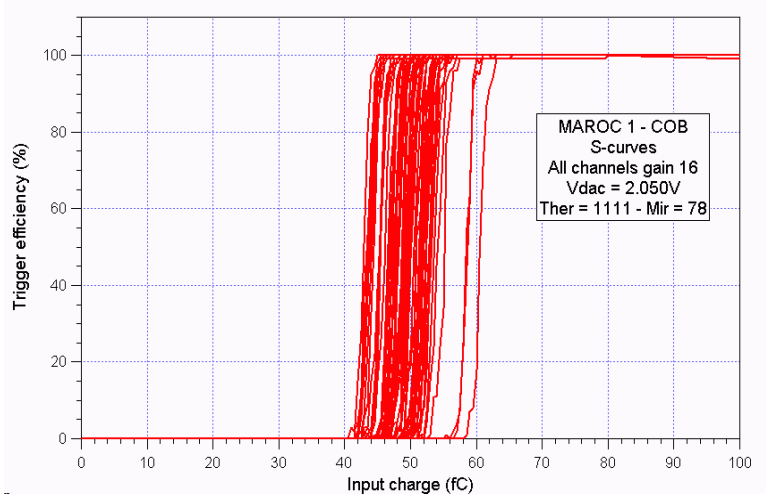


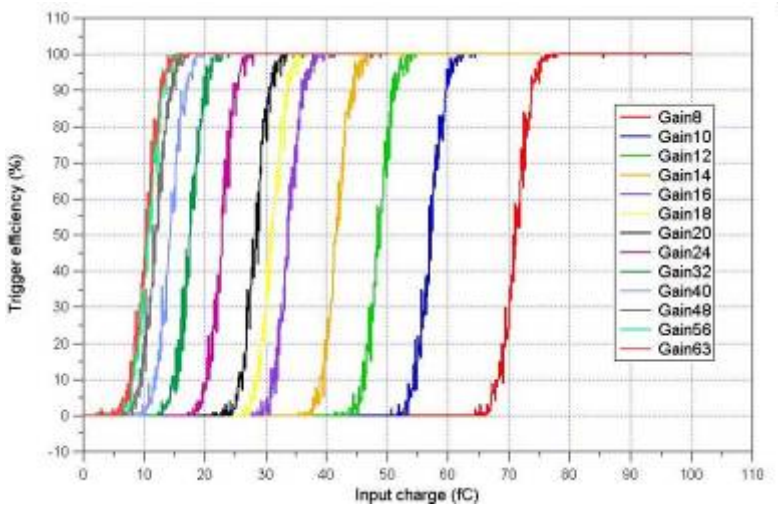
HaRDROC layout

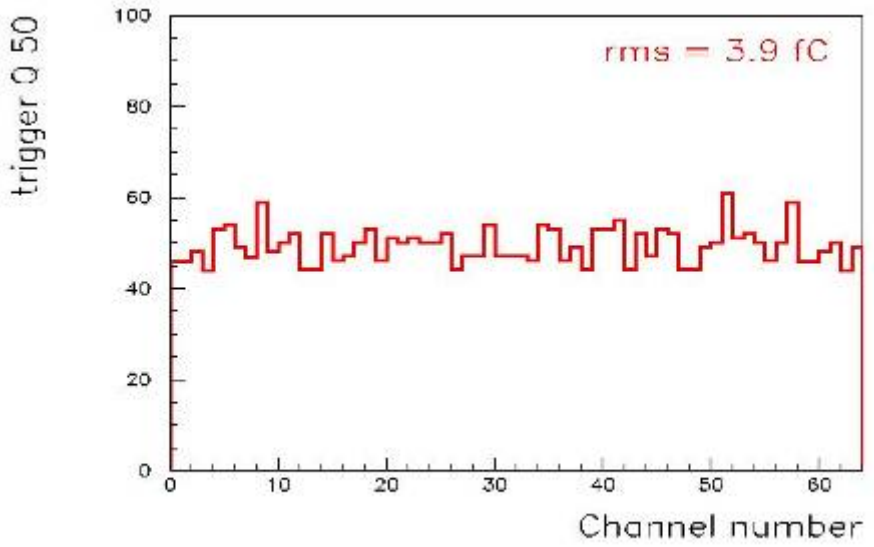
- Suited for RPCs, GEMS and Micromegas DHCALs.
- Quasi-binary readout (2 thresholds/channel)
- Fabricated in sept 06 in AMS SiGe 0.35µm technology (16mm²)

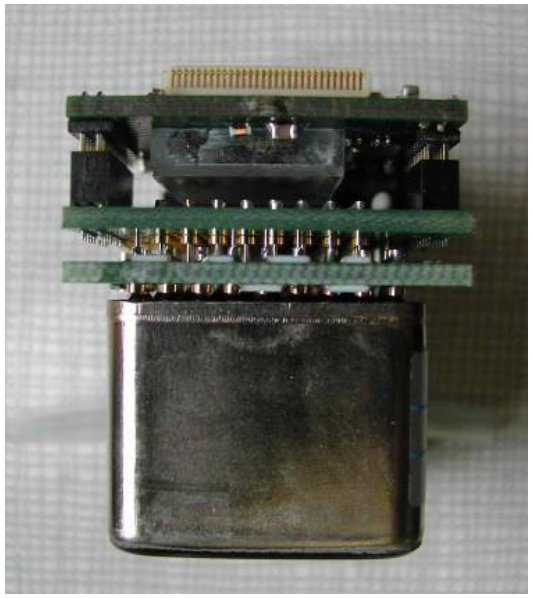


MAROC Efficiency curves





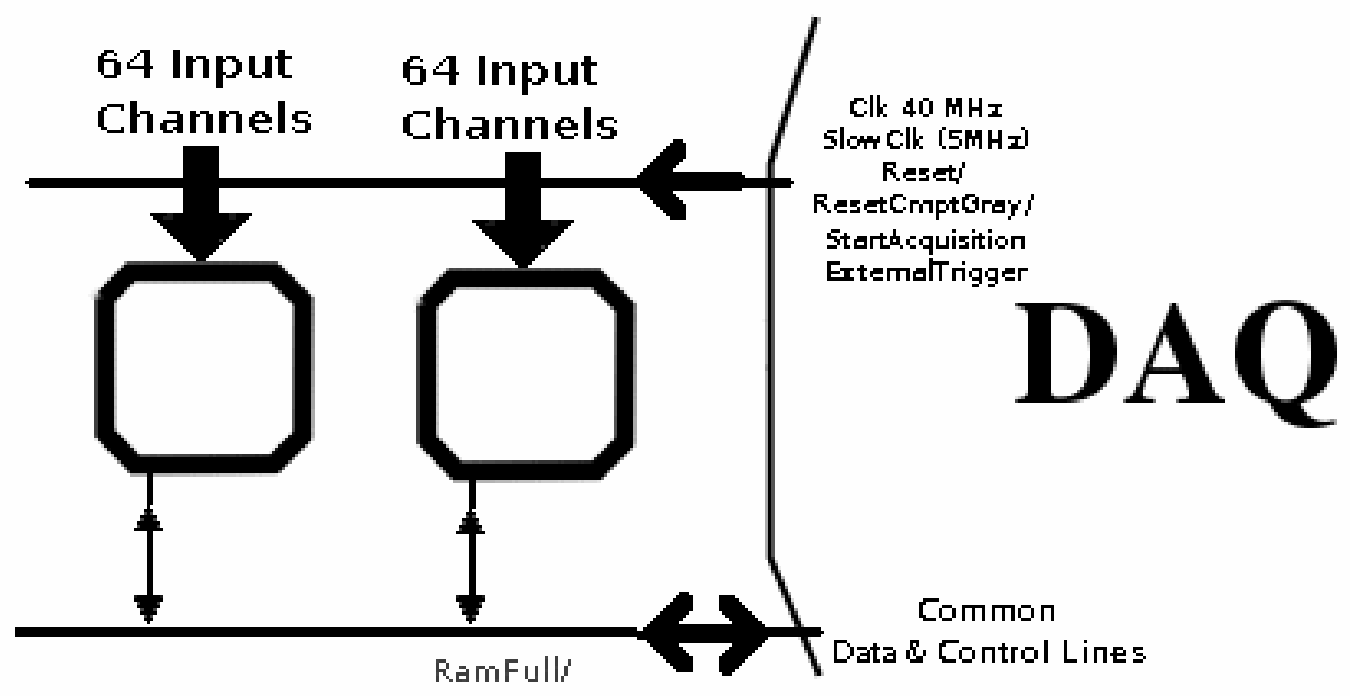




3*3 cm²

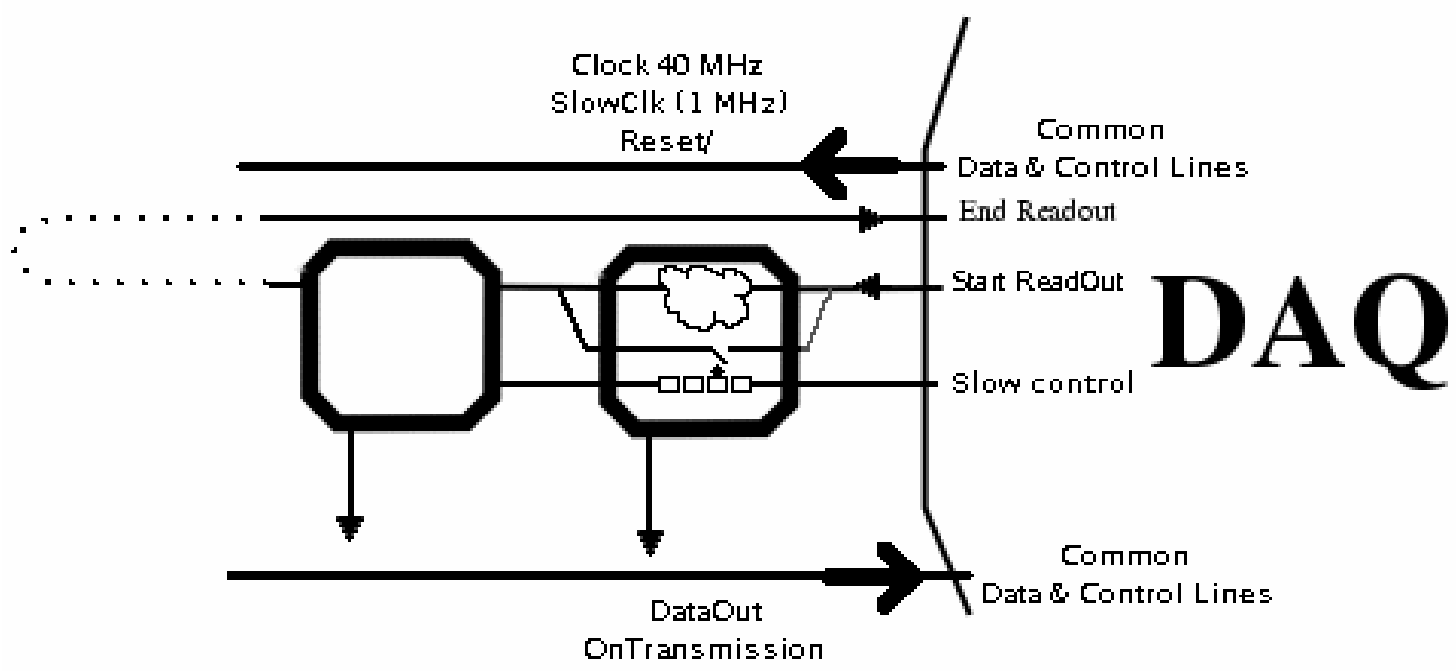
Acquisition mode

- **Store up to 128 events in RAM**
  - Sequential readout @ 100 MHz : 20k* 10 ns = 200 μs (read up to 1000 chips/inter bunch)
  - Data format : 128(depth)*[2bit*64ch+32bit(bcid)+8bit(Header] = 20kbits
- **Stop acquisition when ram_full signal asserted**
  - Common collector bus for ram_full signal



Readout mode

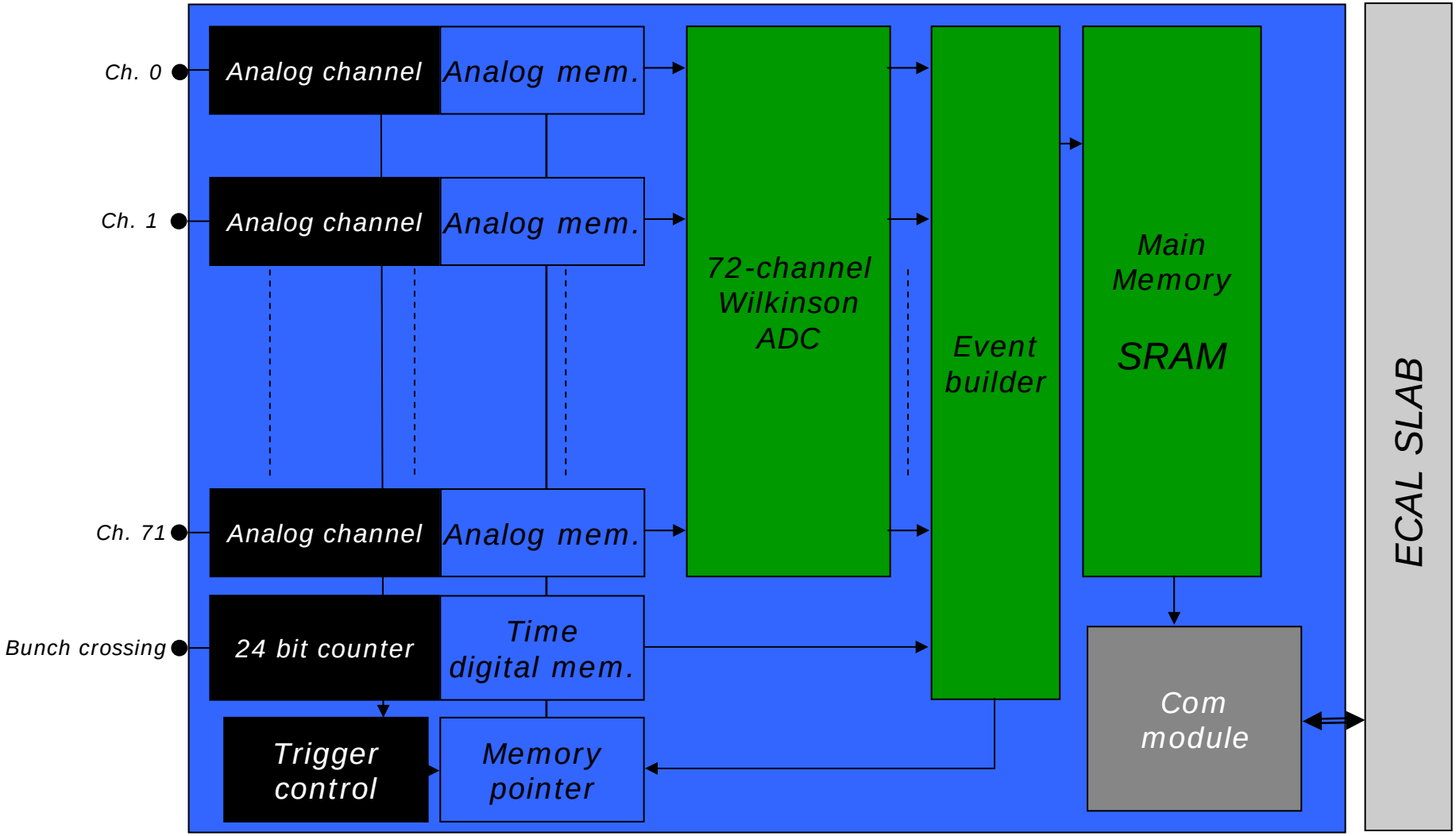
- **Token ring mechanism initiated by DAQ**
  - Possibility to bypass a chip by slow control
- **One data line activated by each chip sequentially**
  - Readout rate few MHz to minimize power dissipation
  - With 500 pF bus capacitance, power dissipation is ~10uW/chip
  - i=CdV/dt = 1 mA => 1 mW for up to 100 chips on bus
  - Readout time max (ram full) 10kbit * 1 μs = 10 ms/chip



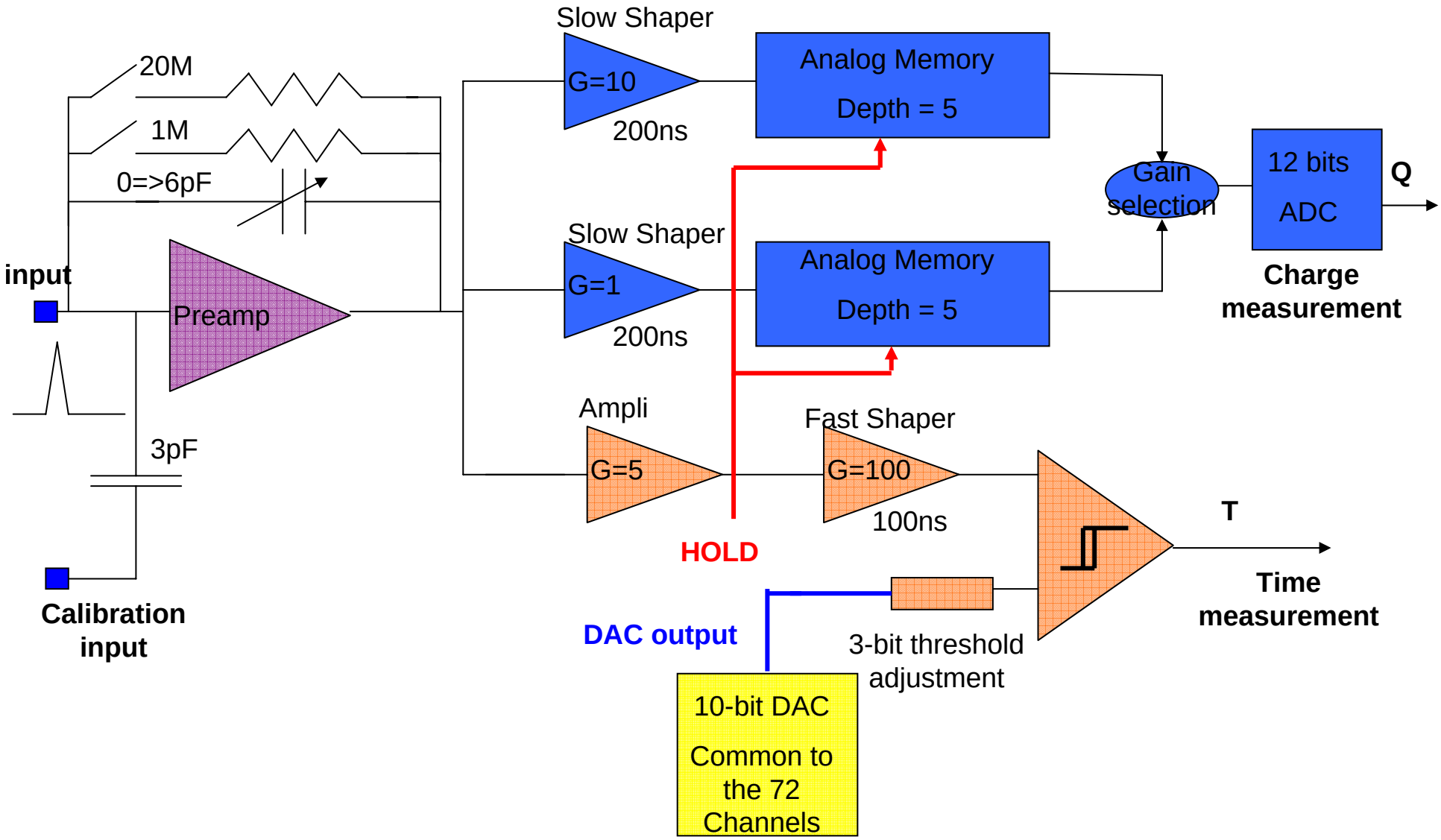
EUDET ECAL ASIC

- **72 channels**
  - Scales with the 4 factor reduction in pad size and is compatible with physics prototype
- **Detector DC coupling**
  - Prepares the case the on-detector MMIC HV capacitance is not affordable
  - Provides leakage current monitoring, up to 1 μA/Ch
- **Auto-trigger**
  - If one channel is hit during a bunch crossing, then the whole chip is recorded with a time tag (BCID)
  - The auto trigger activates the T&H
- **Analogue pipeline, ADC & digital registers**
  - 8-depth analog pipeline to store « in bunch » events
  - Wilkinson 12 bit 100MHz ADC
  - On chip storage, inter-bunch data outputting
- **Digital data output**
  - Daisy chained with redundancy : one output for 40 ASICs
  - Common architecture for ECAL and HCAL

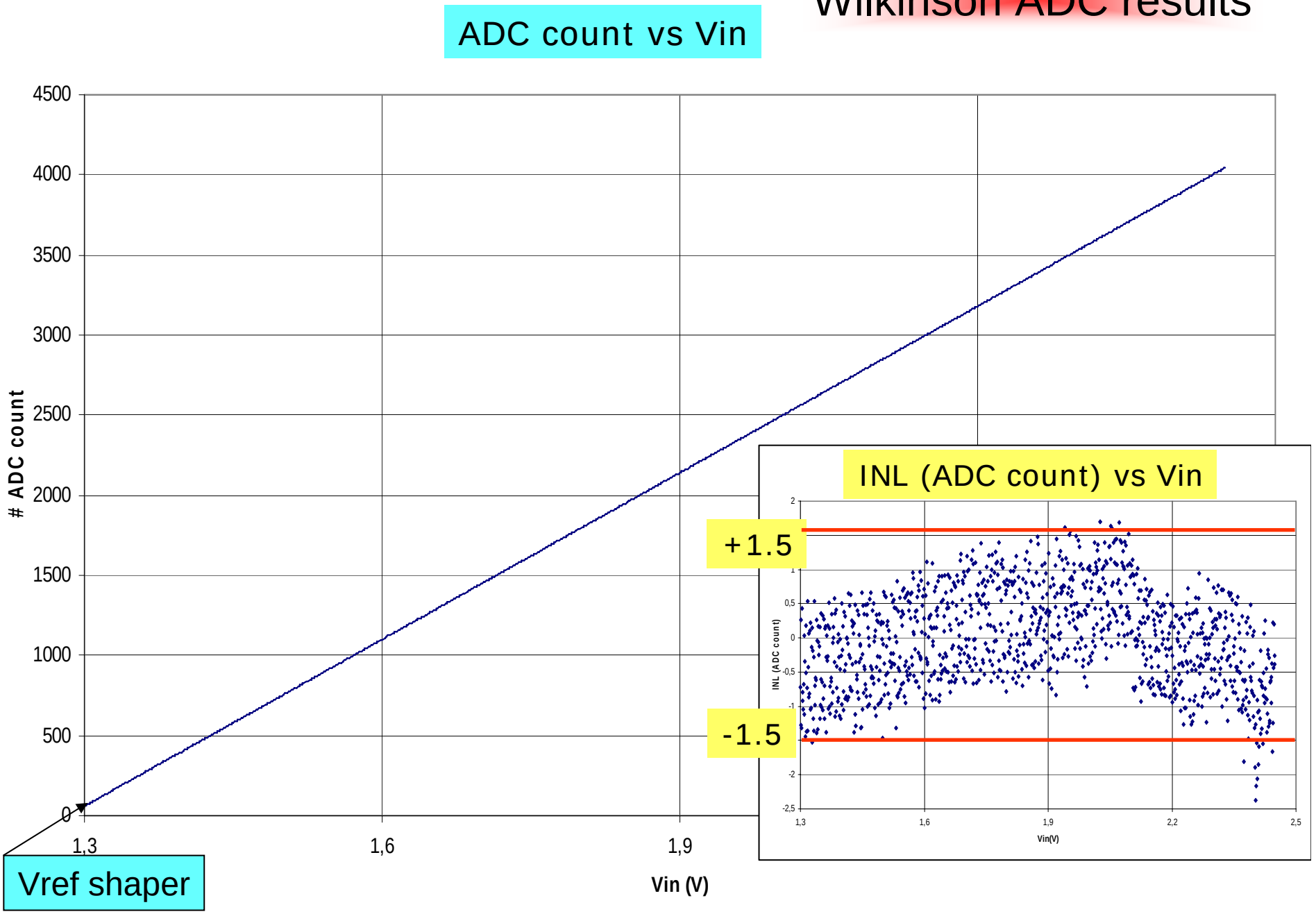
General block scheme



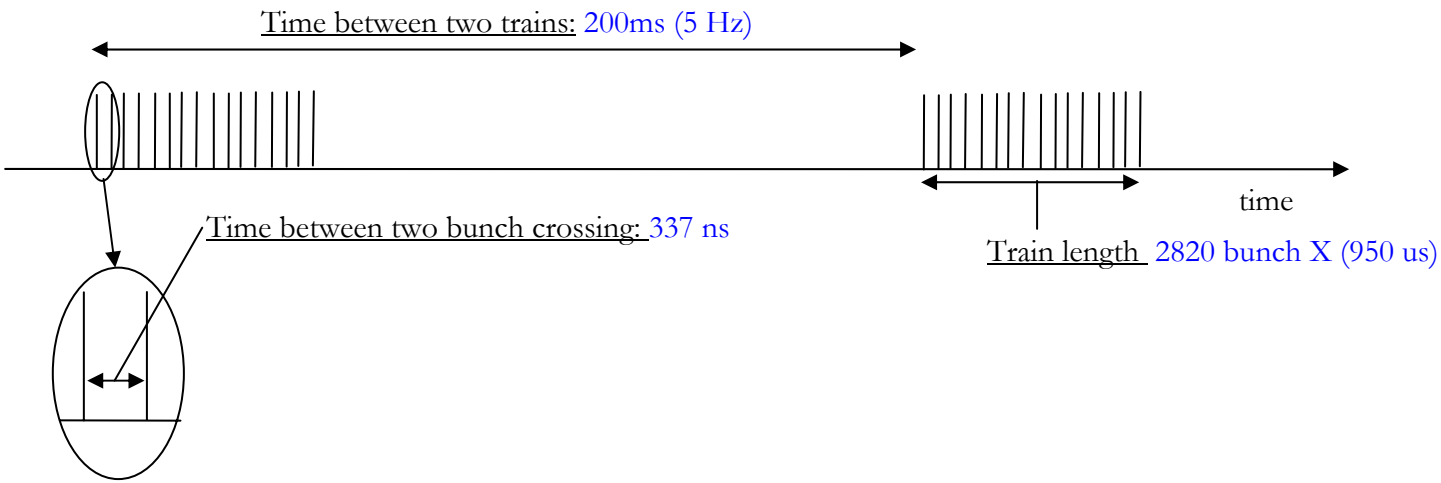
One channel

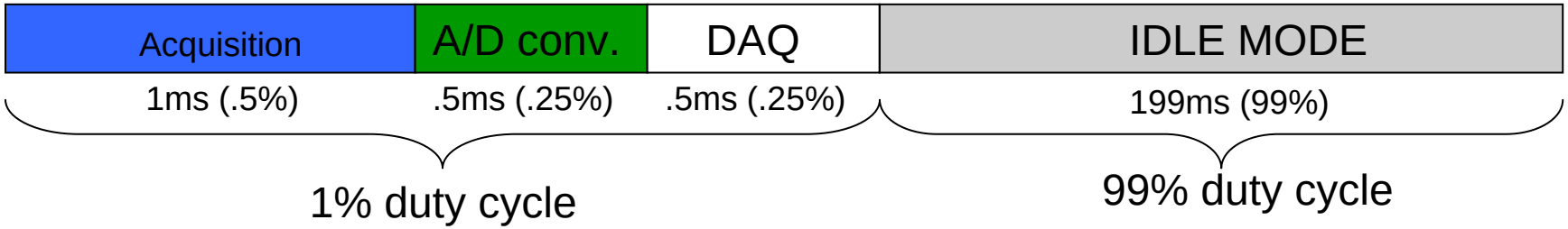

Slow Shaper
20M
G=10
Analog Memory
Depth = 5
200ns
1M
0=>6pF
Gain selection
12 bits
ADC
Q
Charge measurement
Slow Shaper
input
G=1
Analog Memory
Depth = 5
Preamp
200ns
Ampli
Fast Shaper
3pF
G=5
G=100
100ns
T
HOLD
Time measurement
DAC output
3-bit threshold adjustment
Calibration input
10-bit DAC
Common to the 72 Channels

Wilkinson ADC results

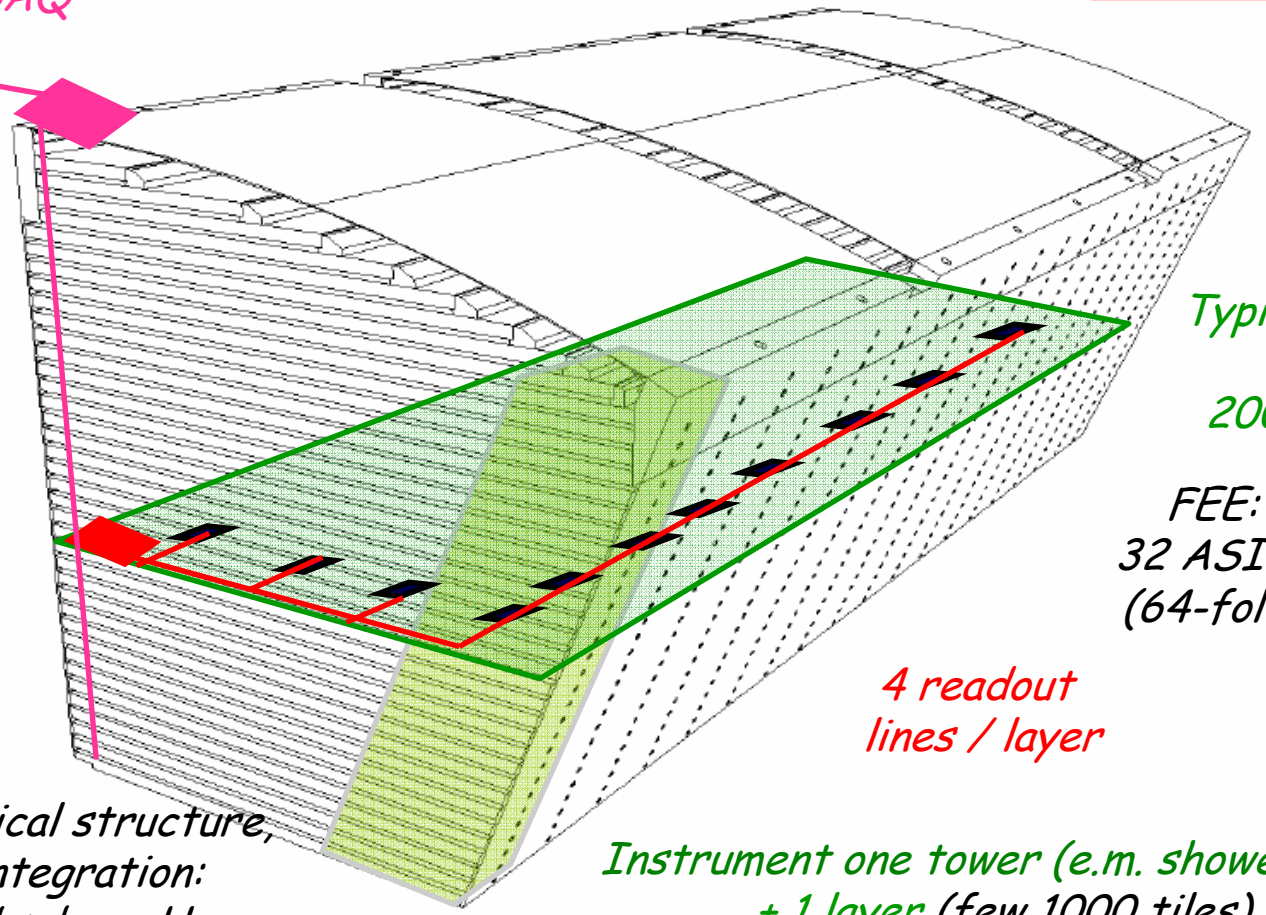


Time considerations



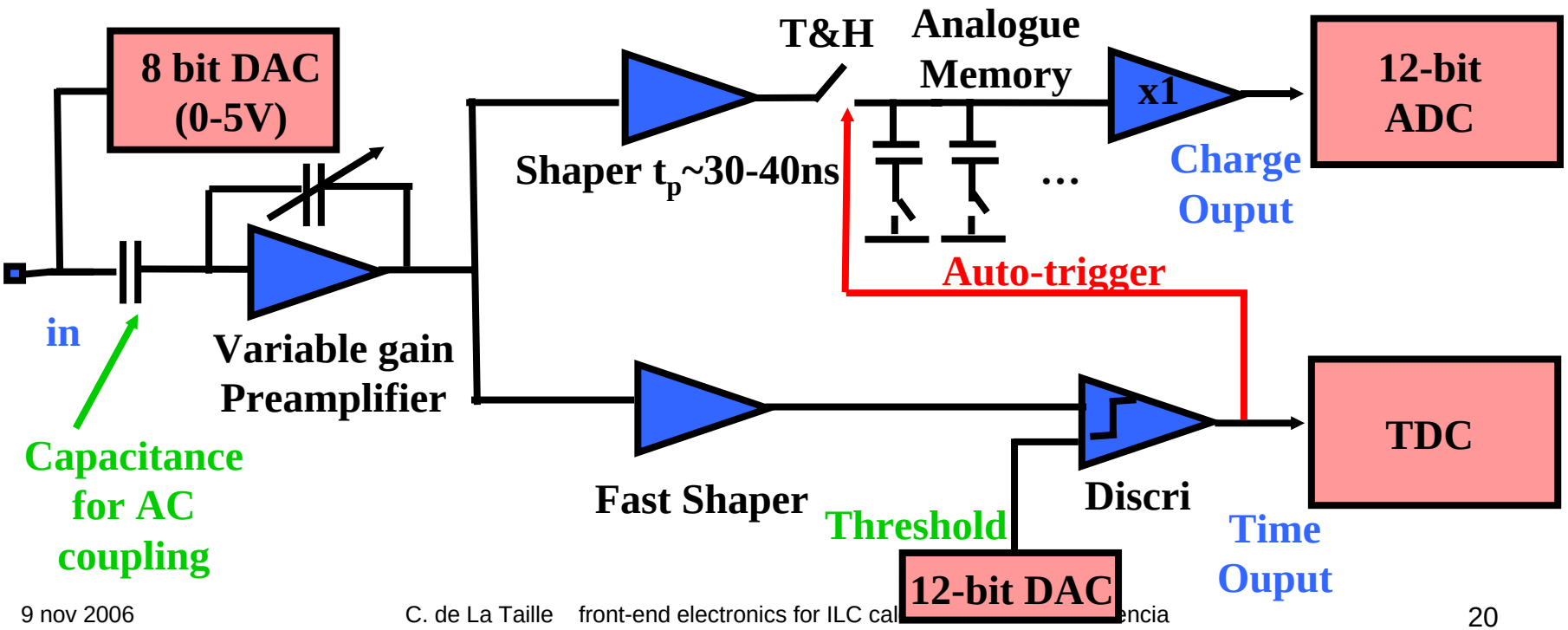


HCAL architecture



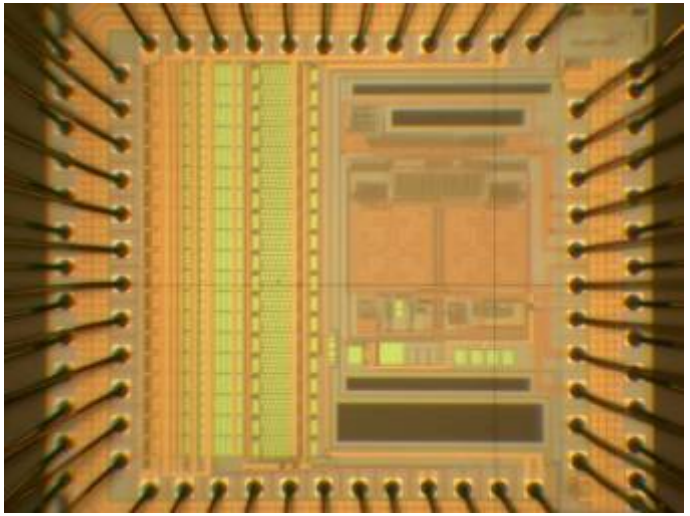
Prospective for A-HCAL SiPM Chip

- **Similar developments for AHCAL**
  - Chip fully dedicated to SiPMs developped after ECAL chip
  - Internal DAC for SiPM gain adjustment (5V range)
  - Auto-trigger (fast shaper + Discriminator)
  - Internal TDC, 1 ns step
  - Internal 12 bit ADC
  - Power pulsing



Conclusion

- **Several large dynamic range ASICs developped for CALICE physics prototypes**
  - ECAL W-Si calorimeter : FLC_PHY3 = 10^4 channels in beam, dynamic range 0.1-600 MIPS
  - AHCAL Tile-SiPM calorimeter : FLC_SiPM = 10^3 channels installed, beam in summer 06



- **Second generation calorimeter ASICS now being designed for EUDET module**
  - Power pulsing, Zero-suppress, Auto-trigger…
  - HArDROC for DHCAL Readout submitted sept 06
  - ECAL chip to be submitted in nov 06
  - AHCAL SiPM ASIC to be submitted in mar 07

- **System aspects to progress in parallel**
  - "Stitchable" PCBs for large module
  - Second generation DAQ
  - Power supplies ! Mechanics, reliability…
  - Low power low cost essential target