# Vertex Detector Sessions: Summary

- Brief Report on the Sessions on Tuesday and Wednesday
- News since LCWS in Bangalore

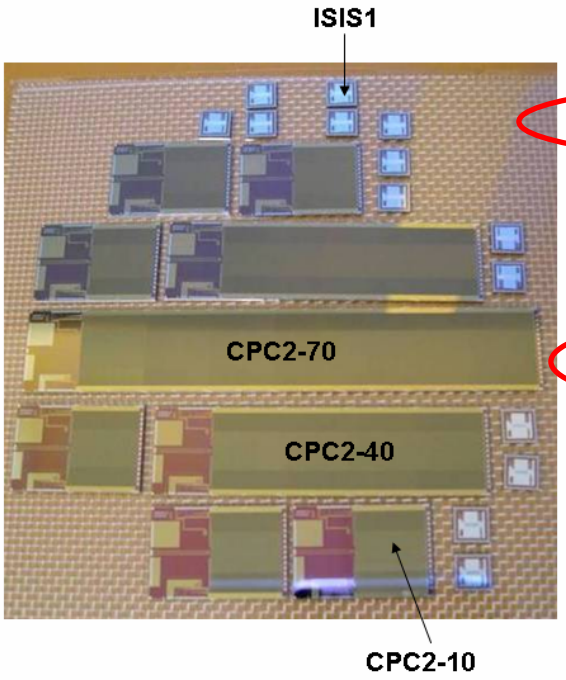
# Vertex Detector Sessions : Agenda

- TUESDAY NOVEMBER 7TH FROM 17:15 TO 18:30+ (ADEIT - 1.1 & 1.2 ) :
  - **LCFI collaboration report :** *K.Stefanov (RAL)*
  - **DEPFET report :** *L.Andricek (MPI/Munich)*
  - **CMOS sensor report of IN2P3 & DAPNIA :** *A.Besson (IPHC/Strasbourg)*
  - **Report on deep N-well sensor R&D :** *L.Ratti (INFN/Pavia)*

- WEDNESDAY NOVEMBER 8TH FROM 14:30 TO 16:00 (ADEIT - SALA GRADOS ) :
  - **Status of the EUDET/JRA-1 telescope :** *T.Haas (Univ.Hamburg & DESY)*
  - **Discussion ⟼ proposed topics :**
    - **Push-Pull option (contrib. from A.R.)**
    - **Detector Outline Document**
    - **A.O.B. (Vx Det. review in Autumn '07, ...)**

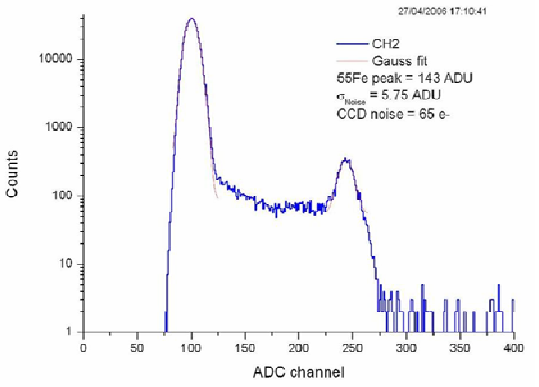
- LCFI: CP-CCDs / ISIS / mechanical support studies

## Second Generation CPCCD : CPC2




- 6 wafers with single level metal:
  - ❖ Four CPC2 wafers (3 × 100 Ω.cm/25 µm epi and one 1.5kΩ.cm/50 µm epi)
  - ❖ Two 100 Ω.cm wafers sent to VTT for bump bonding
- 2 CPC2 wafers with 2-level metal (busline-free CCD) delivered
  - ❖ Designed to reach 50 MHz operation
  - ❖ Important milestone for LCFI
- We have another 12 wafers to be processed after evaluation of the present variants

Yield from 4 CPC2 wafers: 71% for CPC2-10, 63% for CPC2-40, 25% for CPC2-70



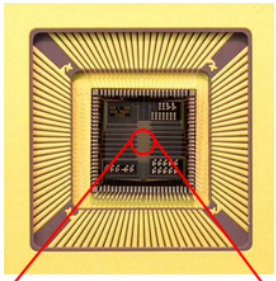

- **CPC2-10 (low speed version) works fine, here at 1 MHz clock**
- **$^{55}$Fe spectrum at -40 °C and 500 ms integration time**
- **Noise is a bit too high, external electronics is suspected**

Drivers ready, waiting for r/o chips

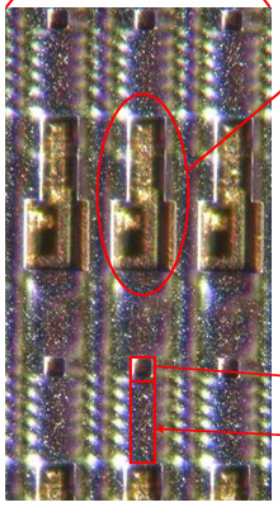
→ first preliminary test results may be possible earlier

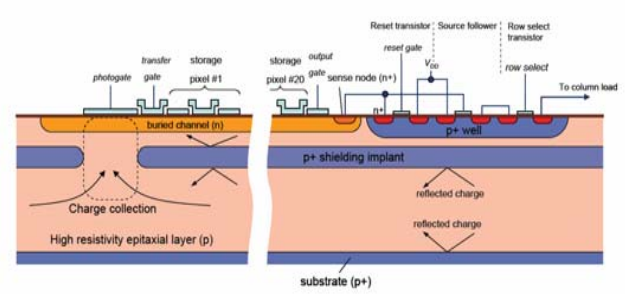
- LCFI: CP-CCDs / ISIS / mechanical support studies

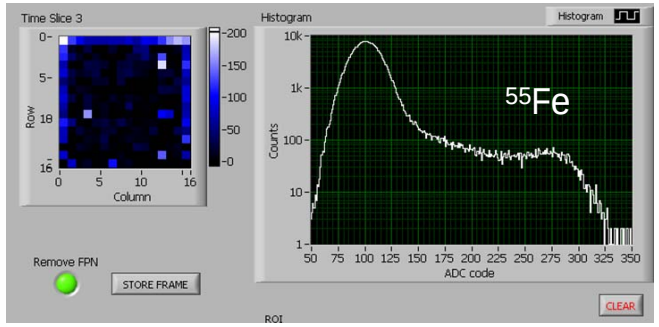
## The ISIS1 Cell



- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each;
- Cell pitch 40 µm × 160 µm, no edge logic (pure CCD process)
- Chip size ≈ 6.5 mm × 6.5 mm




proof of principle shown, continue with R&D

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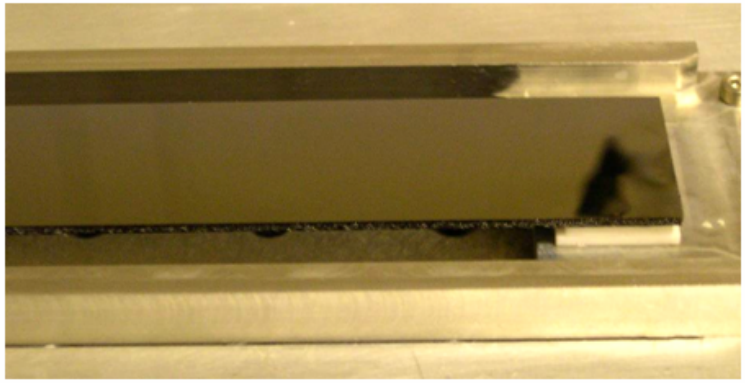
- LCFI: CP-CCDs / ISIS / mechanical support studies

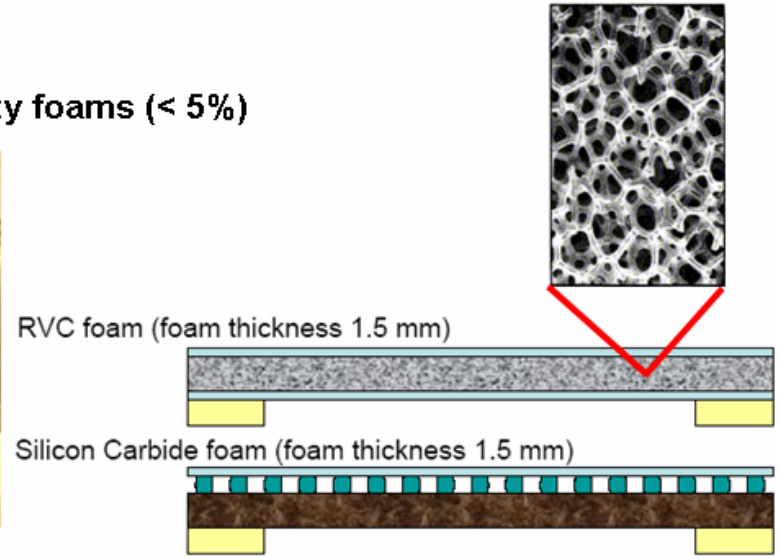
## Mechanical Support Studies

- RVC (Reticulated Vitreous Carbon) and silicon carbide are excellent thermal match to silicon
- Silicon-RVC foam sandwich (~ 3% density)
  - Foam (1.5mm thick), sandwiched between two 25 µm silicon pieces – required for rigidity
  - Achieves 0.09% $X_0$
- Silicon on SiC foam (~ 8% density)
  - Silicon (25 µm) on SiC foam (1.5mm);
  - Achieves 0.16% $X_0$
  - 0.09% $X_0$ possible with lower density foams (< 5%)

important work!
can be adopted by all technologies
MAPS, DEPFET etc.…



*Thanks to Erik Johnson, RAL*

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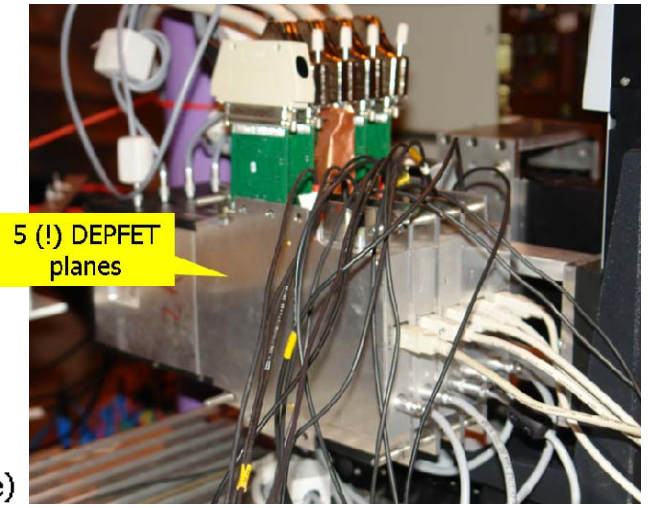
# DEPFET: Beam tests / Thinning results

## Test Beam(s)

:- 5 test beam periods have been done in the past
  3 x @ DESY (1-6 GeV $e^-$) – spatial resolution limited by multiple scattering to ~6µm for us.
  2 x @ CERN (120 GeV $\pi$) – August and October 2006. Analysis in progress...

:- Reference system is the 4 layer Silicon strip telescope (Bonn)
  (double sided strip detectors, 50 µm pitch)

:- Sensors are
  **450µm** thick (mip = 36ke)
  min. pixel size = **33x23.75µm²**
  various DEPFET variations have been studied




:- Speed:
  Clearing in 20ns
  Sample-clear-sample in CURO: ~ 240 ns (This would give a 4 MHz row rate)
  Non-zero suppressed readout (mostly)~ 800 µs/frame (128 rows) → ~ 6 µs/row

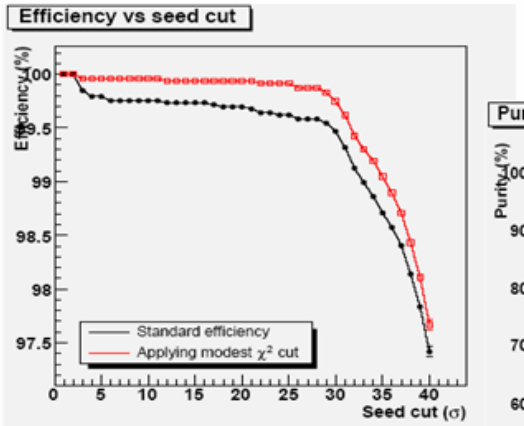
In the recent CERN test beam, a **beam telescope of 5 DEPFET planes** has been successfully operated!



ECFA Workshop, Valencia, November 2006 Ladislav Andricek, MPI für Physik, HLL

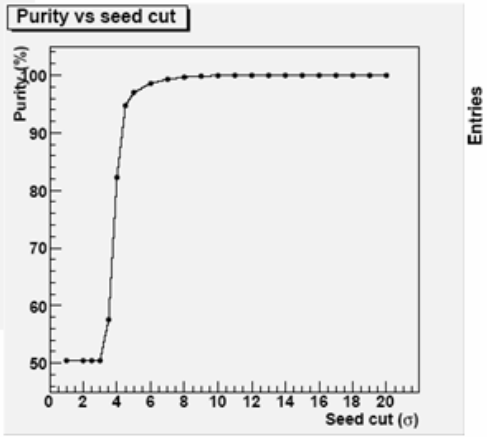
# DEPFET: Beam tests / Thinning results

## Efficiency & Position resolution

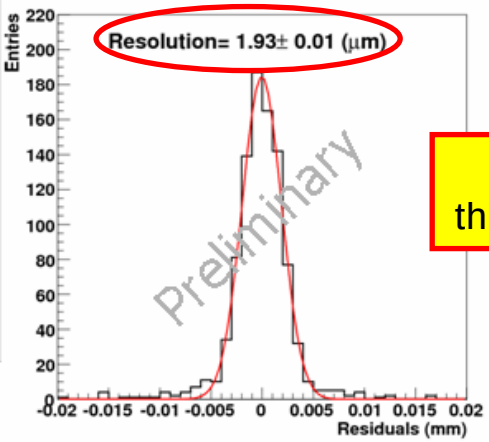



$$\text{Efficiency} = \frac{\text{Number of tracks with cluster}}{\text{Total number of tracks}}$$

$$\text{Purity} = \frac{\text{Number of clusters with tracks}}{\text{Total number of clusters}}$$




CERN Test Beam




450 μm thick sensor

(Jaap Velthuis)

For 5 σ seed cut

- Efficiency ≈ 99.96%
- Purity ≈ 99.6 %

First preliminary result from CERN test beam,
120 GeV π, 33x23.75 μm² pixels
**position resolution ≈ 2 μm**



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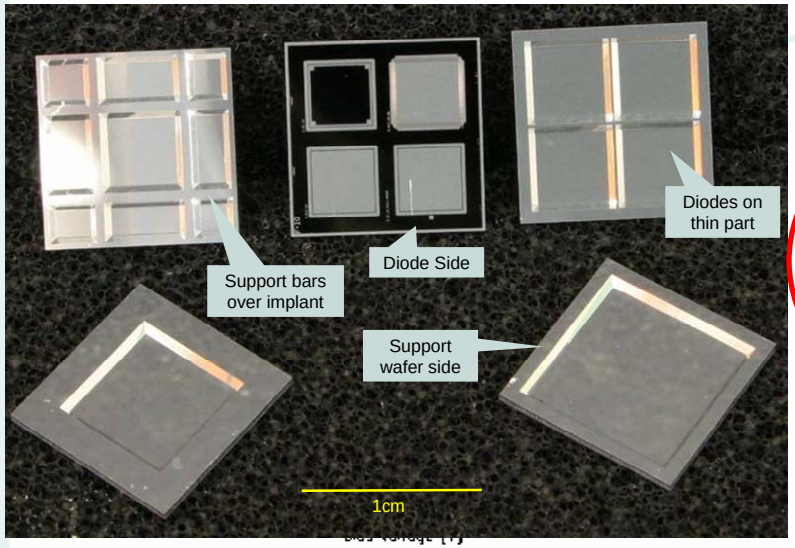
# DEPFET: Beam tests / Thinning results

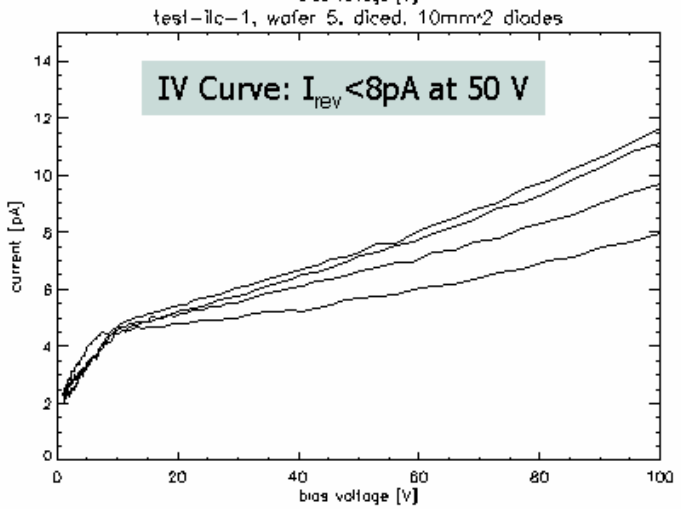
## PiN Diodes on thin Silicon

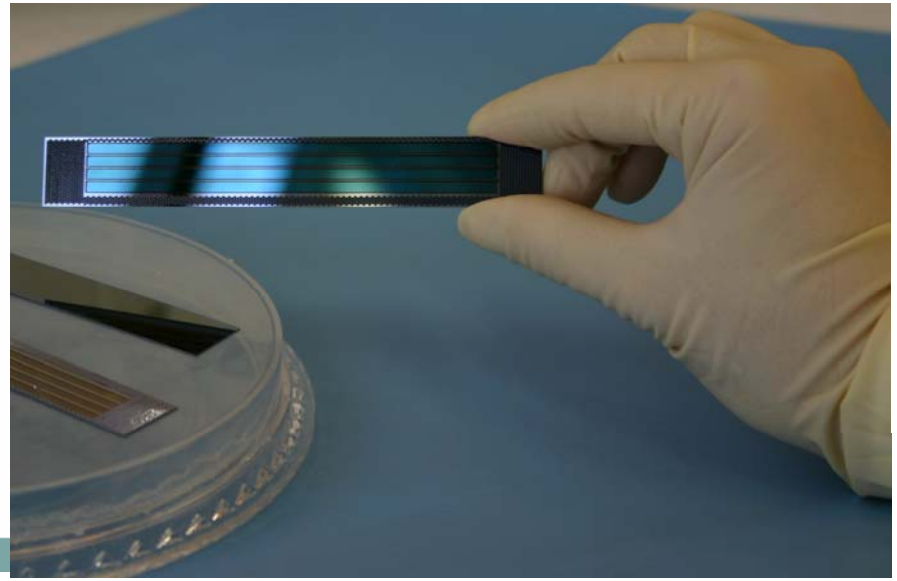



mpi halbleiterlabor

Thin diodes have **excellent** leakage currents.

**Processing** of the SOI wafers and removal of handle wafer **does not degrade devices!**



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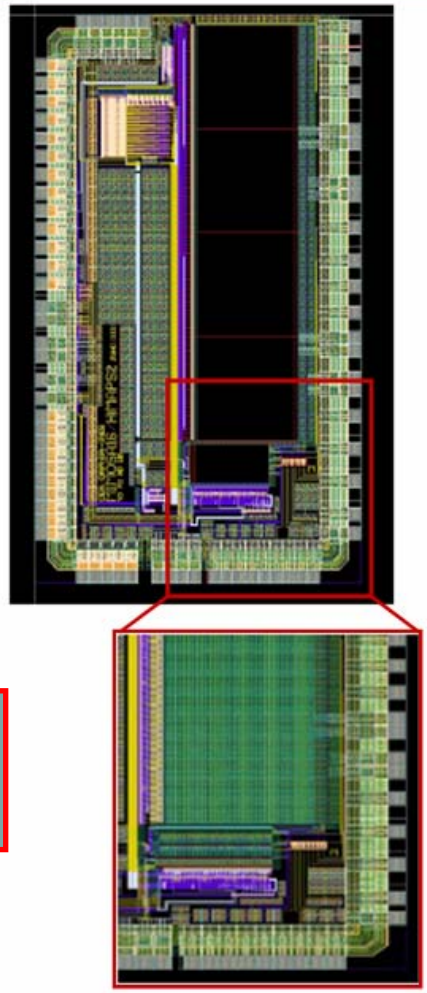
- CMOS Sensors: Mimosa16 and ADC development program

August Besson informed us about the latest Mimosa and ADC run at AMS

## High Read-Out Speed Architecture: MIMOSA-16

- MIMOSA-16 design features :
  - AMS-0.35 OPTO translation of MIMOSA-8
    - 11–16 µm epitaxy instead of ~ 7 µm
  - 32 // columns of 128 pixels (pitch: 25 µm)
  - On-pixel CDS (repeated at end of each column)
  - Discriminator at end of each column



just returned from foundry!

reticle contains various other sensors for

-: STAR
-: EUDET telescope

and small Flash ADCs

The operation of CMOS Sensors in real (less demanding) experiments is within reach.

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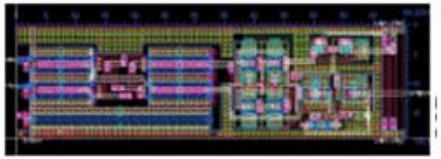
- CMOS Sensors: Mimosa16 and ADC development program

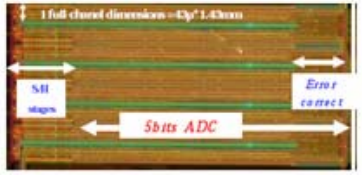
## Progress on ADC developments and plans

- Several different ADC architectures under development
  - LPCC (Clermont) : flash 4+1.5-bit ADC
    - 1st proto tested, 2nd proto back from foundry
  - LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5-bit ADC
    - 1st proto tested, 2nd proto under test
  - DAPNIA (Saclay) : Ampli + Suc.App.R (4- and) 5-bit ADC
    - 1st proto under test
  - IPHC (Strasbourg) : SAR 4-bit and Wilkinson 5-bit ADCs:
    - 1st proto submitted end October 06

LPCC, new comparator



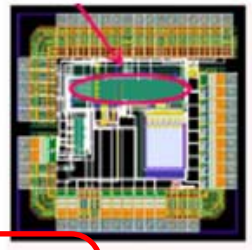
LPSC, 5-bit ADC




- Present outcome of development :
  - Typical differences between architectures :
    - ~ factor 2 in power & speed
  - Observed pbs: loss of 1–2 bits

  (e.g. due to offset dispersion between columns)
    - solutions under study
    - ⇨ include enhanced signal amplification before ADC

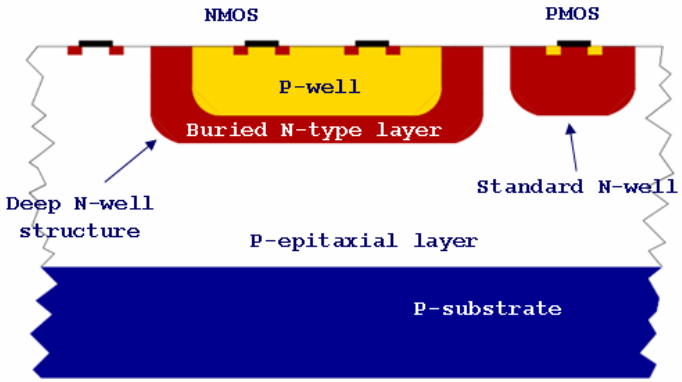
DAPNIA, 6 ADC in //



- Next steps :
  - Final ADC designs expected to come out in 2007
  - Submission of 1st col. // pixel array proto equipped with ADCs & ∅ end 2007

- Deep N-Well MAPS: new concept

## Deep N-well MAPS concept




- In triple-well CMOS processes a deep N-well is used to isolate N-channel MOSFETs from substrate noise
- Such features were exploited in the development of **deep N-well (DNW) MAPS** devices

- A DNW is used to collect the charge released in the epitaxial layer
- A readout channel for capacitive detectors is used for Q-V conversion → gain decoupled from electrode capacitance
- NMOS devices of the analog section are built in the deep N-well
- Using a large detector area, PMOS devices may be included in the front-end design → charge collection inefficiency depending on the ratio of the DNW area to the area of all the N-wells (deep and standard)

ILC Workshop 2006 – Valencia, 6-10 November 2006 3

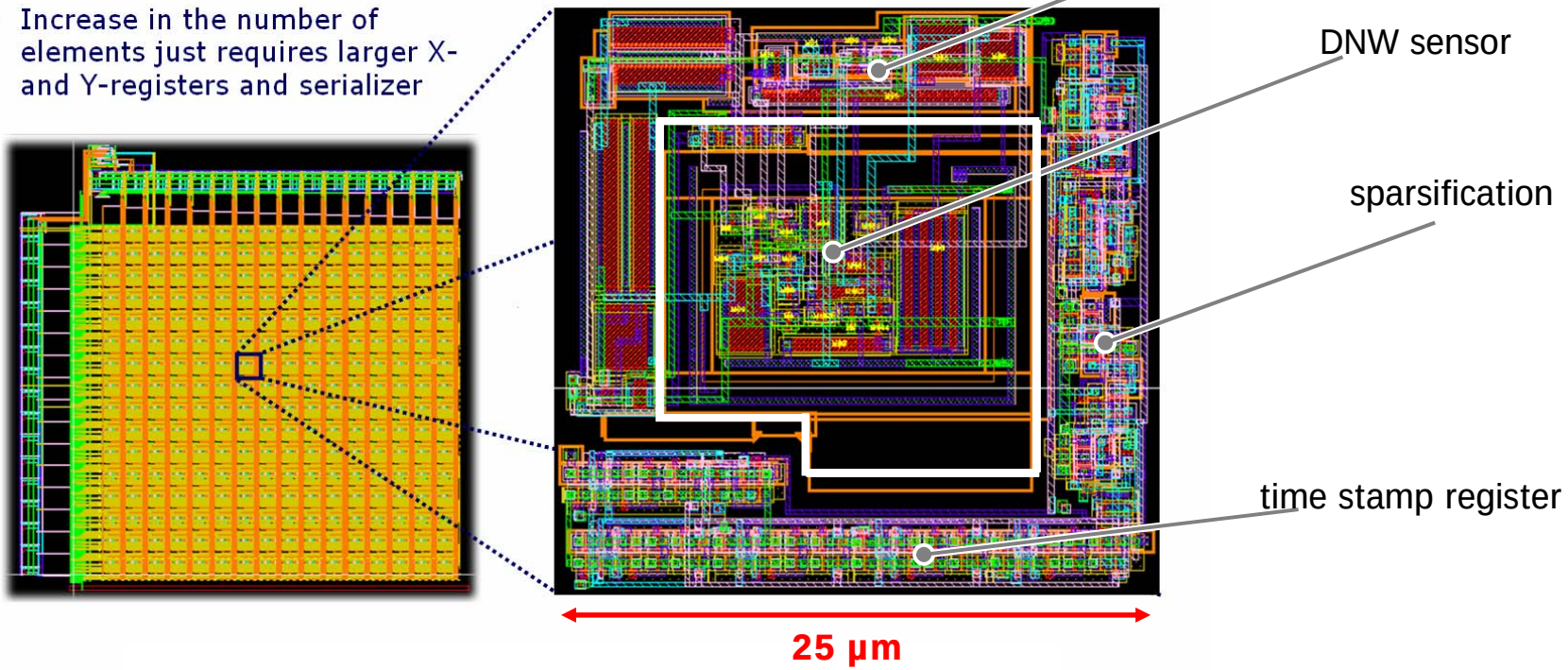
- An ambitious goal is to design MAPS with similar readout functionalities as in hybrid pixels (sparsification, time stamping, e.g. FPIX)

- Deep N-Well MAPS: new concept

## ILC DNW MAPS demonstrator

ILC-València 06

- A 16x16 MAPS demonstrator chip is being designed in the 130 nm bulk CMOS technology by STM
  - Increase in the number of elements just requires larger X- and Y-registers and serializer

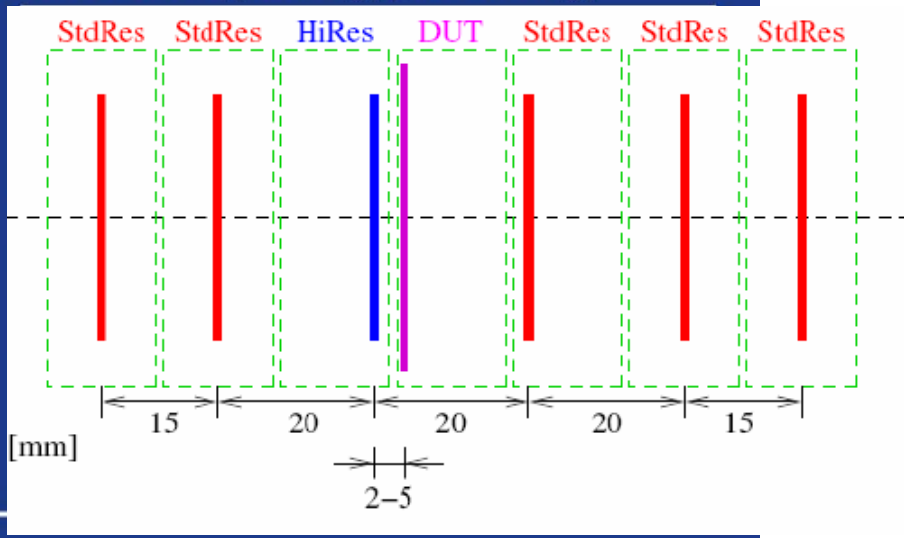



- Simulations show good noise and threshold dispersion performances at a power dissipation close to the ILC vertex specifications

- EUDET JRA1 Program

# Testbeam Infrastructure (JRA1)

- Provide a large bore high field magnet
- Provide beam telescope with:
  - Very high precision ( < 3µm precision even at lower energies)
  - High readout speed ( frame rate > 1 kHz)
  - Easy to use (well defined/described interfaces)
  - Wide range of conditions for devices under test (cooling, positioning, magnetic field
- Major uses
  - Pixel sensors
  - Large volume tracking devices
- Initial setup @ DESY
  - < 6GeV/c electrons
- Transportable
  - Hadron beams at FNAL or SLAC




7 November 2006

*Tobias Haas: Pixel Telescope*

- ...since Bangalore

## 1st ILC Vertex Workshop at Ringberg Castle, May 28 to May 31, 2006

- Two and a half days of presentations and discussions.....

**Sunday evening**

Introductory talk by Wolfgang Hollik
"Precision Physics at the ILC "

**Monday**

:- Physics and Simulation tools
:- VTX Detector in the various concepts
:- Integration and ladder design
:- Background at the VTX

**Tuesday**

:- Detailed presentations of the various proposed technologies and concepts
:- Common Efforts
:- Discussion

**Wednesday**

:- "White Paper" Discussion
:- Workshop Summary

Wednesday afternoon: Tour through the MPI Semiconductor Laboratory

09.11.2006 Ladislav Andricek, MPI für Physik, HLL

- ...since Bangalore

1st ILC Vertex Workshop at Ringberg Castle, May 28 to May 31, 2006

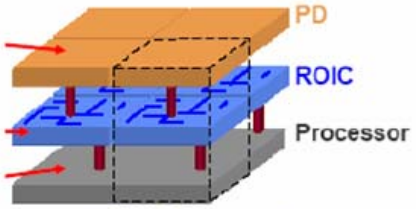
about 50 participants from all regions...

- ...since Bangalore

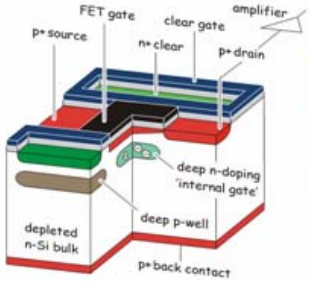
# Technologies

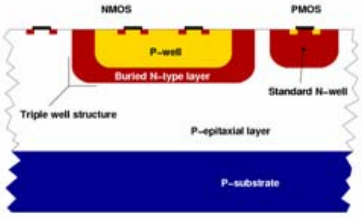
**Many different technologies**

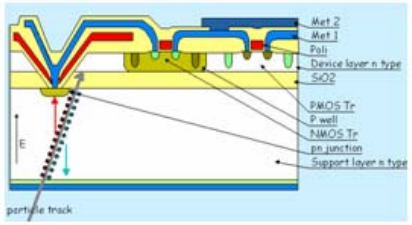
**CP-CCD**
**DEPFET**
**FAPS**
**FP-CCD**
**MAPS**
**MAPS (tripple well)**
**SOI**
**3D**

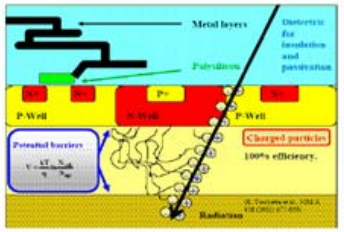


3D Pixel Layout[9]




**Excellent reviews by Konstantin Stefanov, Joel Goldstein, Rainer Richter, Hans Krueger, Marc Winter, Devis Contarato, Valerio Re, Tadashi Nagamine, Ray Yarema, Wojciech Kucewicz**

May 31, 2006 H-G Moser MPI fuer Physik/HLL

http://www.hll.mpg.de/~lca/ringberg

# ...since Bangalore

ILC Vertex Tracker Status Report

**The ILC Vertex Tracker**

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T. Greenshaw
*Department of Physics, University of Liverpool, Liverpool, UK*

**1. INTRODUCTION**

The vertex detector (VXD) is one of the most challenging elements of the detectors for the ILC. It is therefore not surprising that many technologies are under consideration and that the relevant R&D is being pursued in laboratories across the world. However, there will be at most two detector systems at ILC. How will the community choose the most appropriate technologies for use at the ILC and identify the most promising routes for future upgrades to the vertex detectors? The free and frank parallel sessions that are held at many regional workshops are one way of advancing our understanding of the various vertex detector concepts and of the progress being made towards their realisation, as are the vertex-specific world-wide teleconferences organised by the community. Recently, members of the community met at the ILC Vertex Detector Workshop at the Ringberg castle in Germany. From this meeting, and from discussions at the Snowmass ILC workshop last year, the idea developed that the community prepare a report on the status of R&D for the ILC vertex detector. The main purpose of this report will be to provide a level of technical information on the vertex detector that is deeper than has ever before been published in one document, in order to inform not only the ILC vertex detector groups, but the broader ILC physics community and the ILC detector concept groups about the progress in the field. The aim will be to summarise the current status and perceived future challenges, for all the vertex detector technologies currently being pursued. Each technology imposes its own constraints on the issues of mechanics and integration, as well as the basic choice of long barrels vs short barrels plus end-disks. The discussion of these options will form an important part of this report.

**2. ONGOING SENSOR R&D**

**2.1. Technology and Architectures**

Physics requirements push the tracker sensor specifications to new levels. While much has been learned in nearly two decades of VXD on Silicon detectors for the LHC experiments, the ILC requirements motivate new and complementary directions for the detector development. The key features steering the activities and ultimately defining the figures of merit against which a choice of the technology will be performed, may be outlined as follows:

- single point resolution of $\sim 3\,\mu$m at least for the innermost layer
- single layer thickness of $\approx 0.1\%\ X_0$, again with emphasis on the innermost layer



"White Paper" → **ILC Vertex Tracker Status Report**

- Initiated at Snowmass (M. Battaglia, M.Caccia, M.Winter et al.)
- Discussed already at the ECFA 2005 in Vienna

**Status now:**

A **document** giving the **scope** of the report and describing the **guidelines for the authors** is now **being finalized**.

This will then be **sent to the representatives** of the various technologies asking for their contributions.

The hope is that this report will give an in depth overview of the **different technologies** for the VTX, their pros and cons, and the status of the **R&D focused on the application at the ILC VTX**.

**It could be an extremely useful document, in particular in view of the R&D panel review for the VTX Tracker scheduled next year.**