

Silicon tracking for LDC

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***The LDC Meeting at the ECFA ILC Meeting, in Valencia,
November 11 2006***

4 components: SIT, SET, FTD, ETD

Central barrel End cap

SET and ETD CAD designs based on:

- a unique type of elementary module,
- made of 1, 2 or at maximum 3 sensors (“universal” sensor), single sided (false double-sided)

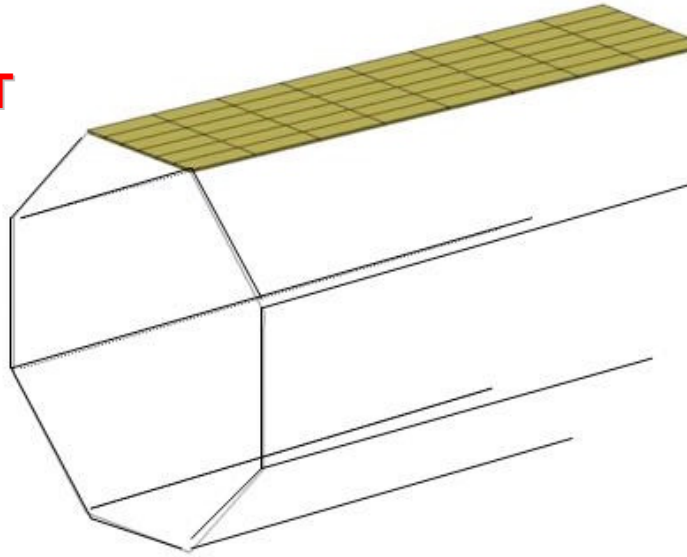
SIT an FTD design will be most probably different:

- baseline for SIT still double sided microstrip detectors
- Pixel alternative are now seriously addressed by various SiLC teams both from the point of view of simulations and of Si technology. An effort is launched in this direction within SiLC.

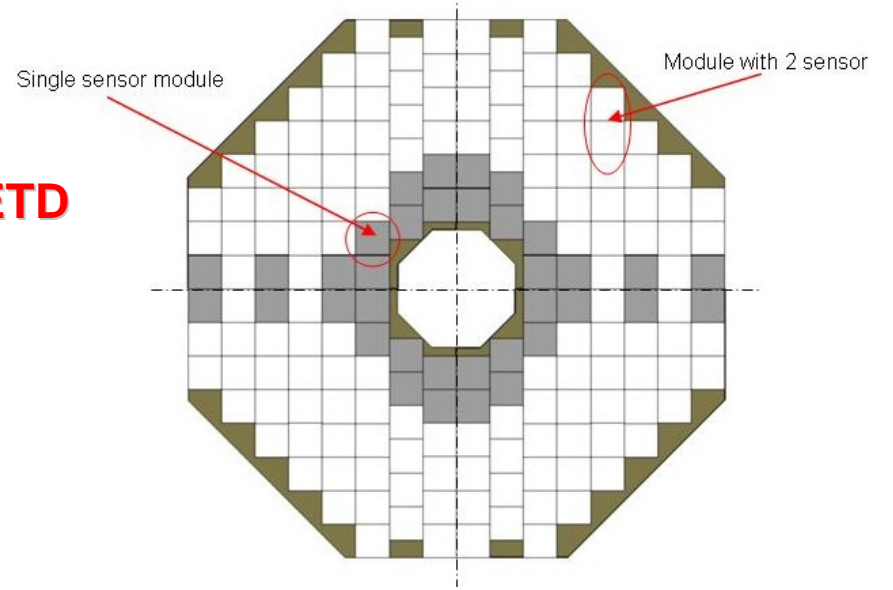
Likewise for the FTD disks:

- “Conventional” hybrid pixel à la BTeV are the proposed baseline
- Other pixel solutions are starting to be studied by several SiLC teams

SET

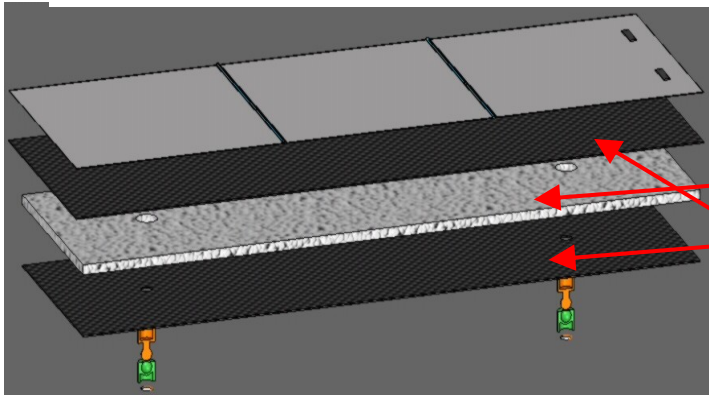


ETD

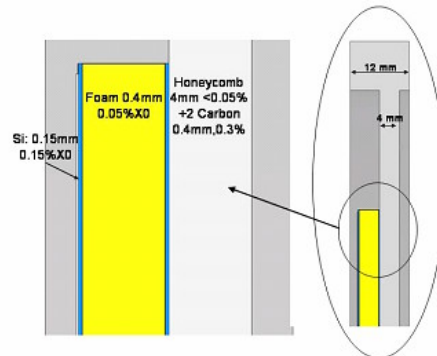


Thinned Sensors + chips

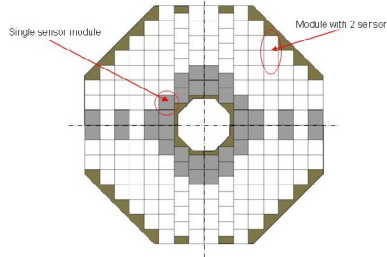
Foam + 2 Cfiber slices



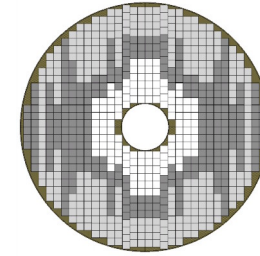
Elementary module 0.7%X0 → 0.5%X0



Total: 0.87%X0/layer



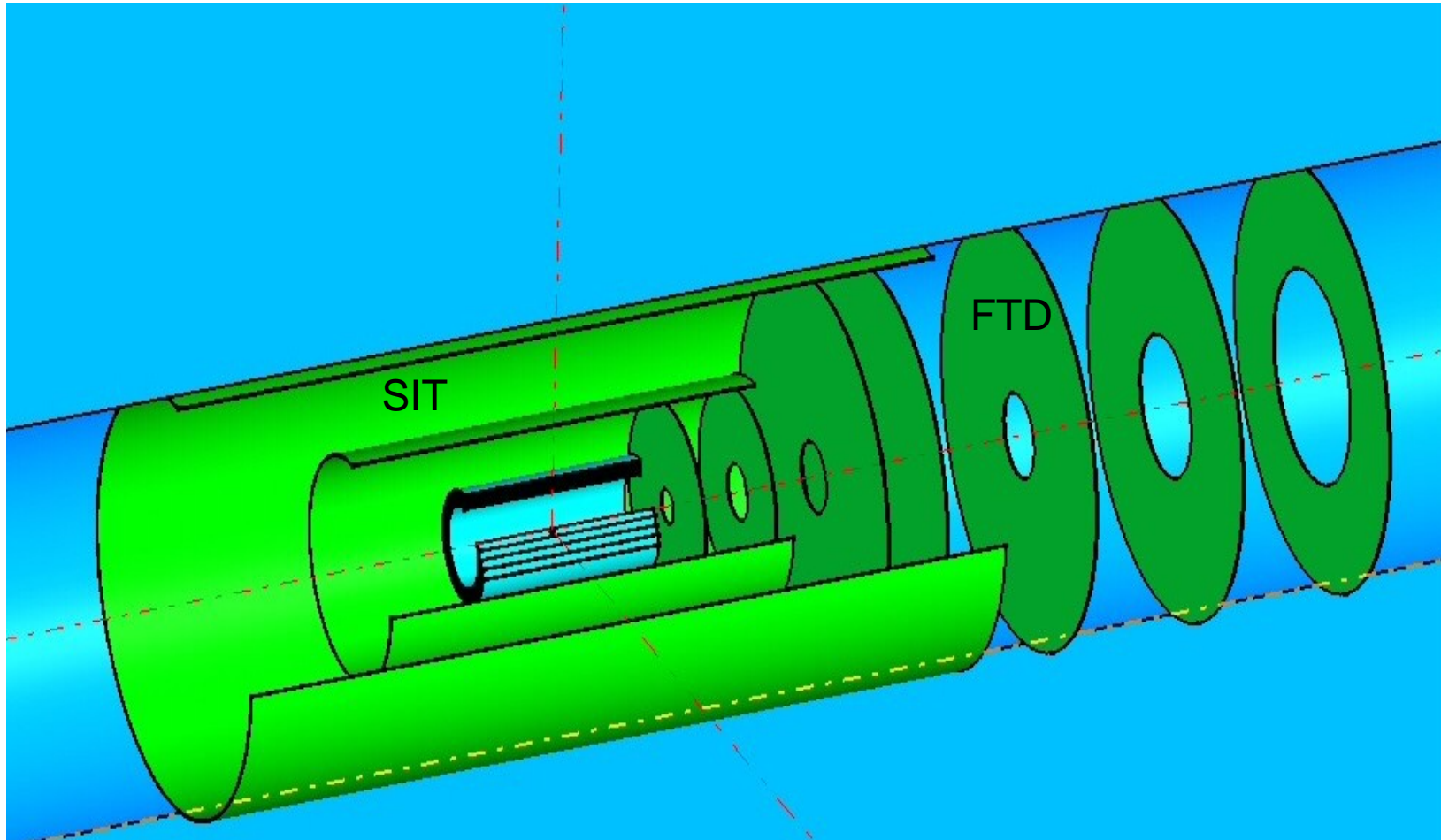
ETD

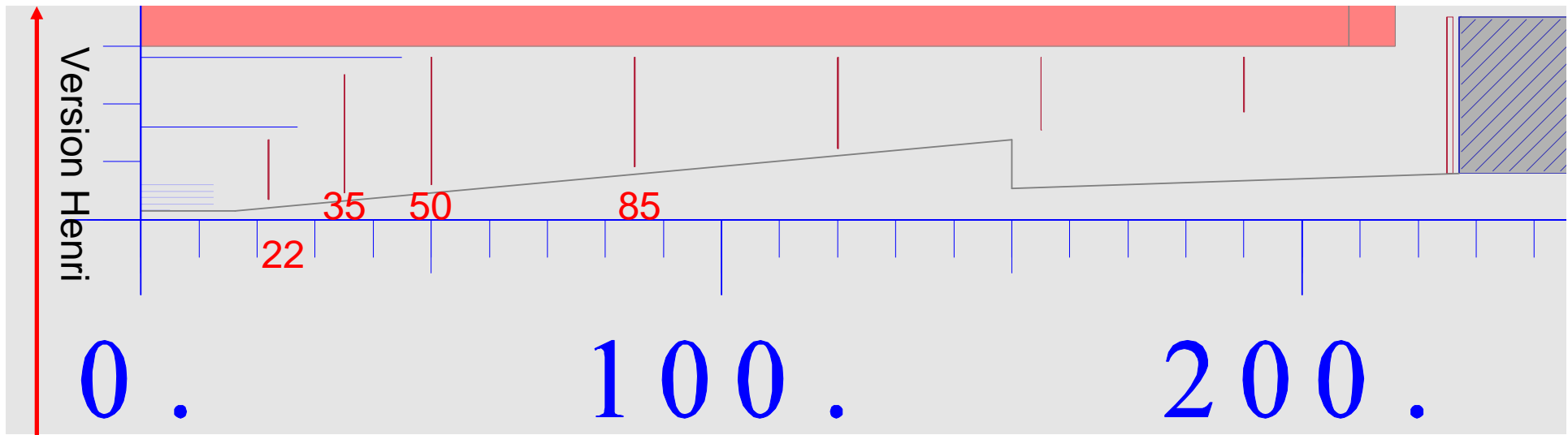


The total percentage of X0 per layer at this present stage of the design is 0.87% all included, per layer in the ECT with the proposed structure.

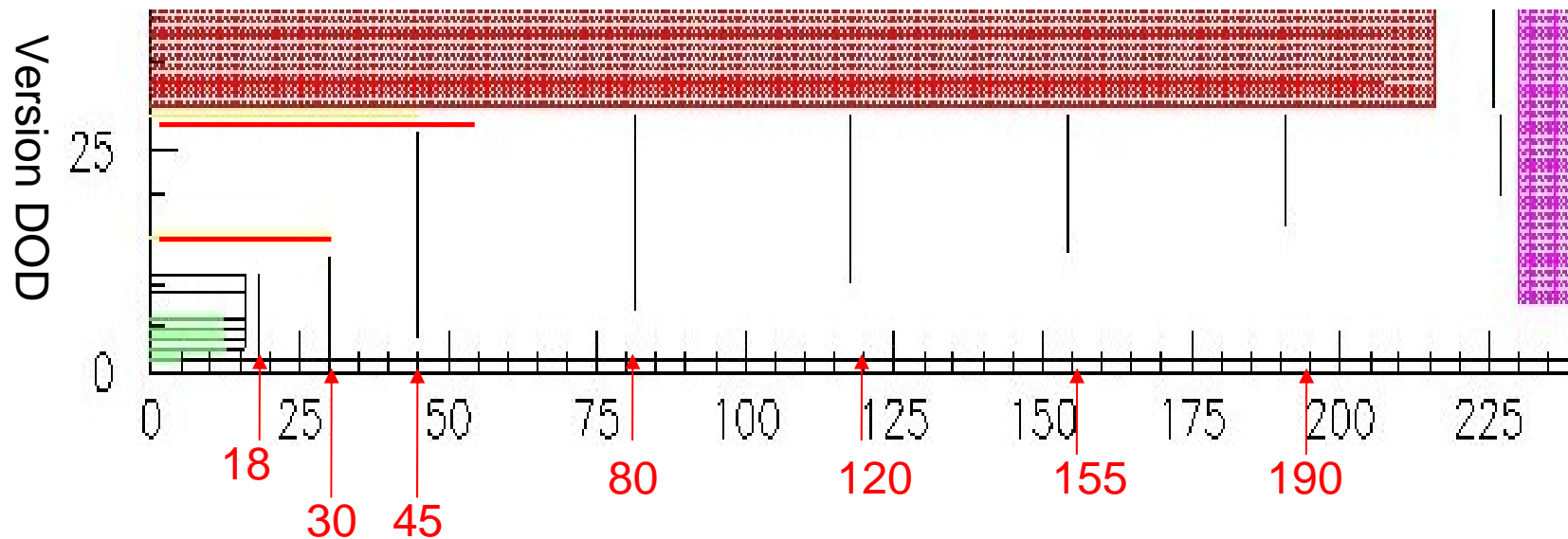
It is interesting to note that in one or the other design, the total number of elementary modules and of channels to be read out is similar. In the 10x10cm² sensor case, there will be respectively 68, 88 and 92 modules with respectively 2, 3 or 4 sensors, leading to a total number of 248 modules and 253952 channels per plan, thus a total number of channels of 661856 per XUV. In the 20x20cm² sensor case, there will be 36 single sensor modules and 72 double sensor modules per plane. This will lead to 221184 channels per plan and a total of 663552 channels per XUV.

The inner tracking part: SIT + FTD





In total 7 disks are proposed on either side that will be located at distances of 18, 30, 45, 80, 120, 155 and 190 cm from the interaction point. In addition it is under study if one would profit from an extension of the forward tracking by installing silicon disks in front of the luminosity calorimeter.

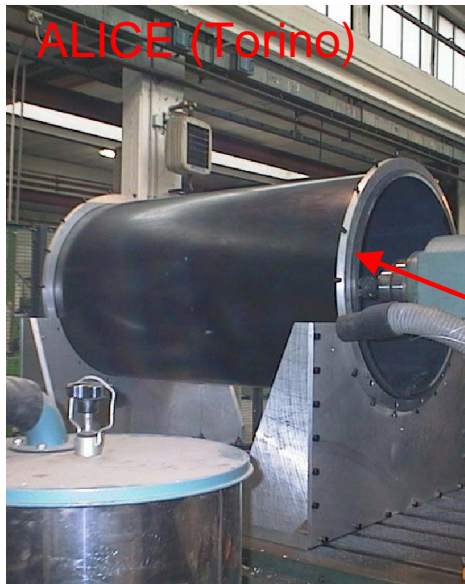


COOLING SYSTEM

A cooling system prototype must be provided for next year (EUDET). Various studies were performed with mechanical prototypes in Paris.

In the actual ILC environment for the Silicon tracking system the cooling system is defined by the following conditions:

- ❖ Taking as hypothesis that the relatively low radiation level allows to reach up to 30 degrees maximum temperature
- ❖ And a temperature gradient of 10 degrees C,
- ❖ With a power dissipation per electronic channel of no more than 1mW
- ❖ The main need for cooling is to preserve the detector from the environmental conditions, i.e. the heat provided by the other devices.
- ❖ Plus the need for a Faraday envelope.
- ❖ Reducing the material budget for this envelope is a prerequisite.

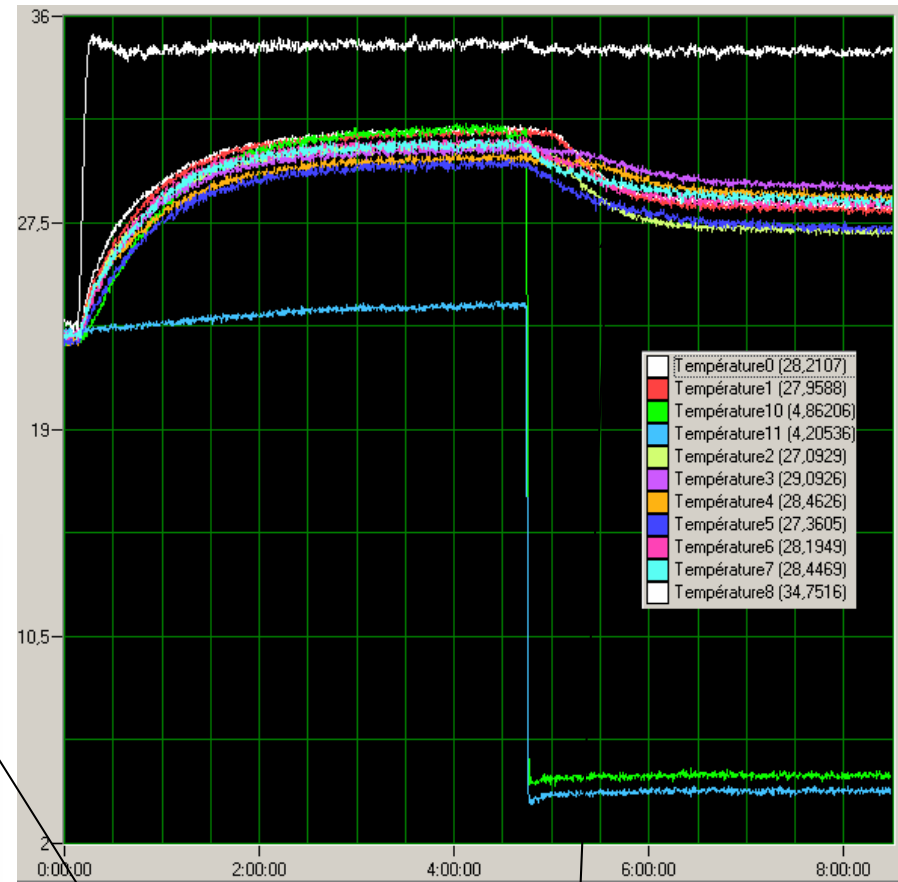
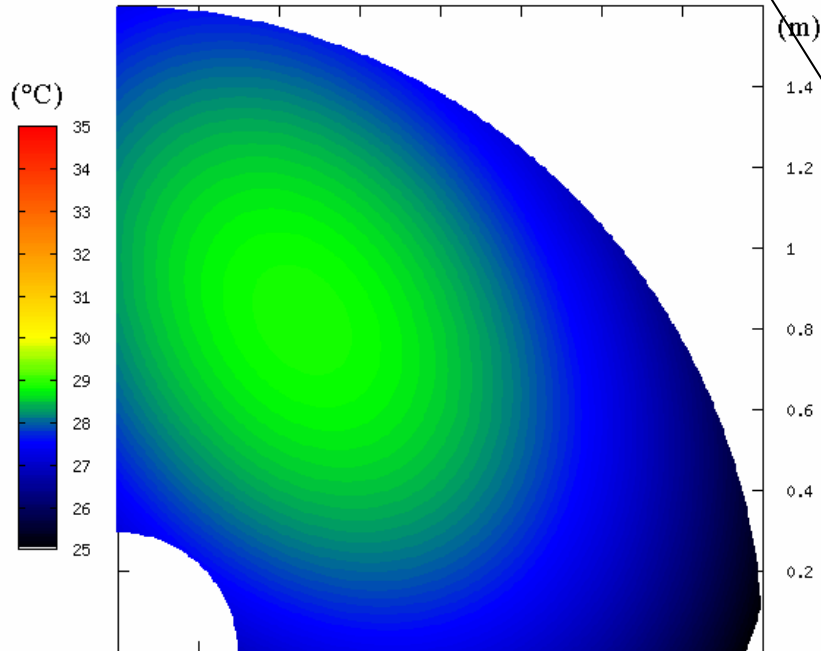
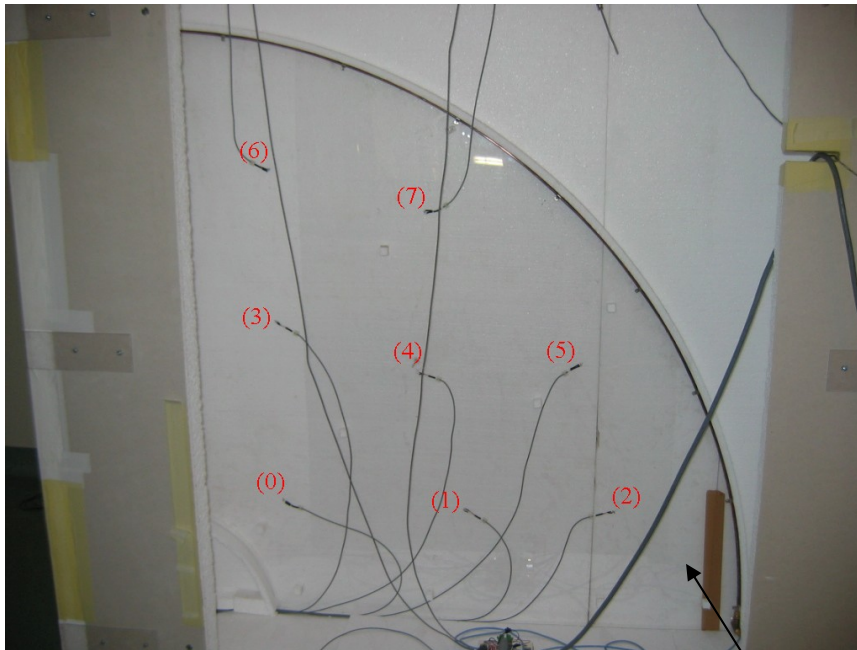


Studies are underway profiting for the expertise acquired at LHC, example:

Cylinder: 1.2m length
by 0.62 diameter
4+4 PLIES => 1,2 mm
ROHACELL => 5 mm
0,5% X0
WEIGHT = 10 kg



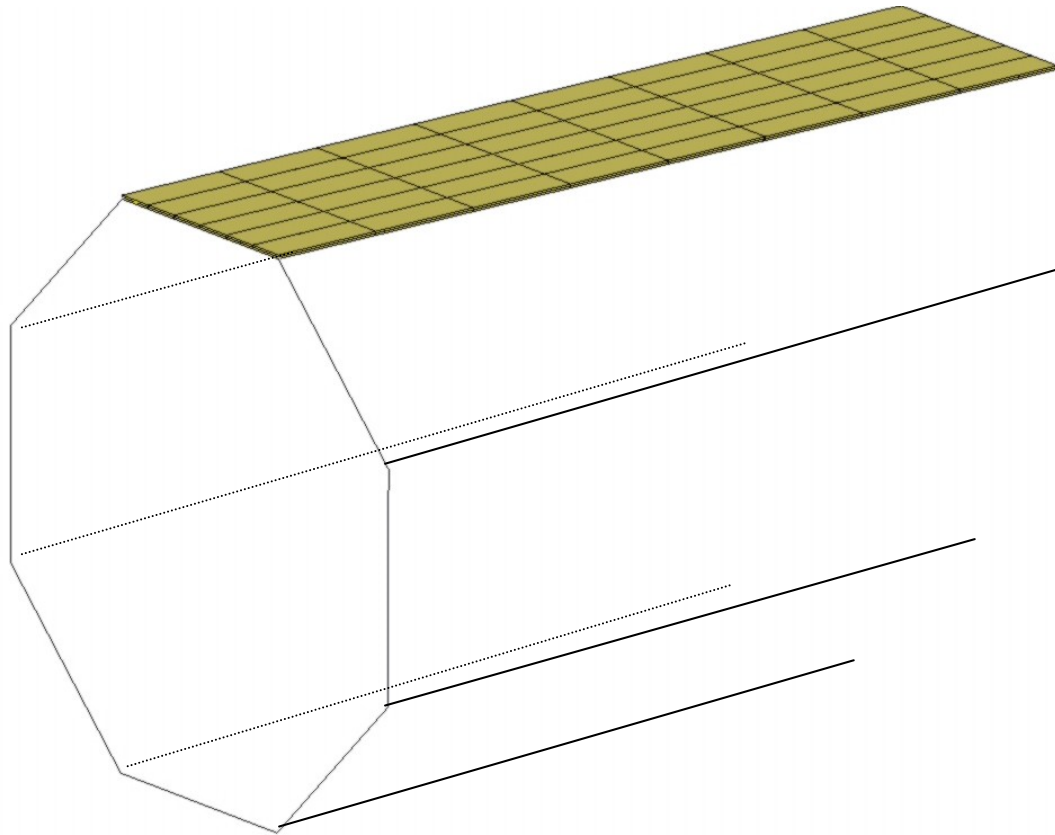
Example of thermo mechanical studies for the End Cap Si tracker (LPNHE-Paris)



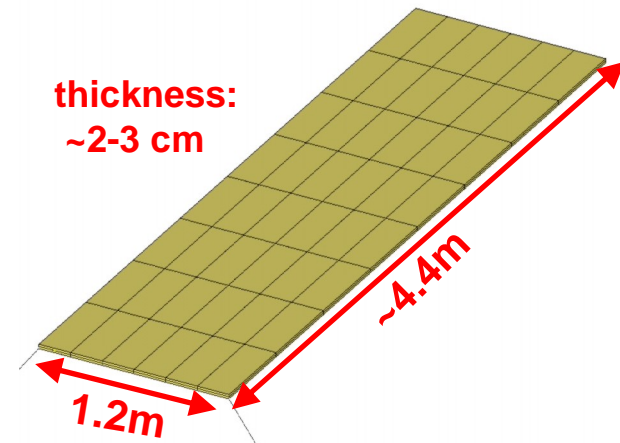
Measurements, results and modelling

SET: Silicon External Tracker

False double sided layer
60 cm long μ strips
20x20 cm² sensors

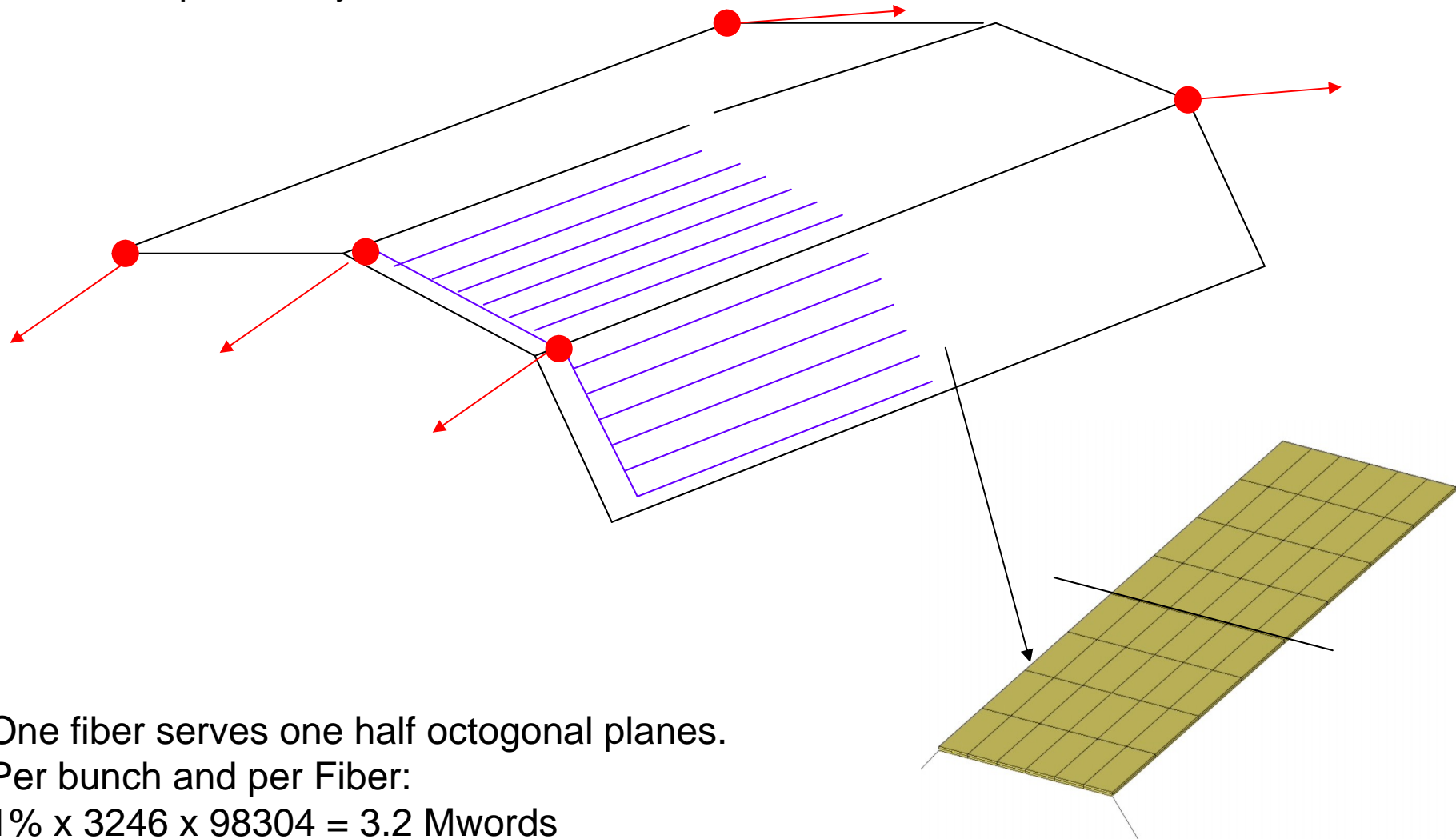


Total surface: ~86 m²
Nb channels: 1,572864
Nb of fibres: 8 per side



# ladders/octagone	96
# sensors/octagone	288
# channels/octagone	196608
# μ chips/octagone	192
# μ coax/octagone	192
# fibres/octagone	2
# μ chips/fibre	96
# voies/fibre	98304

Daisy chaining the FE chips of 4 adjacent modules, on the 2 planes of the same octagonal plane, with a micro coax; Thus 6 micro-coax/octogon plane on each side, all read out in parallel by fibres.



One fiber serves one half octogon planes.

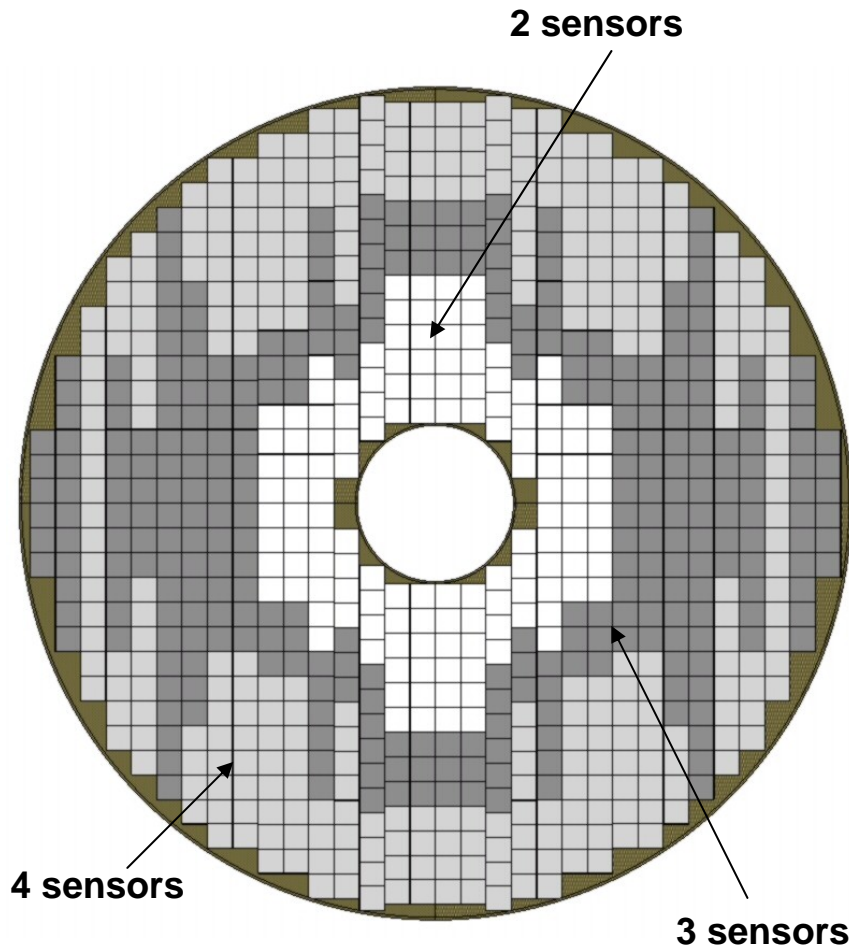
Per bunch and per Fiber:

$1\% \times 3246 \times 98304 = 3.2$ Mwords

Thus 19.2 Mbyte or resp 32Mbyte depending the processing on detector

Duration of the readout procedure: 19.2M or $32\text{M}/6\text{Gb/s} = 3.2$ or 5.3 ms

End Cap Tracker



Total area per XUV: ~15 m²

Nb modules x 2, 3 or 4 (10x10 cm²)/plane:
68, 88, 92

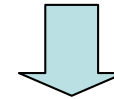
Total modules/plan: 248 (248 μ chips)

Total μ chips/plan: 248 (1 per module)

Total Nb of channels/plan: 253952

Total Nb of channels/XUV: 761856

All these numbers X 2 because 2 sides!



Total number of chips: 1488

Total number of channels: 1,523712

***For this design:
modules are made of 10x10 cm² sensors (6'').***

As previously pointed out the other XUV design results in the a similar Number of readout channels and thus DAQ parameters.

XUV gives similar scenario than SET. Thus also relatively few fibres on each side.

20/10/2011

The total data per hit channel is given by: Address(32 bits) + time(BCO) + data (10) bits.

The main challenges of the overall DAQ system sitting on the detector are to have a highly performing readout and realtime processing system with the lowest possible material budget. They have to be taken into account in the design of the overall DAQ architecture schema, the electronics components, the packaging and the cabling as well as of the calibration and the cooling systems.

4. Transmission of the data flow

We briefly give some indication about the cabling schema to transmit the data flow from the detector to the outside world. This topic will be particularly dependent of the technology developments which, in this field, are expected to be very important. Presently it is foreseen to use micro-coax cables of typically one inch diameter, 300 mW power dissipation at 1 GHz and that can be power cycled. Kapton cables are also under consideration. At a later stage in the cabling scheme, i.e. to transmit the information from the edge of the detector to the outside, 6 GHz SCM fiber optic links are presently considered. Of course all this is under serious investigations taking into account what are the prospects in the related industrial domain. Two main issues

- Cabling versus and/or fibers. Micro coax cables are making a comeback and seems to gain some favour with respect to fibers. This all issue has to be followed in close contact with the corresponding industrial developments
- High multiplexing rate versus redundancy. The present goal is to apply large multiplexing factors to reduce as much as possible the number of channels and the overall cabling, therefore also decreasing the material budget. A large multiplexing factor of at least 512/1 or even 1024/1 is under study at the A/D converter level. Then other multiplexing factors will be applied on the cabling path. Of course this has to be balanced with respect to redundancy (safety issue) in order to avoid loosing a large fraction of the detector information if any problem occurs in the readout and data processing/transmission chain. It should be mentioned that this increase in multiplexing factors should result in a decrease in the overall cost.

5. Application to a component of the Silicon tracking system

The present DAQ scheme of the external Silicon component in the LDC concept is briefly summarized here, as an example of what is currently under study.

A Silicon external tracking component (SET) sitting between the TPC and the electromagnetic calorimeter in the central barrel, has been proposed in the LDC concept [3]. In the current design it is made of 60cm long strips and it follows the octagonal design of the electromagnetic calorimeter. The overall device is divided into two parts that are assembled jointly at 90 degrees with respect to the beam axis. Each half is made of 8 rectangular plans of 2.4m length by 1.2 m width. Each of these rectangular plans are made of modules composed of 3 single sided sensors of 20 by 20 cm² bonded to each other to form the 60cm long strips. The SET component is a false double sided layer, false meaning that this layer is indeed made of 2 single sided layers. This device will cover a total area of the order of 80 m² and corresponds in the present design to roughly 1.6 million of channels to be read out.

The daisy chaining the Front End chips of 4 adjacent modules on the same half plane with micro coax cabling, results in a total of six micro coax cables for each half plan. The resulting signal would be then transmitted from the edge of each half plan to the outside world by fibers. A total of 8 fibers for each side would thus transmit the overall detector information. For safety, each fiber would be doubled by another fiber in case there is a problem. Thus 16 fibers on each side would be needed to transmit the overall processed information.

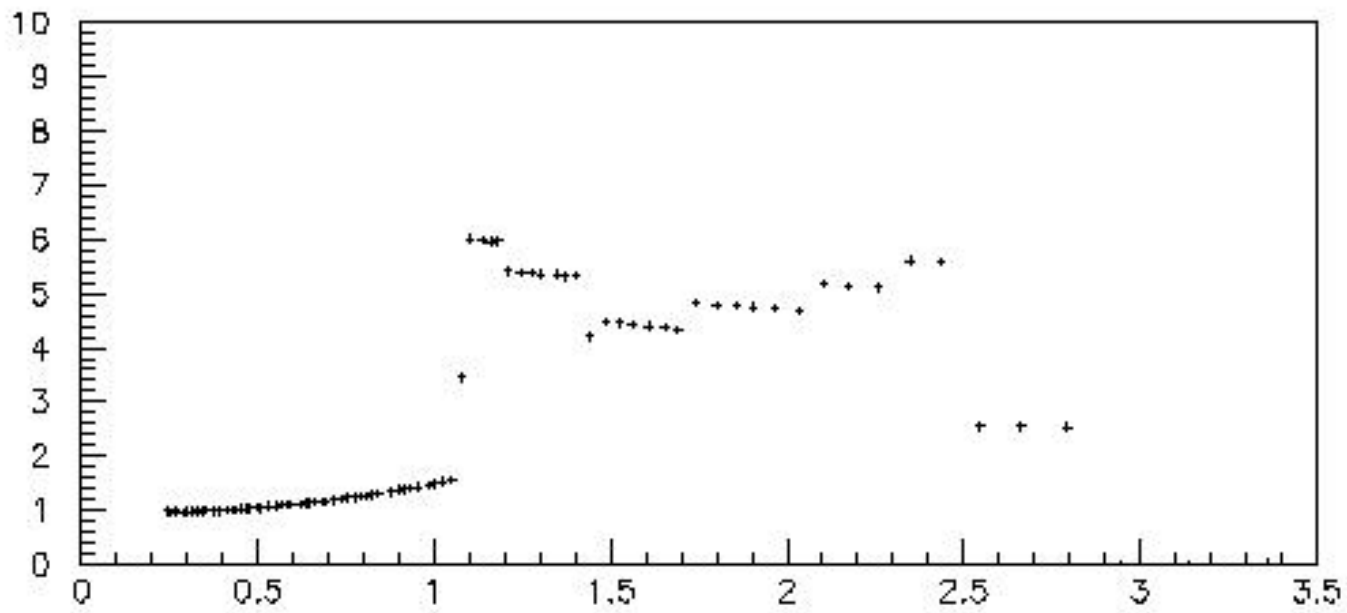
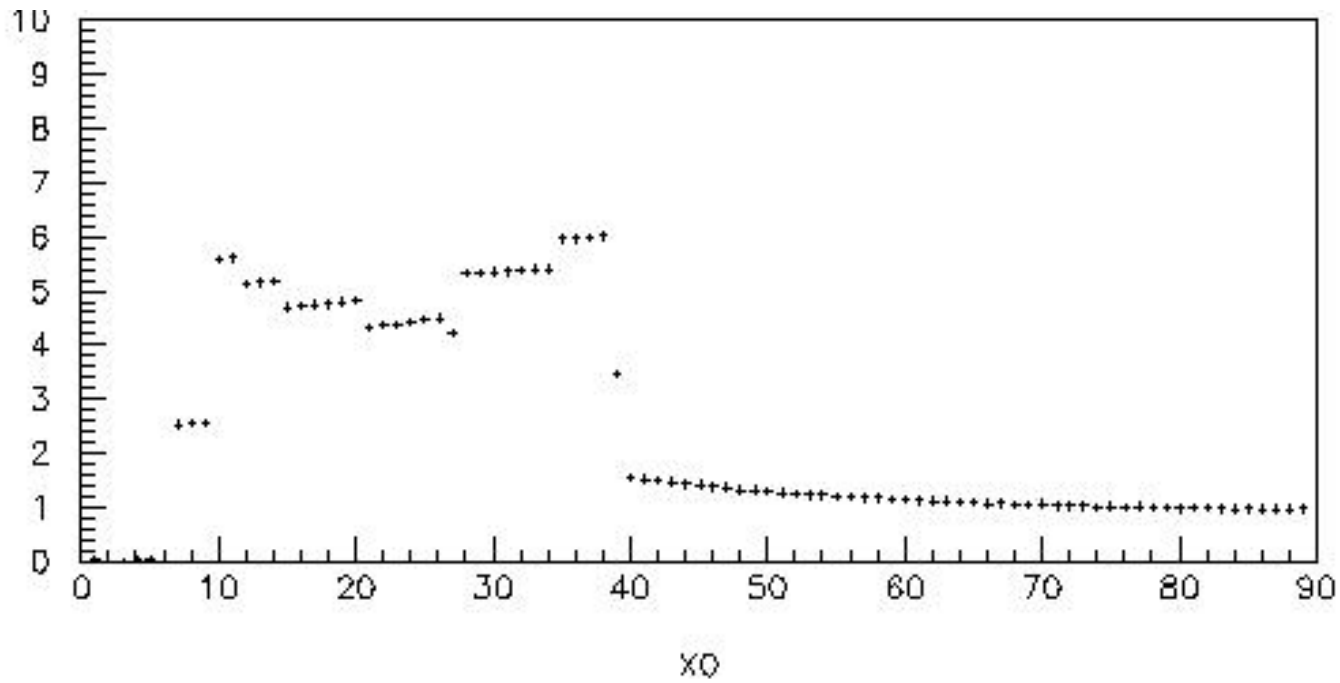
Taking for this external Silicon component a 1% occupancy, 3000 bunch trains per crossing and of the order of 100000 channels treated by fiber, this gives 3.2 Mwords per bunch and per fiber and between 19 to 32 Mbytes depending the processing on detector, as a total. It corresponds to 3.2 or 5.3 ns total processing duration for 6Gb/s fibers. This gives the current status of thinking on the total amount of informations to be transmitted by these very large area tracking components, a tentative way to reduce the needed number of on-detector chips, on detector cabling and transmission to the outside world.

People have been so far mostly focused on developing the front-end readout chips but they are starting now to start developing the design and the needed R&D on the following components of the DAQ. This includes the packaging, the cabling and the repartition of

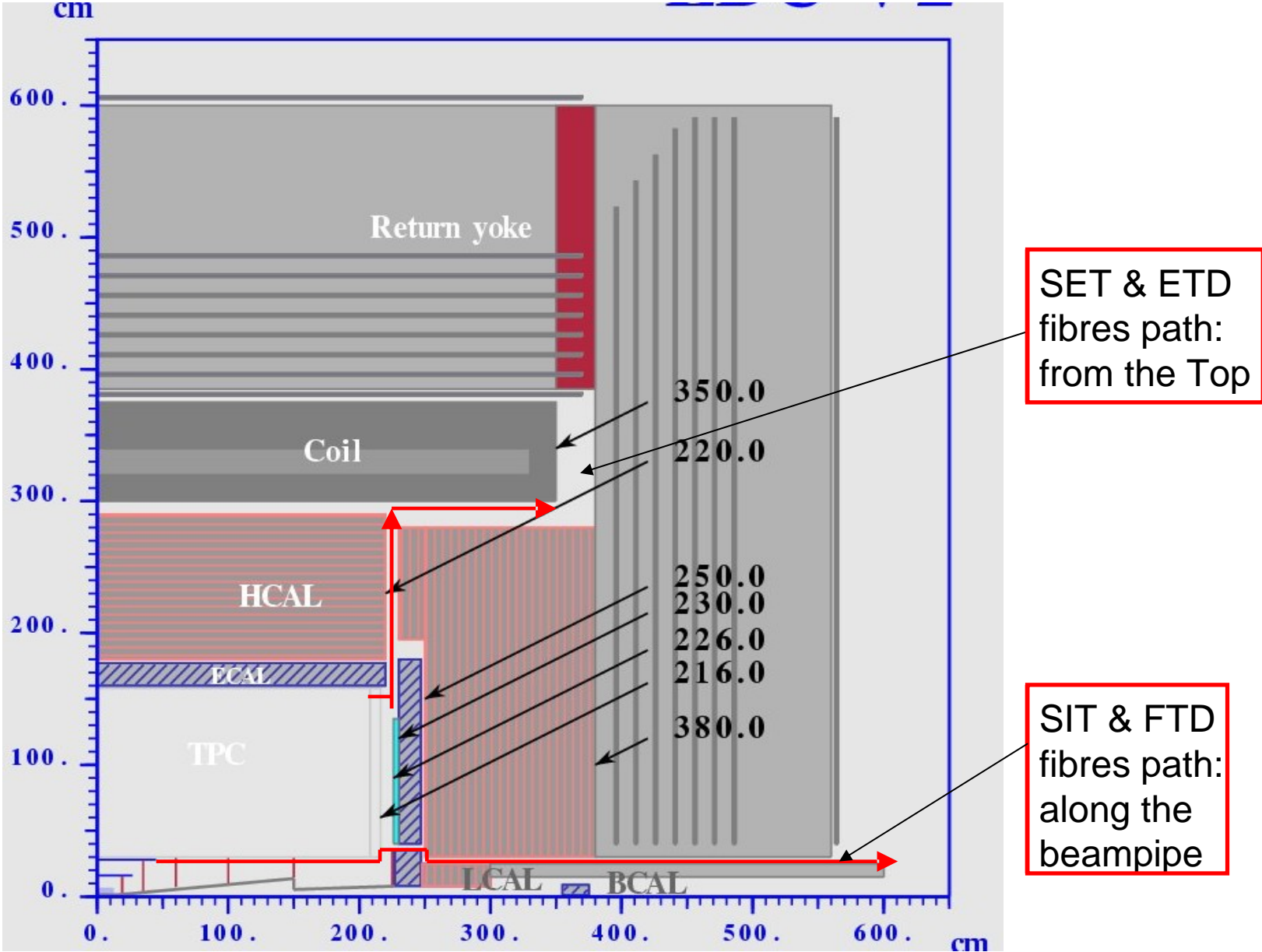
From:
 Preliminary thoughts on the DAQ for the
 next generation of Silicon Tracking systems
 To appear in Proceedings of LCWS06
 (J.F. Genat , ASN)

Material Budget

A first tentative estimate of the material budget in %X0 is given in the two plots next slide. It includes all the materials for the detectors and the electronics as presently foreseen. Also included is a 0.5%X0 insulating envelope surrounding the detector components to insulate them both for electromagnetic compatibility purpose and also for keeping good thermal conditions.



Silicon detectors cabling paths out of the detector in the LDC case



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