Inductive Adder Modulators for ILC DR Kickers

Craig Burkhart *SLAC*

For SLAC-LLNL Team

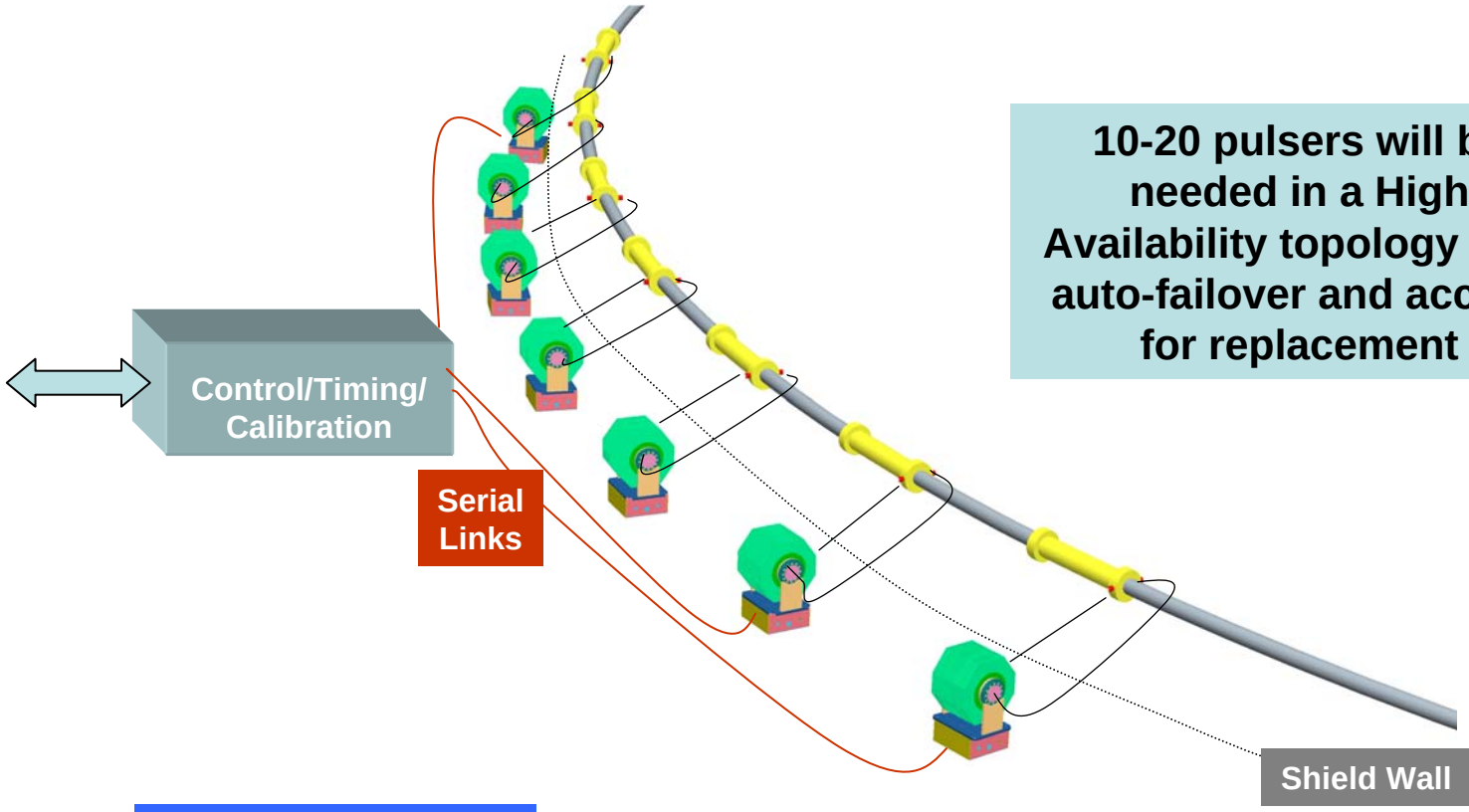
Ed Cook, C. Brooksby *LLNL*
R. Cassel, T. Beukers, C. Burkhart,
M. Nguyen, R. Larsen *SLAC*

September 26, 2006

Inductive Adder Modulators for ILC DR Kickers

- SLAC/LLNL Program
- Inductive Adder Topology
- Inductive Adder Modulators
- Areas of Advanced Development for ILC DR Applications

System Topology



10-20 pulsers will be needed in a High Availability topology with auto-failover and access for replacement

C. Brooksby BN/LLNL

DR Kicker Modulator Requirements

Pulse Length:	~5 ns
Output Voltage:	± 10 kV (two simultaneous pulses of opposite polarity required)
Load Impedance:	50 Ω
Burst Repetition Rate:	~3MHz
Burst Duration:	~ 3000 Pulses
Average Repetition Rate:	15,000 PPS (5 bursts per second)
Intra-pulse Stability:	7×10^{-4}
Bunch spacing:	20 ns

SLAC/LLNL High Availability (HA) Damping Ring Kicker System Development Program

- Goal: Demonstrate *Full System Architecture* for HA Damping Ring Kicker System
  - Develop prototype
  - Multiple unit operation
  - System timing
  - Calibration
  - Diagnostics
  - Auto-failover
  - Demonstrate reliability
  - Evaluate System Trade-offs

SLAC/LLNL High Availability (HA) Damping Ring Kicker System Development Program

- Motivation
  - System Development: Many groups working on kickers to optimize pulse shape, but overall system needs prototype demonstration.
  - High Availability: Reliability/Availability critical for system of ~ 10-20 or more pulsers in series.
  - Inductive Adder: Induction modulator has ideal balanced output architecture (+/- 10kV output) but needs optimization for rise & fall time, impedance matching, stability of calibration, HA service features.

Basic Design

- Modular Inductive Adder Topology
  - Extra modules and auto-failover if one or two modules fail
  - Each module has multiple MOSFETs in parallel
  - Balanced output for identical pulses to each side of kicker e.g. 200A into 50 Ohms
  - Multiple units to make full kicker system
  - Small units easily substituted when one fails
  - Redundancy in form of extra kickers for >99% Availability
  - Sophisticated card-level diagnostics for HA management

FY ’07 Goals

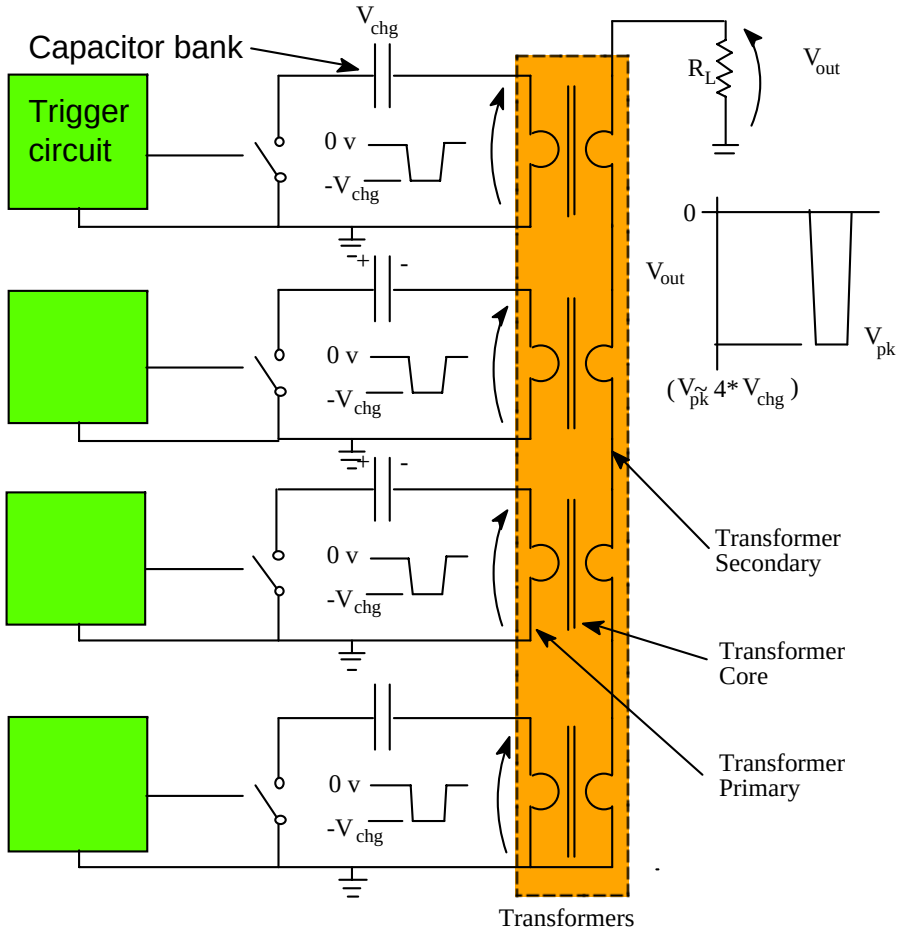
- Complete development and testing of short pulse (~5 ns) module
- Initiate development of prototype modulator: 5 ns, $\pm$10 kV, 50 Ω , 3 MHz
- Start design of calibration system
- Initiate design of timing system

SLAC/LLNL FY ’07 Budget (pro-forma)

- LLNL
  - $225k M&S (transfer from SLAC)
  - Fractional support: E. Cook, designer, & tech
  - Prototype development
- SLAC
  - 0.3 FTE
  - Prototype support systems development: controls, timing, & calibration

Inductive Adder Circuit Topology

Note:
Conceptually, for fast pulses, the mechanical structure of an inductive adder is virtually identical to that of an induction accelerator



Inductive Adder Concept - Simplified Schematic

E. Cook LLNL

Inductive Adder Topology: Advantages

- Modular: Adder comprised of a stack of identical modules
  - Topology arrays discrete switching devices: parallel/series
  - All modules triggered independently
  - Scaleable to higher voltages by adding modules
  - Redundant: can run n/N
- Single-turn transformer has high bandwidth
- All drive components ground referenced
- No dc high voltage
- Pulse format defined by external trigger generator
  - Pulse width and PRF agility
  - High burst frequency: >1 MHz

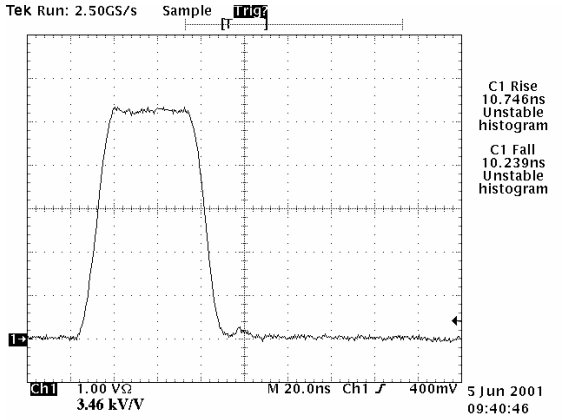
LLNL Inductive Adder Systems

- Dual-Axis Radiographic Hydrodynamics Test Facility (LANL)
  - ±18kV ± 10% into 50 Ω
  - 10ns rise and fall times
  - 16–200ns adjustable pulse width
- Plasma Electrode Pockel Cell (LLE/LLNL)
  - 0-20kV into capacitive load (Z ~ 12.5 Ω)
  - 0-200ns flattop to ±1%
- Accelerator Test Facility (KEK)
  - ±8.5kV into 50 Ω
  - ~10 ns flattop, ~20 ns FWHM

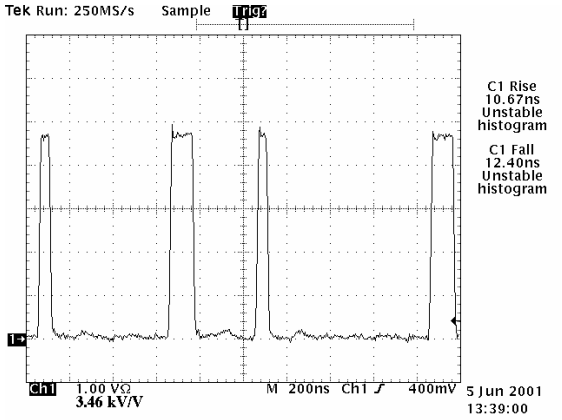
±18kV Pulsers for DARHT Dipole Kicker

DARHT Modulator Output Characteristics

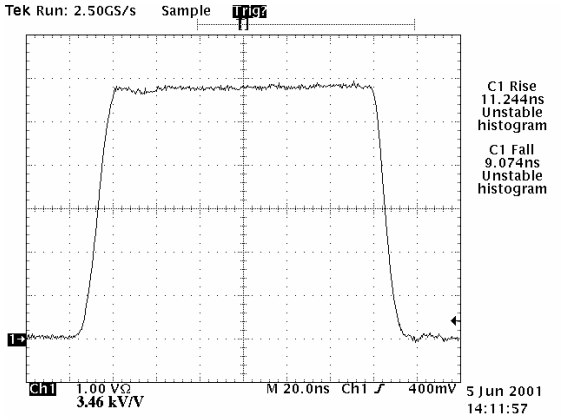
Output:
30 ns,
18 kV,
50 Ω



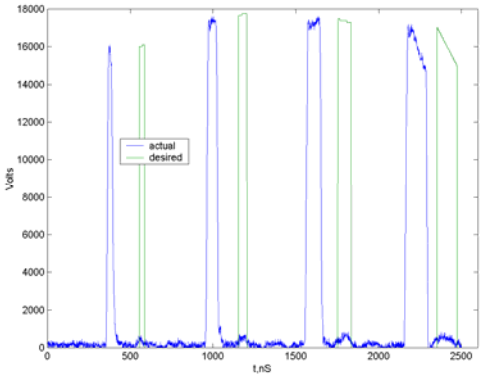
4-Pulse
Agile Burst:
Pulse Width
Frequency



Output:
120 ns,
20 kV,
50 Ω



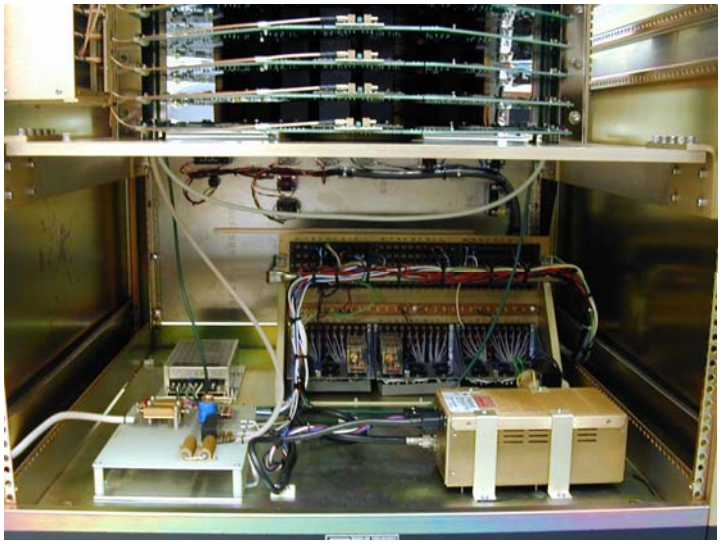
4-Pulse
Agile Burst:
Amplitude
Modulation



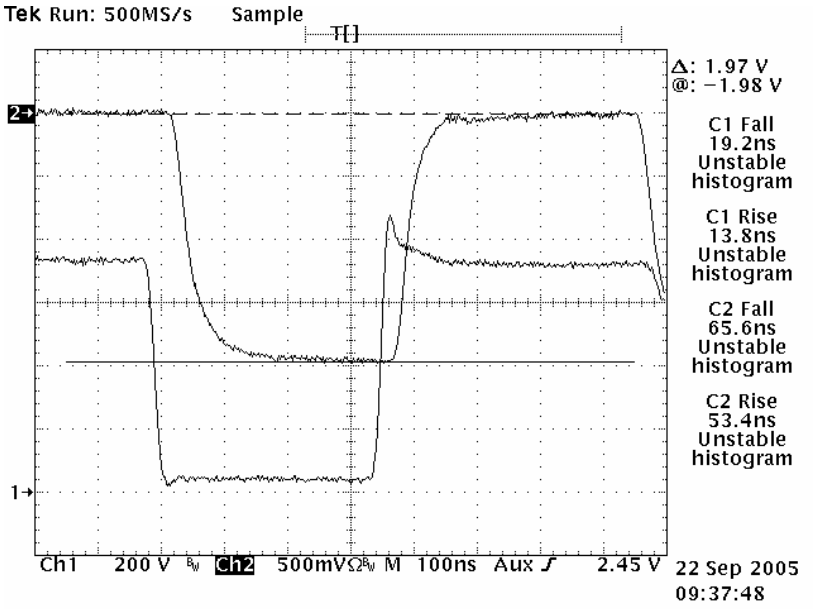
NIF PEPC Modulator

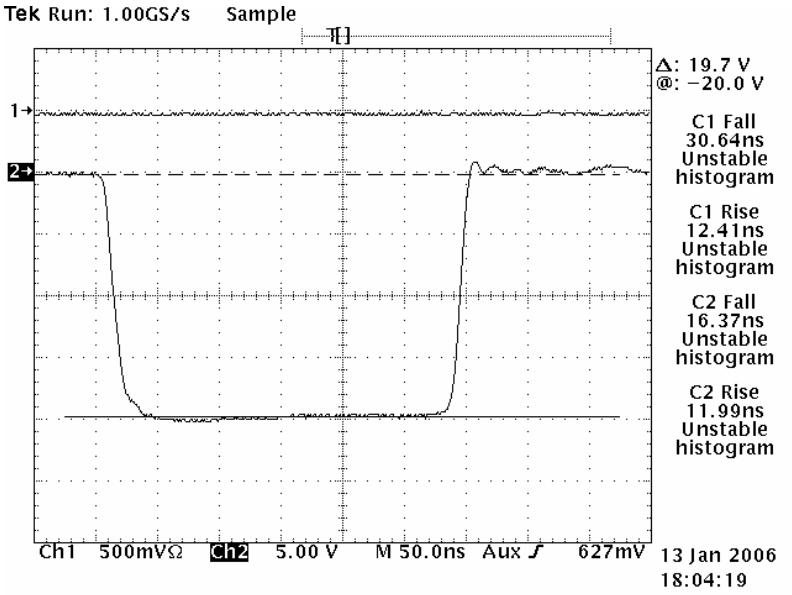
Completed assembly w/ temporary control panel

Controls, power supplies, and trigger interface



NIF PEPC Modulator: Stalk Impedance





Initial Stalk Design:
Top: V_{load} @ 5kV/div (resistive load)
Btm: V_{drain} @ 200V/div

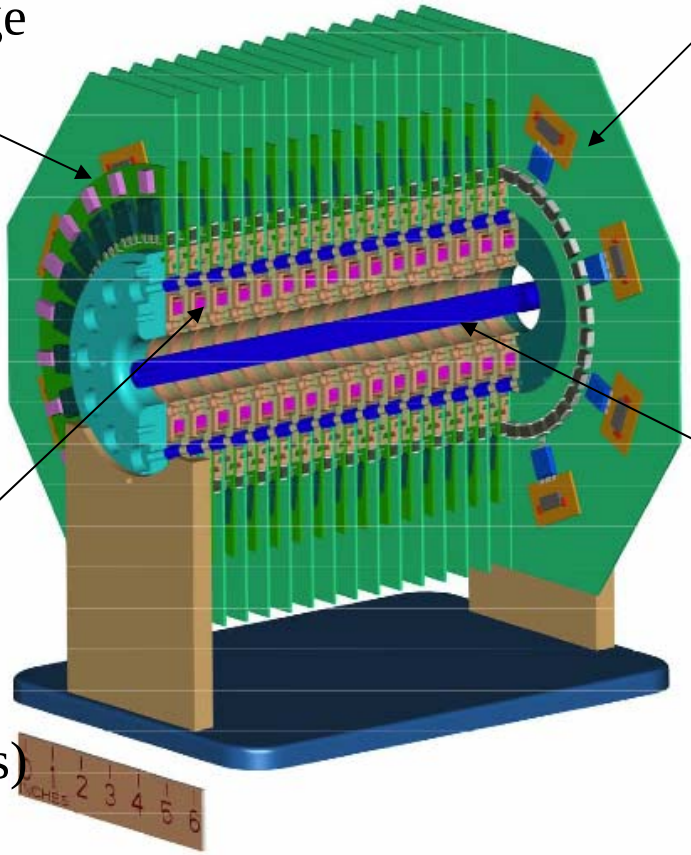
Corrected Stalk Design:
Btm: Vload @ 5kV/div

Initially did not meet risetime requirement into load. This was due to stalk impedance being too high resulting in multiple reflections within modulator which slow down output risetime. MOSFET switching transitions are fast enough to meet requirements.

KEK ATF Adder Conceptual Layout

Diode clamp bd. (MOSFET over-voltage protection)

MOSFET drive bd. with surface-mount capacitors



Cross-Section of adder cells

Center Stalk - will be connected to kicker structure with cables (configuration shown for pos. & neg. polarity pulses)

Prototype Components - MOSFET Drive Board

Master Trigger Circuit

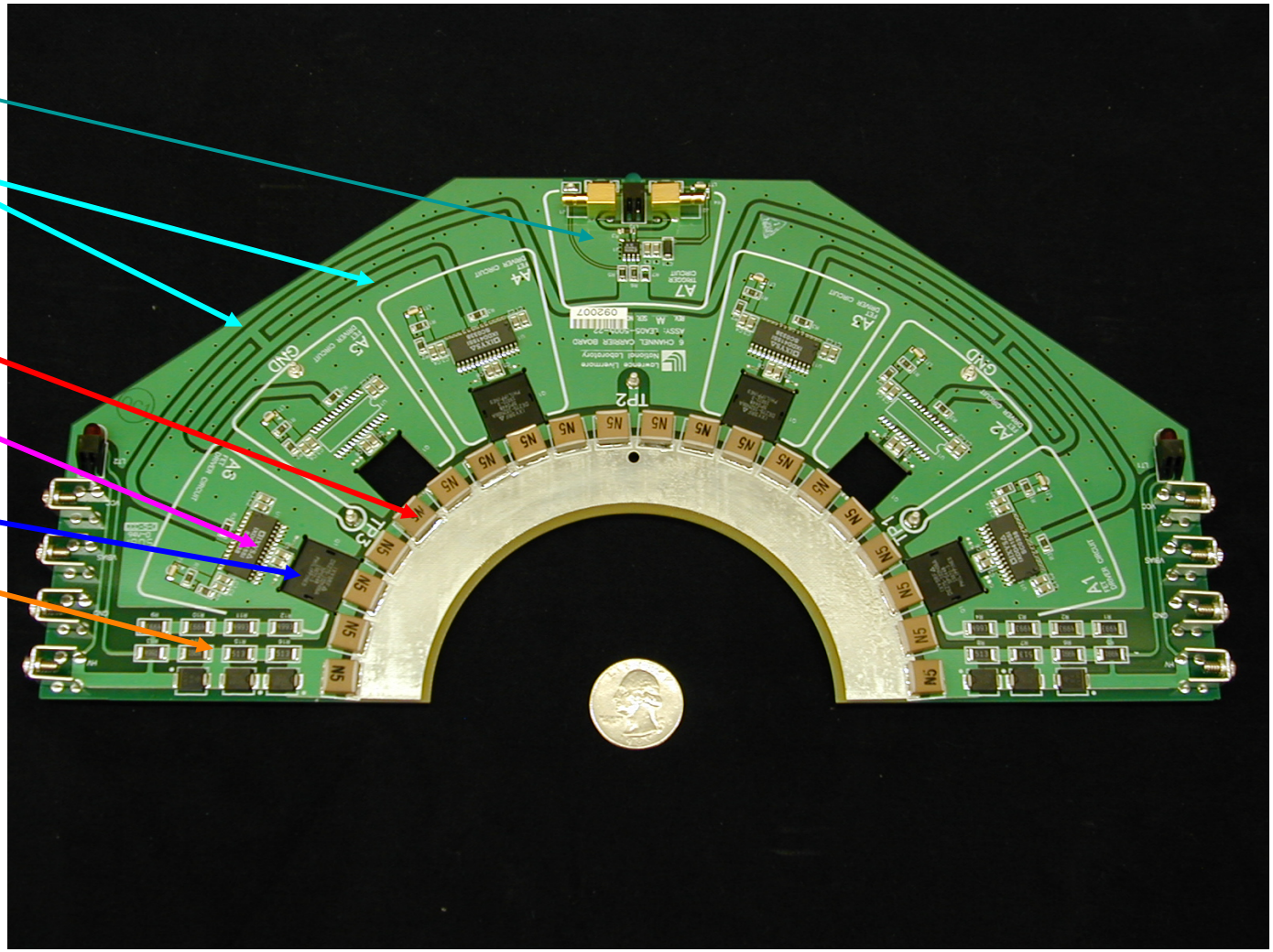
Trigger Distribution Traces

Capacitor Array - Surface Mount Ceramics

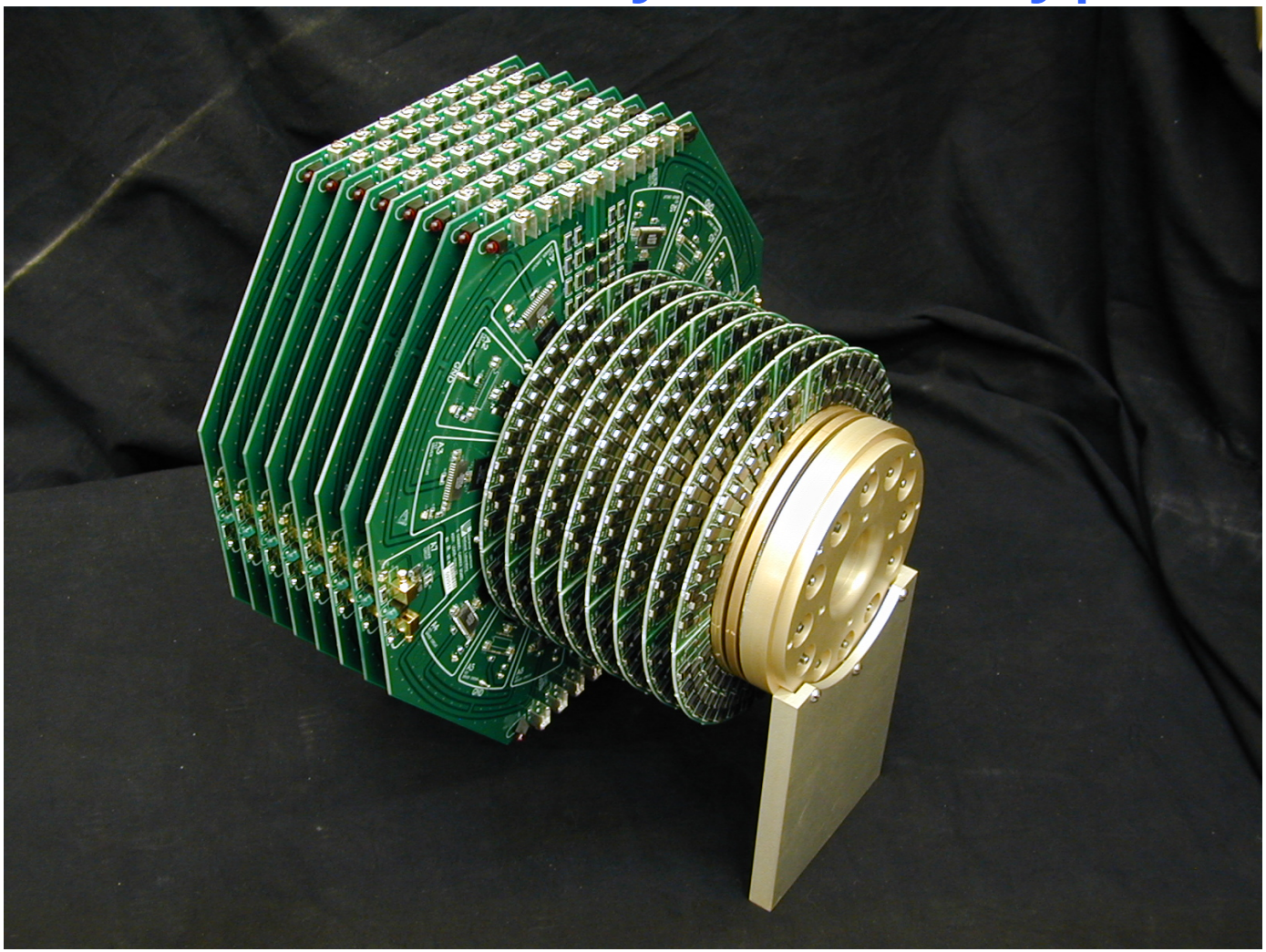
MOSFET Drivers

MOSFETs

Charge Circuit



Partial Assembly of Prototype

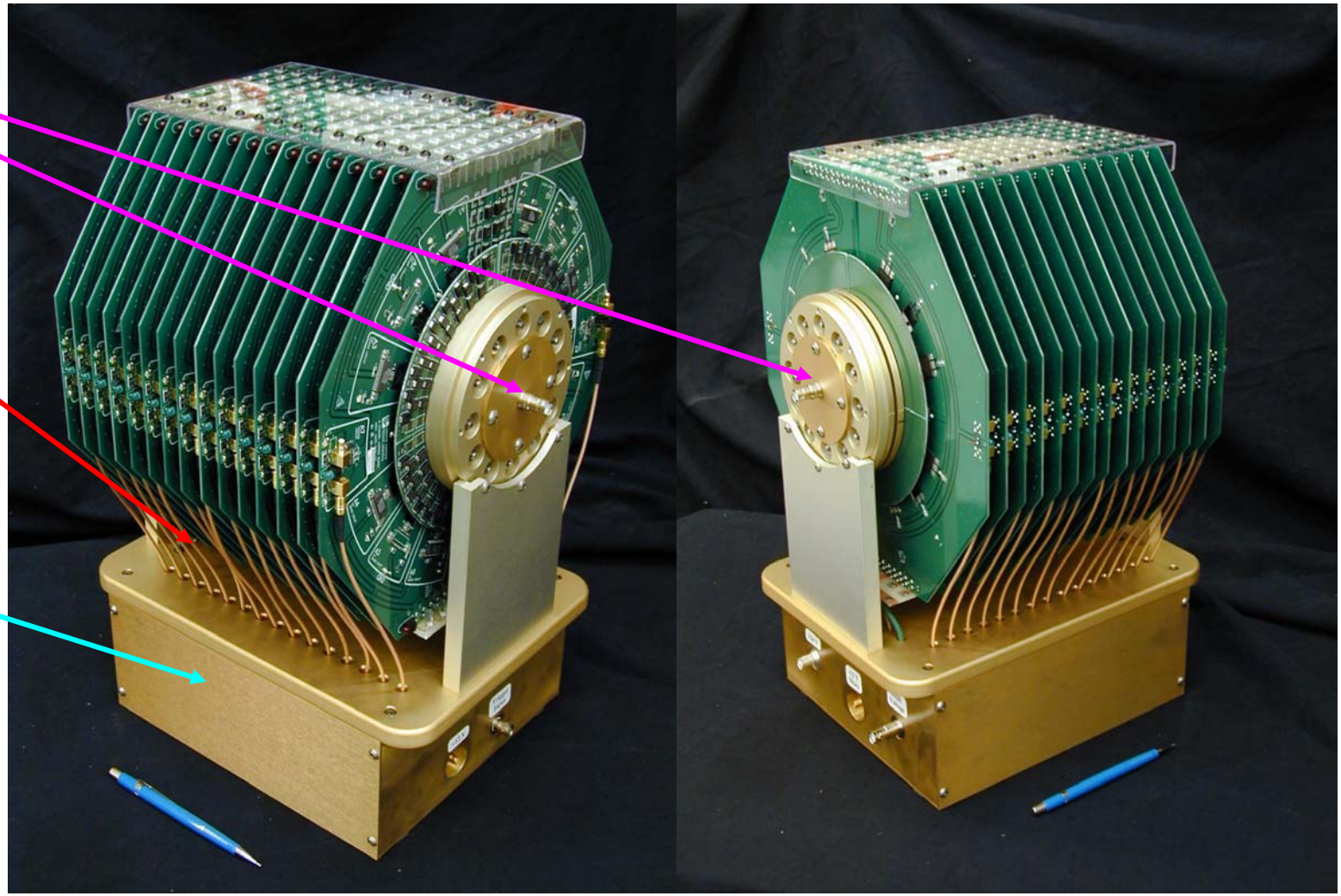


Finished Prototype

Output connectors

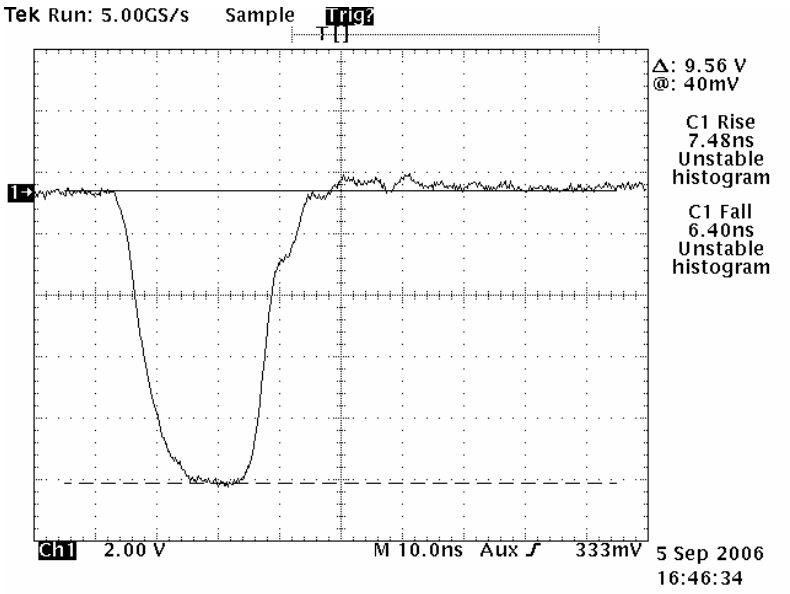
Trigger Cables

Houses trigger distribution, power supplies, etc

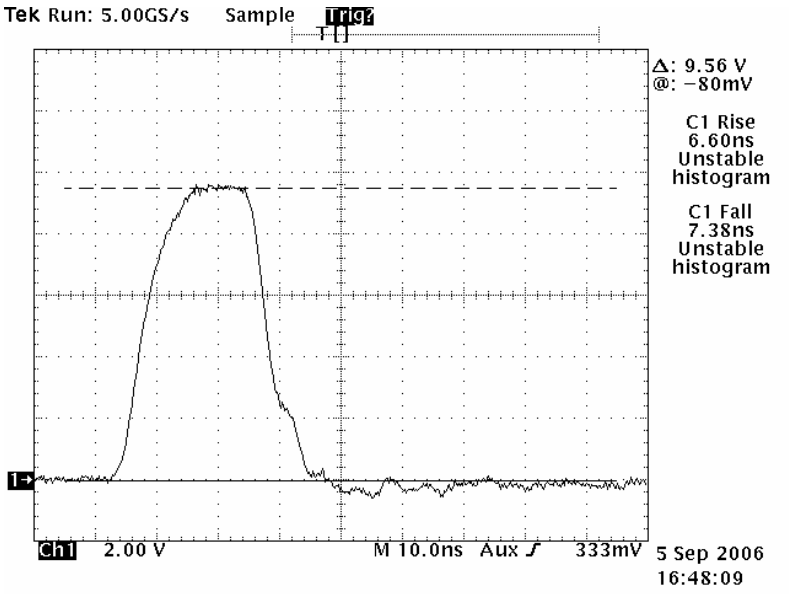


KEK ATF Modulator Output Characteristics

Simultaneous bi-polar outputs: 50 Ω load on each end



Negative Output,
-9.6 kV Flattop



Positive Output,
+9.6 kV Flattop

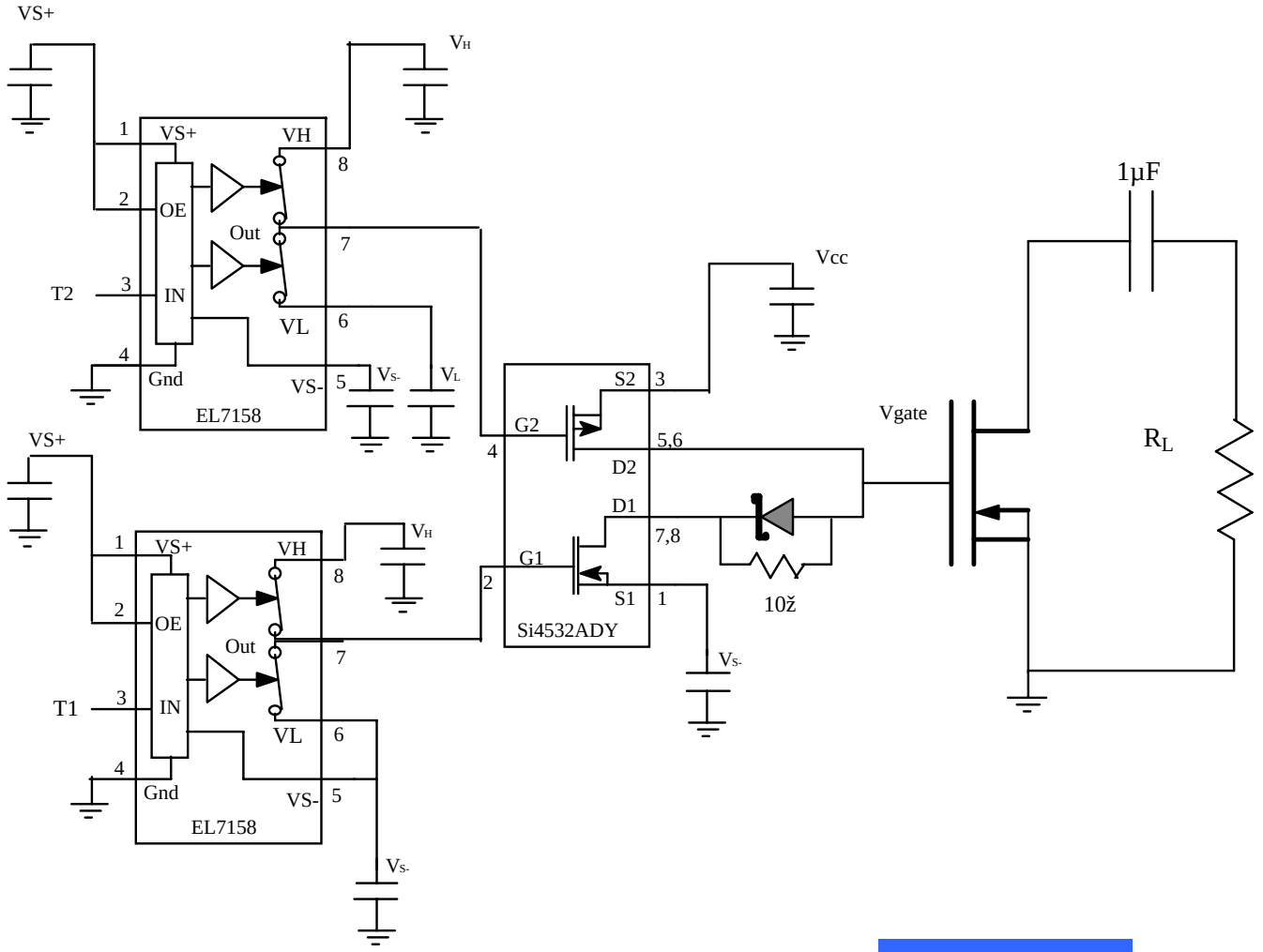
Areas of Advanced Development for the DR Application

- Decrease output pulse length
  - Improve MOSFET switching
  - Decrease propagation delays
- Improve pulse-to-pulse stability
  - Reset adder core / stabilize hysteresis
  - Recharge energy storage caps
- Address transmission line effects
  - Degradation of rise/fall time
- Cooling
  - P_{peak} ~ 8 MW, $<P_{burst}>$ ~ 100 kW, <P> ~ 0.5 kW

Output Pulse Length Reduction

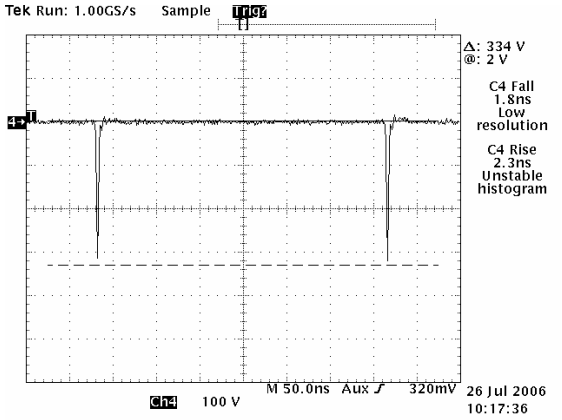
- Propagation delay through IC drivers typically 10 ns (or greater)
  - Discrete component driver
  - Advanced topology, e.g. Cascode
- Overcome package inductance: $L_G \sim L_S \sim 5$ nH, $dI/dt \sim 10^{10}$ A/s
  - Higher voltage driver
  - Hybrid packaging

Discrete Driver

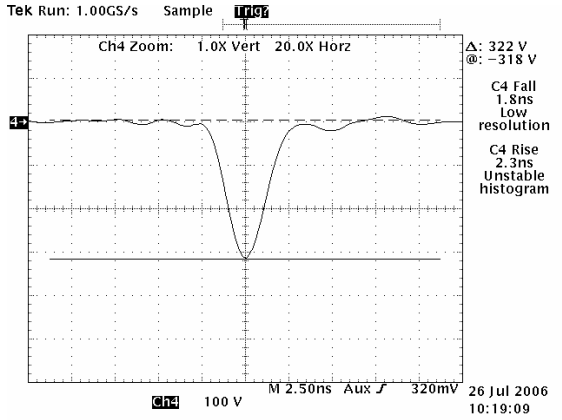


Test Results: 50 Pulse Burst @ 3 MHz, 10 Ω Load, 500 V Charge

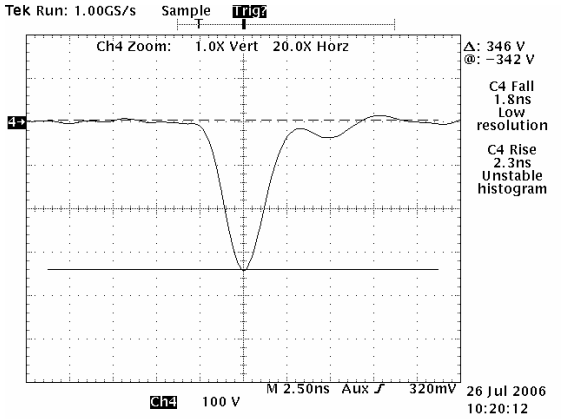
2 pulses from burst



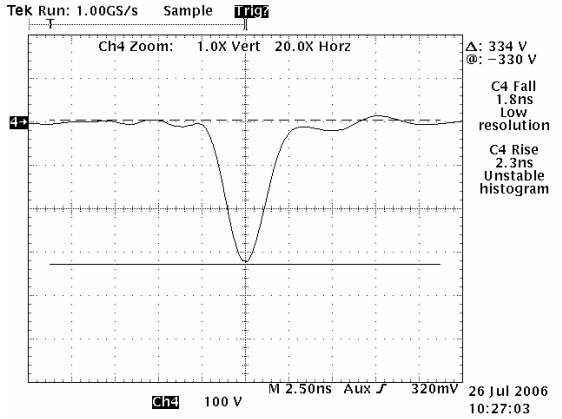
1st pulse of burst



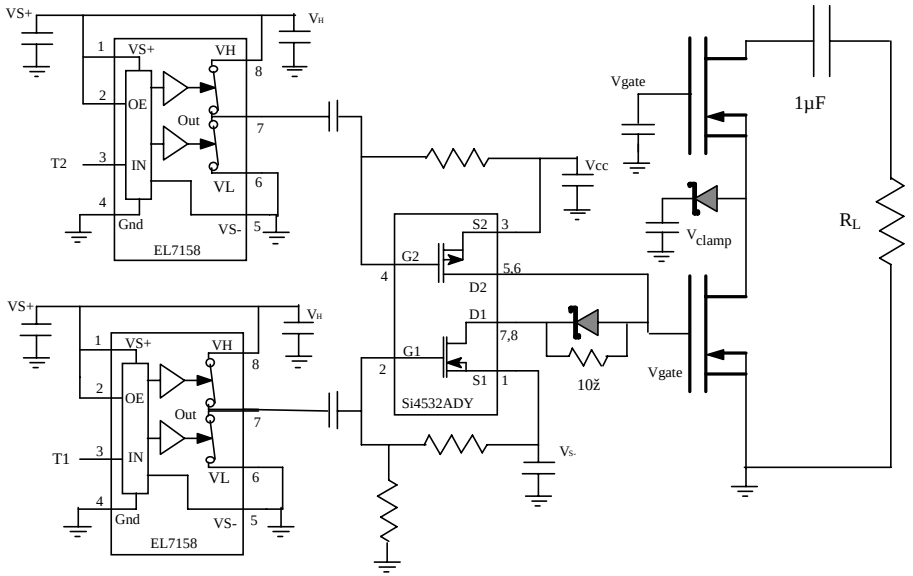
10th pulse of burst

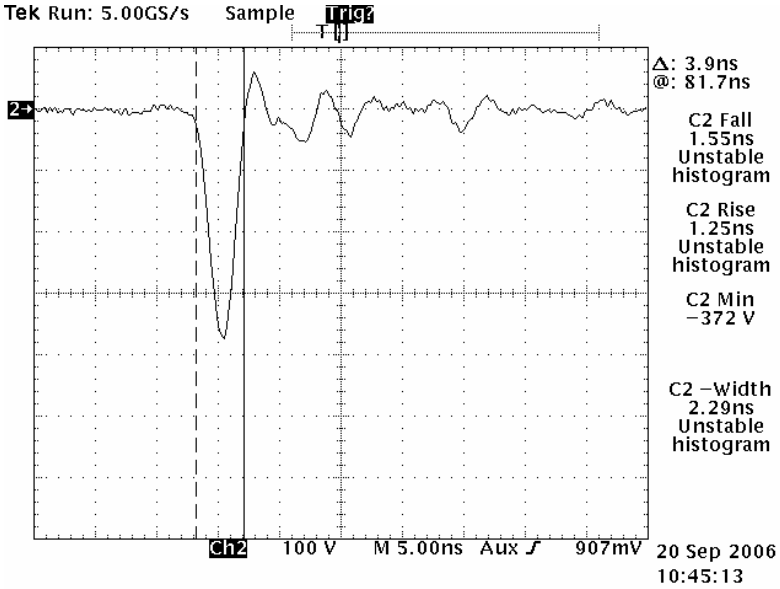


40th pulse of burst



Cascode Driver

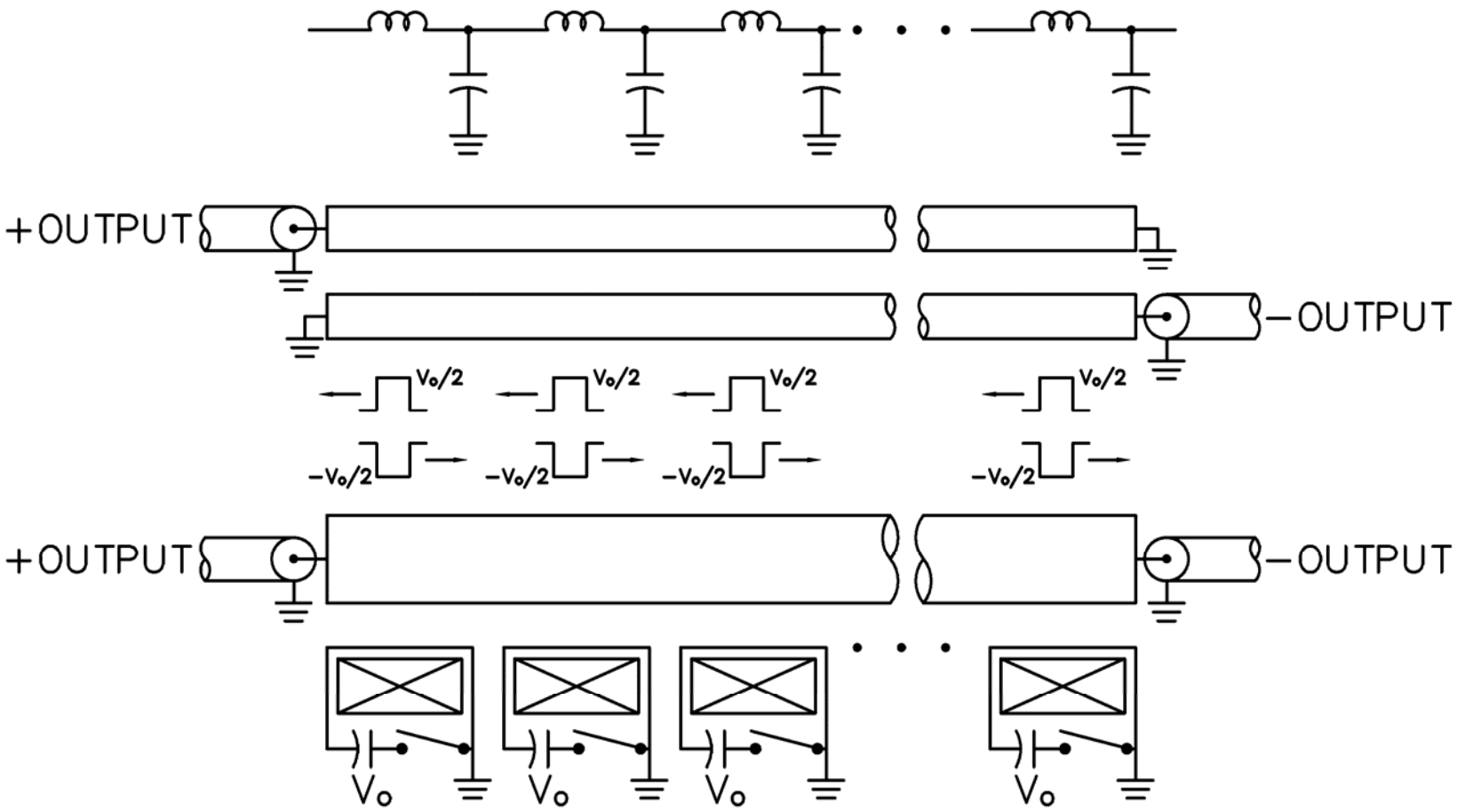




Pulse-to-Pulse Stability

- LLNL adders typically reset/recharge between bursts
  - 3000 pulses, ~3 ns $\rightarrow$ 9 μ s
  - ~1 kV $\rightarrow$ ~10^{-2} V•s (Alt: use remnant flux)
  - ~400 A $\rightarrow$ ~4 mC
- First Point Scientific adders reset/recharge between pulses
  - Minimum voltage on load α 1/D.F.

Transmission Line Effects



Summary

- SLAC/LLNL program is designed to demonstrate *Full System Architecture* for a High Availability Damping Ring Kicker System
- Inductive adder modulator topology
  - Inherently redundant
  - Mature technology
  - Demonstrated over wide range of parameters
- Focus of SLAC/LLNL program is advanced development areas required to meet ILC parameters
  - Short-pulse prototype
  - Timing, calibration, and controls
  - System testing