SCIPP R&D on Long Shaping-Time Electronics

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Bruce Schumm

The SCIPP/UCSC ILC HARDWARE GROUP

Faculty/Senior	Post-Docs	Students
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Alex Grillo		Glenn Gray
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Abe Seiden		

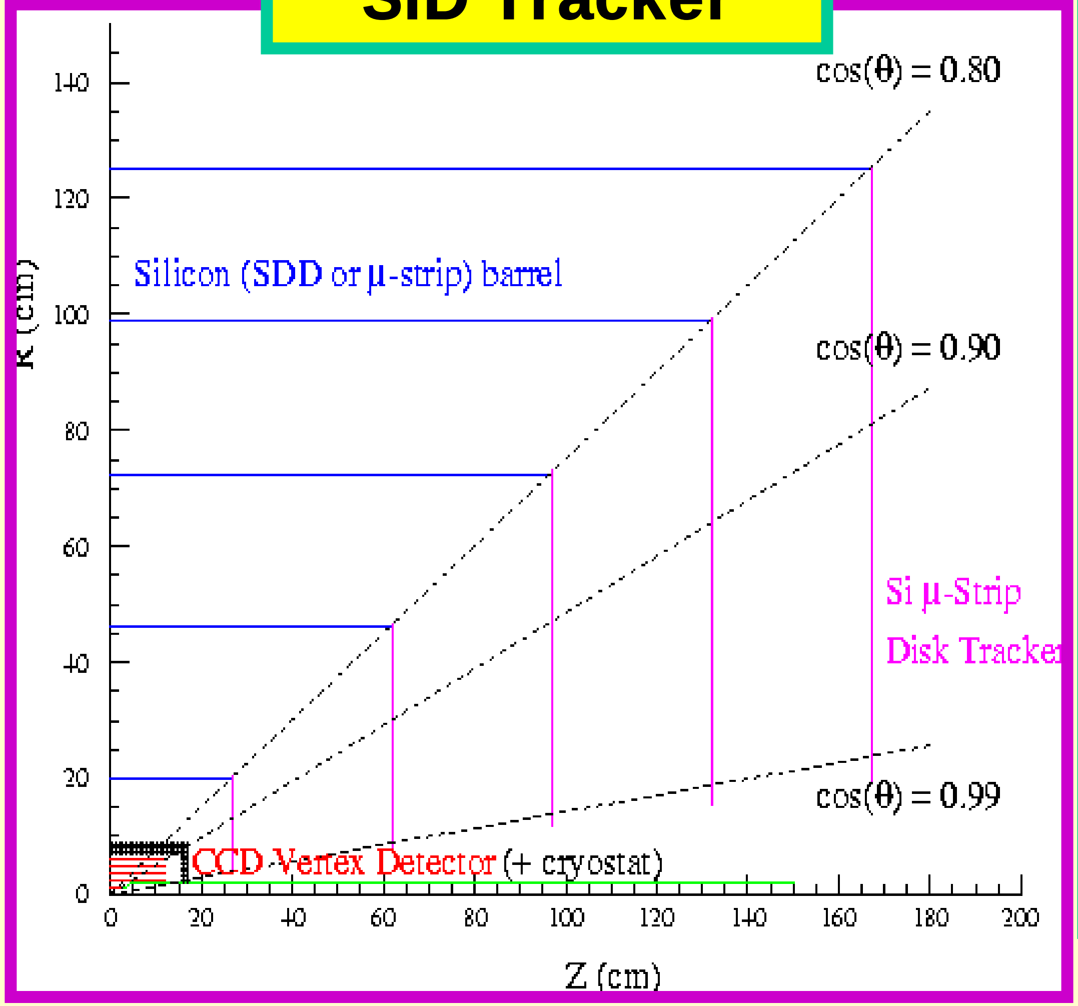
Lead Engineer: Ned Spencer

Technical Staff: Max Wilder, Forest Martinez-McKinney

(Students are undergraduates from physics and engineering)

Silicon Microstrip Readout R&D

SiD Tracker



Initial Motivation

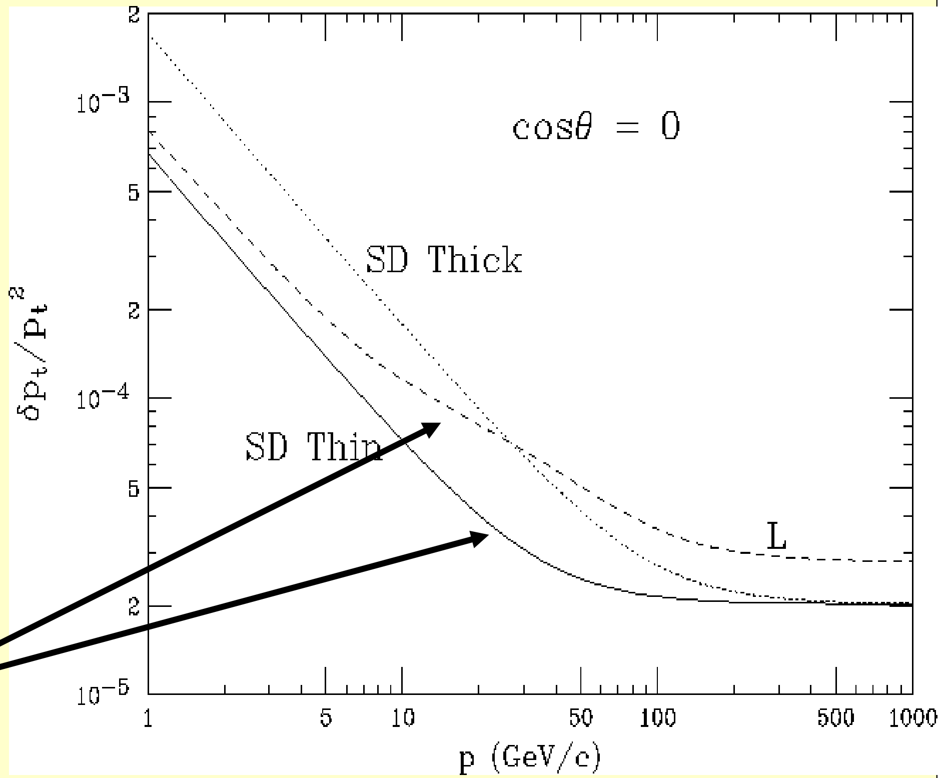
Exploit long shaping time (low noise) and power cycling to:

- Remove electronics and cabling from active area (long ladders)
- Eliminate need for active cooling

The Gossamer Tracker

Ideas:

- Low noise readout ➔ Long ladders ➔ substantially limit electronics readout and support
- Thin inner detector layers
- Exploit duty cycle ➔ eliminate need for active cooling



Competitive with gaseous tracking over full range of momentum (also: **forward region**)

Alternative: shorter ladders, but better point resolution

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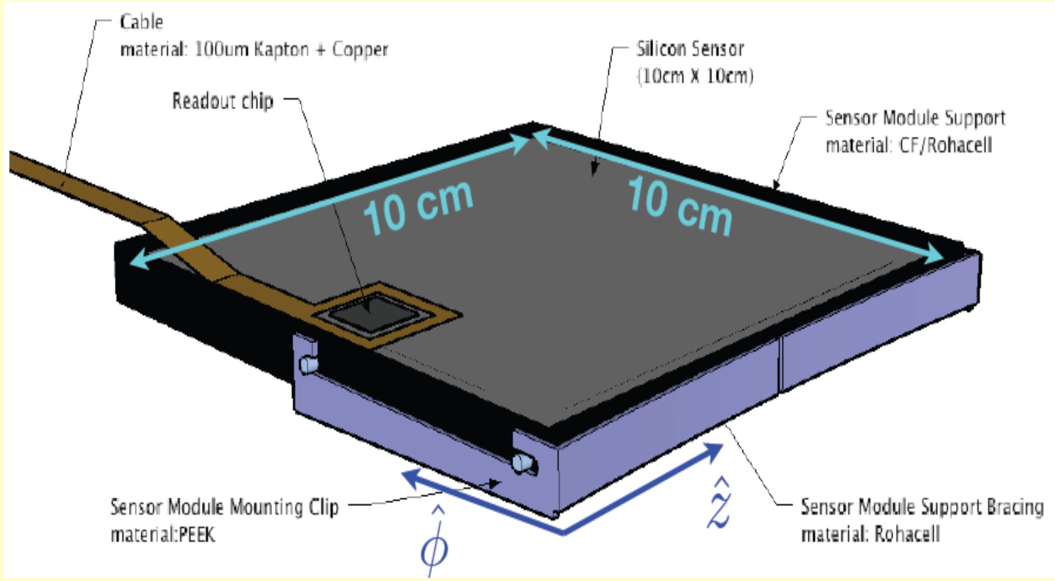
The LSTFE approach would be well suited to use in short-strip applications, and would offer several potential advantages relative to other approaches

- Optimized for LC tracking (less complex)
- More efficient data flow
- No need for buffering



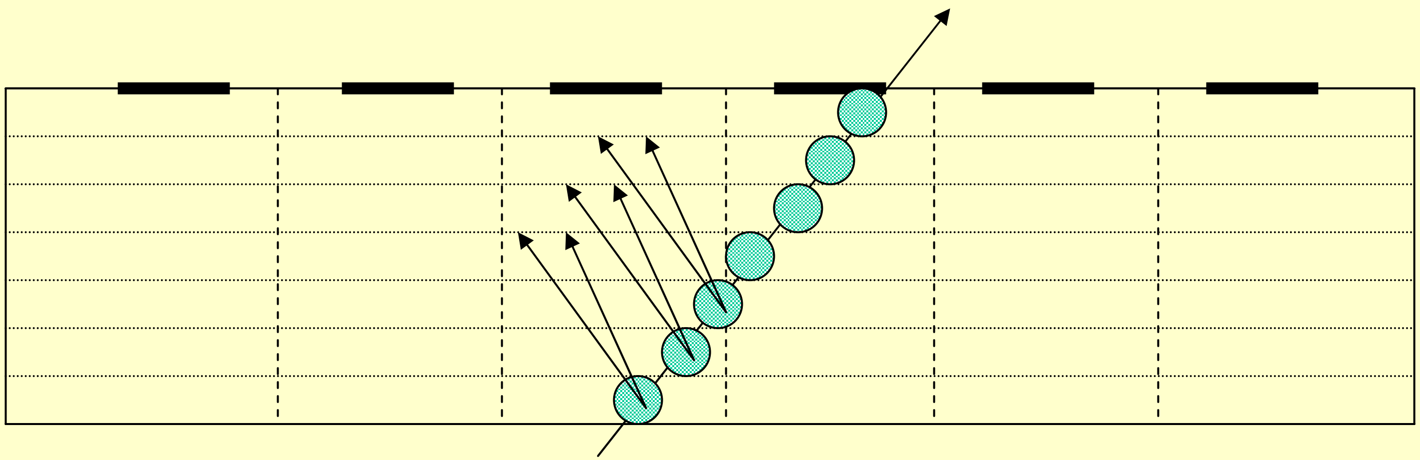
Would require development of 2000 channel chip w/ bump bonding (should be solved by KPiX development)

Pulse Development Simulation

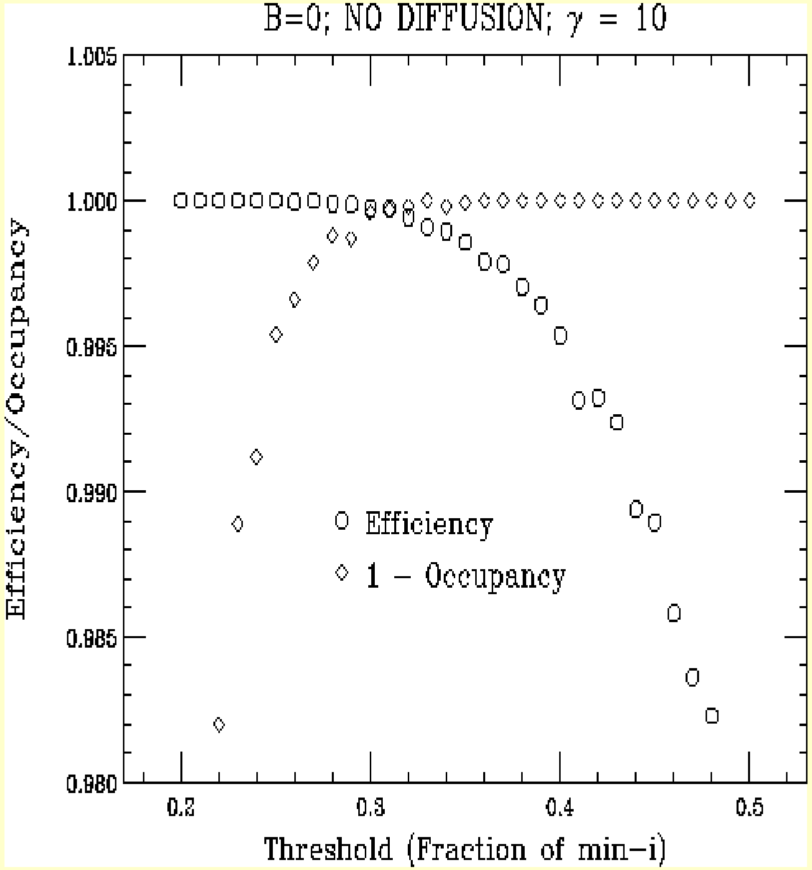
Christian Flacco & Michael Young (Grads); John Mikelich (Undergrad)

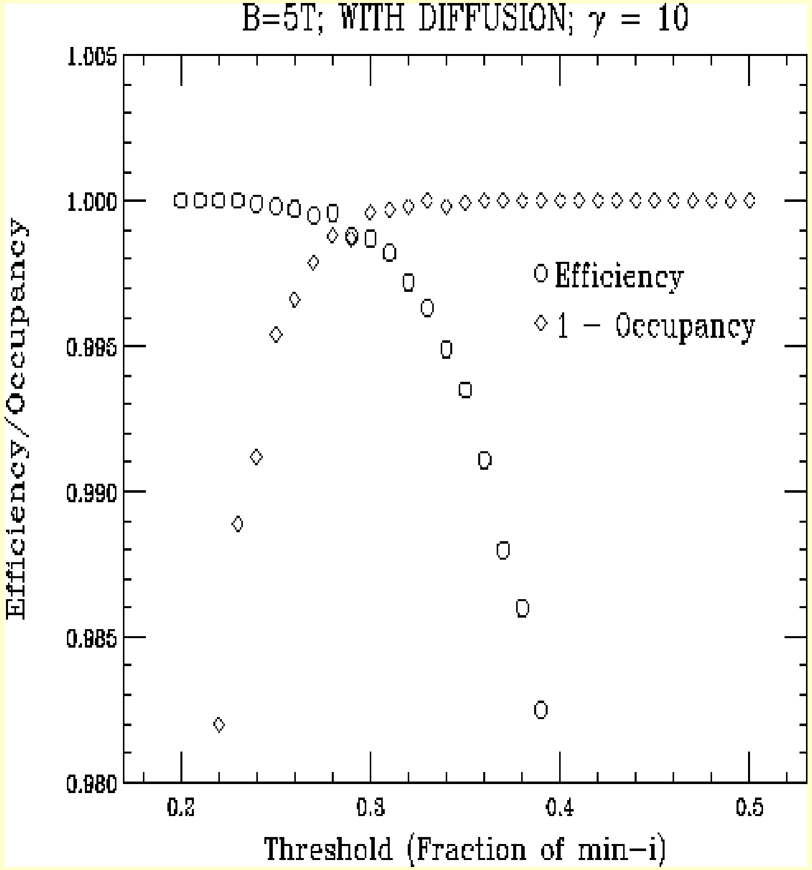
Long Shaping-Time Limit: strip sees signal if and only if hole is collected onto strip (no electrostatic coupling to neighboring strips)

Include: Landau deposition (SSSimSide; Gerry Lynch LBNL), variable geometry, Lorentz angle, carrier diffusion, electronic noise and digitization effects



Result: S/N for 167cm Ladder

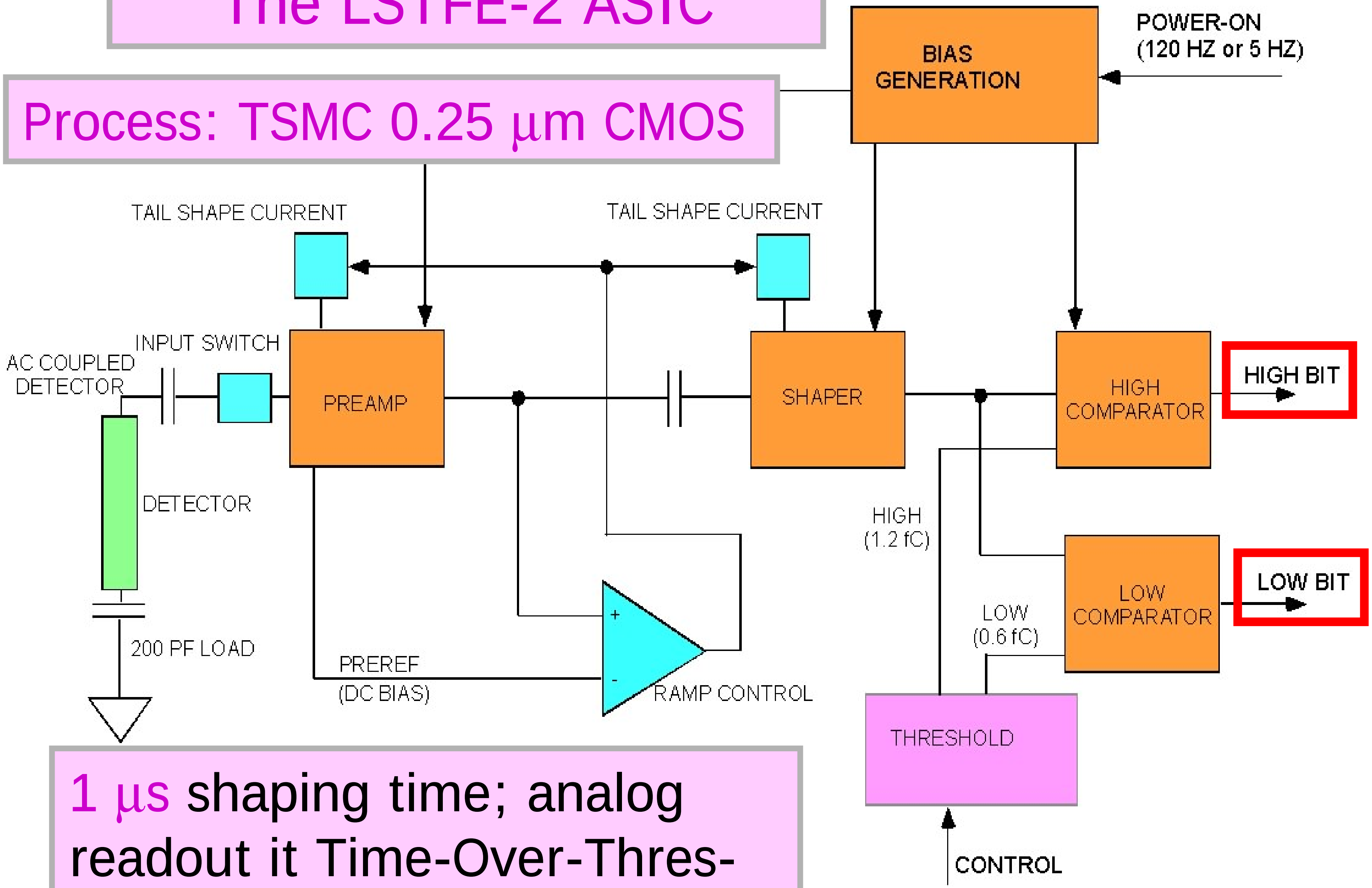




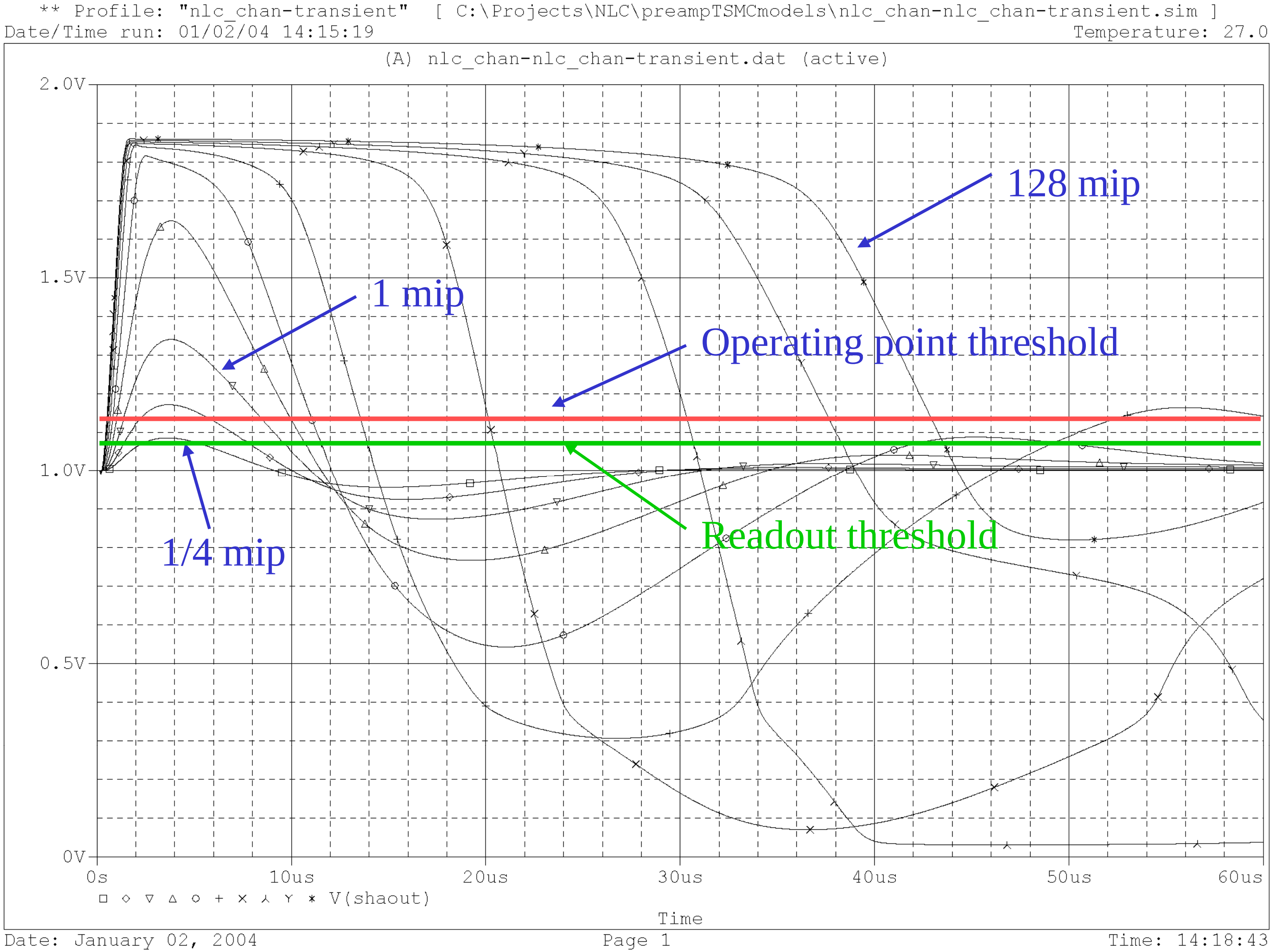
Simulation suggests that long-ladder operation is feasible

The LSTFE-2 ASIC

Process: TSMC 0.25 μm CMOS



1 μs shaping time; analog readout it Time-Over-Threshold with 400 nsec clock


** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim]
Date/Time run: 01/02/04 14:15:19
Temperature: 27.0
(A) nlc_chan-nlc_chan-transient.dat (active)
2.0V
1.5V
1.0V
0.5V
0V
0s
10us
20us
30us
40us
50us
60us
V(shaout)
Time
128 mip
1 mip
Operating point threshold
Readout threshold
1/4 mip
Date: January 02, 2004
Page 1
Time: 14:18:43

Electronics Simulation

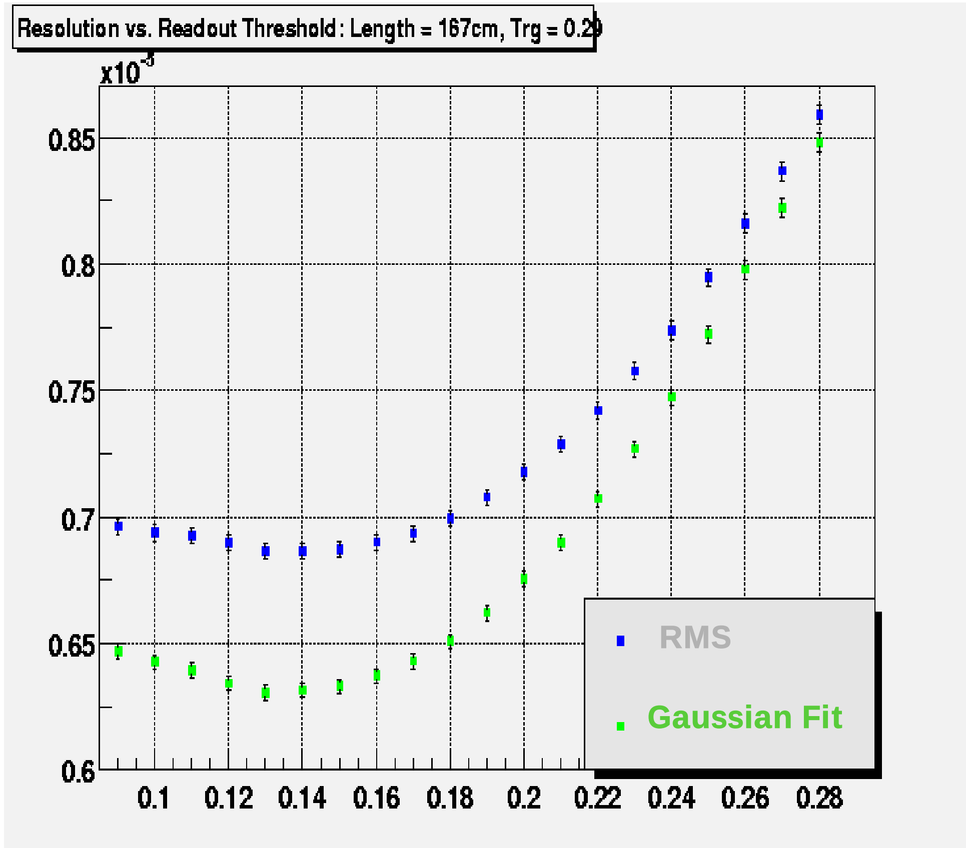
Detector Noise:

From SPICE simulation, normalized to bench tests with GLAST electronics

Analog Measurement:

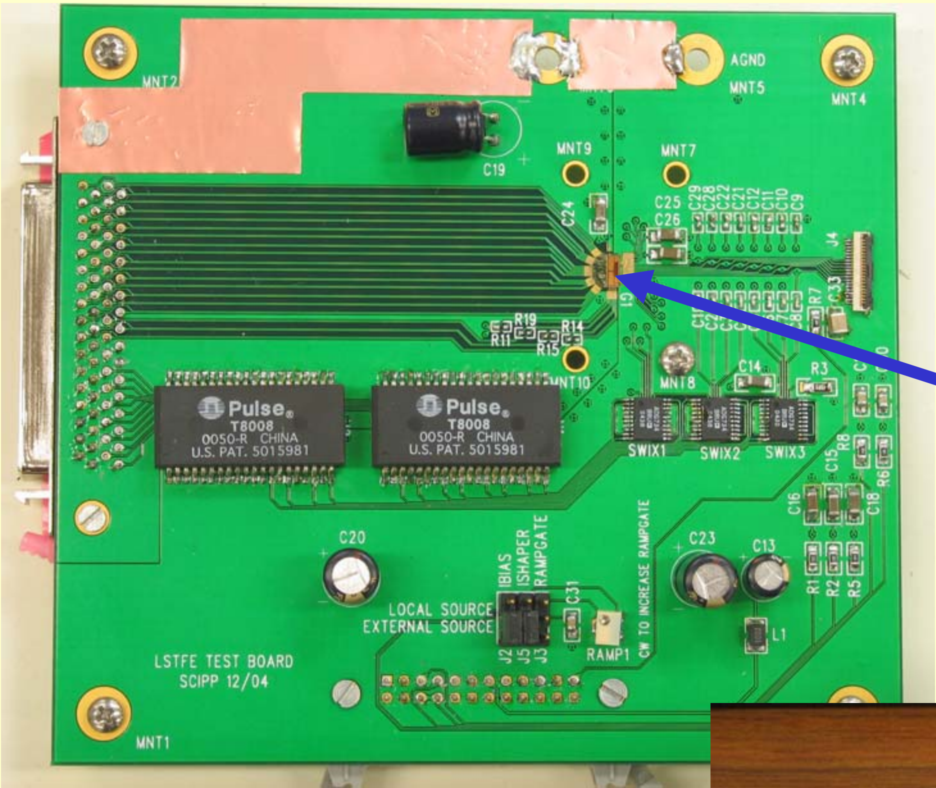
Employs time-over-threshold with variable clock speed; lookup table provides conversions back into analog pulse height (as for actual data)

Essential tool for design of front-end ASIC

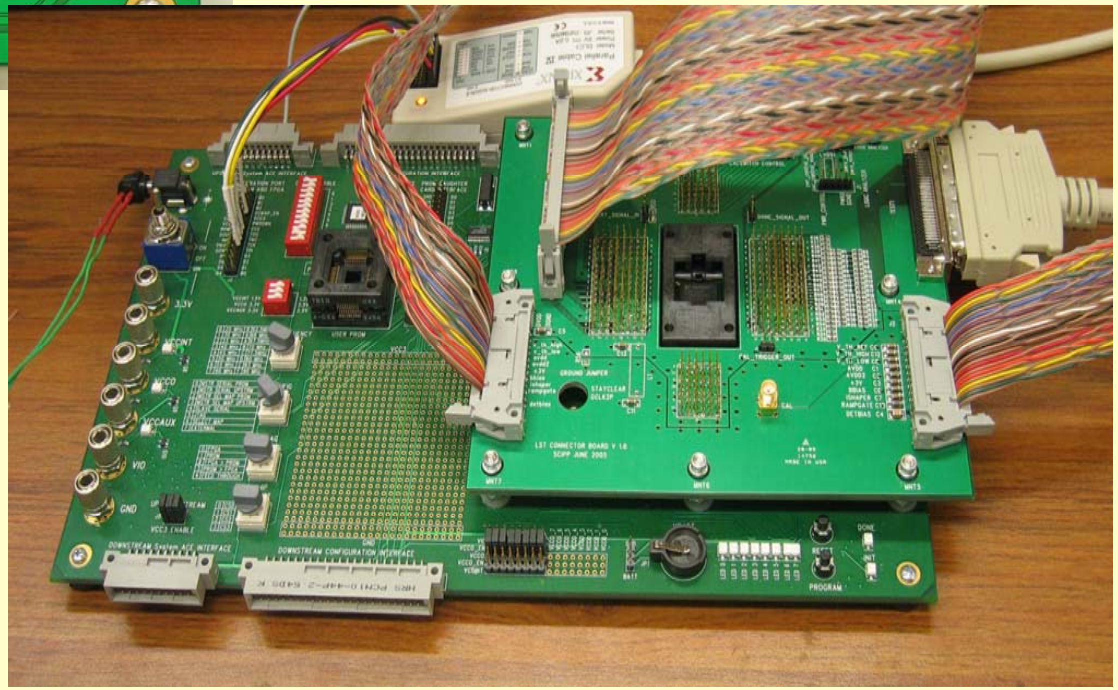


Detector Resolution (units of 10μm)

INITIAL RESULTS



LSTFE-2 chip mounted on readout board



FPGA-based control and data-acquisition system

Note About LSTFE-2 Shaping Time

Original target: τ_{shape} = 3 μsec, with some controlled variability ("ISHAPR")
➔Appropriate for long (2m) ladders

In actuality, τ_{shape} ~ 1.5 μsec; tests done at 1.2 μsec, closer to optimum for SLAC short-ladder approach

Difference between target and actual shaping time understood in terms of simulation (full layout)

Comparator S Curves

Vary threshold for given input charge

Read out system with FPG-based DAQ

Get

```
1-erf(threshold)
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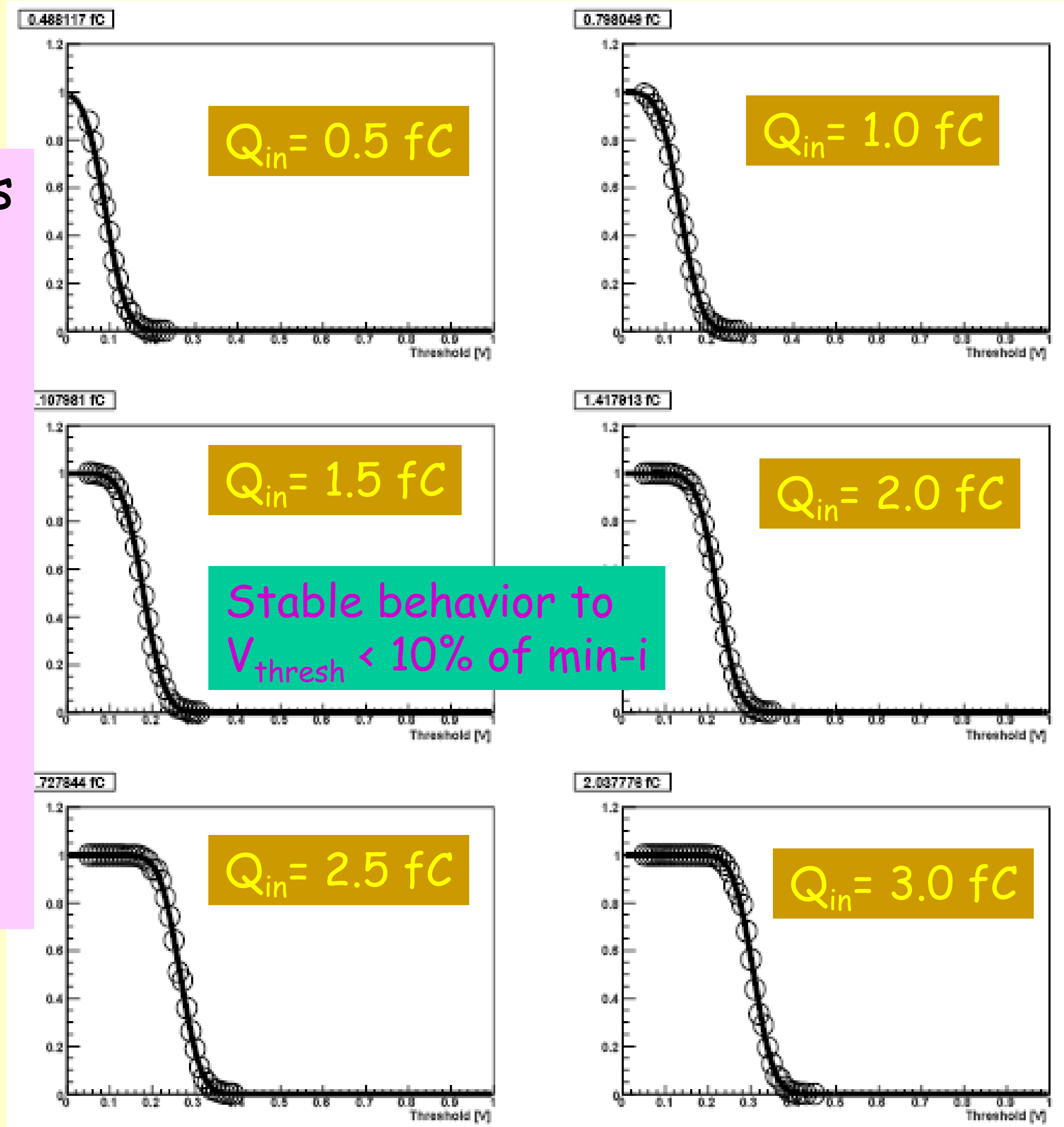
with 50% point giving response, and width giving noise



Noise vs. Capacitance
(at τ_{shape} = 1.2 μs)

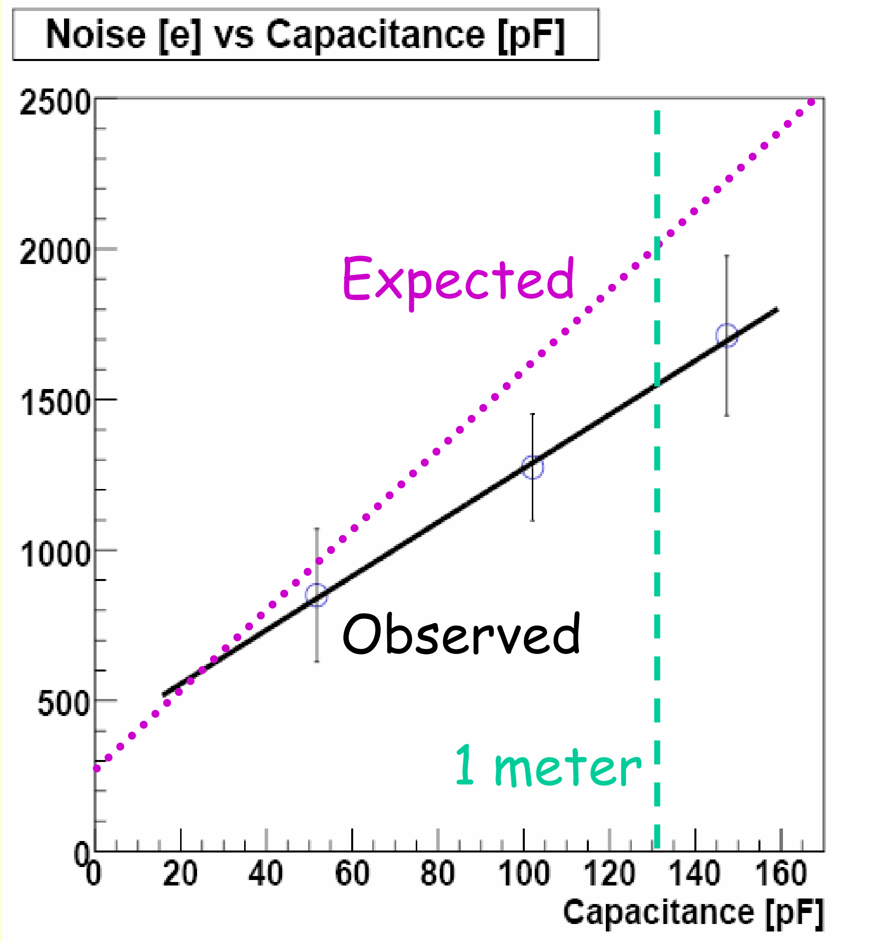
Measured dependence is roughly
(noise in equivalent electrons)

$$\sigma_{noise} = 375 + 8.9*C$$

with C in pF.

Experience at 0.5 μm had suggested that model noise parameters needed to be boosted by 20% or so; these results suggest 0.25 μm model parameters are accurate

➔ Noise performance somewhat better than anticipated.



Power Cycling

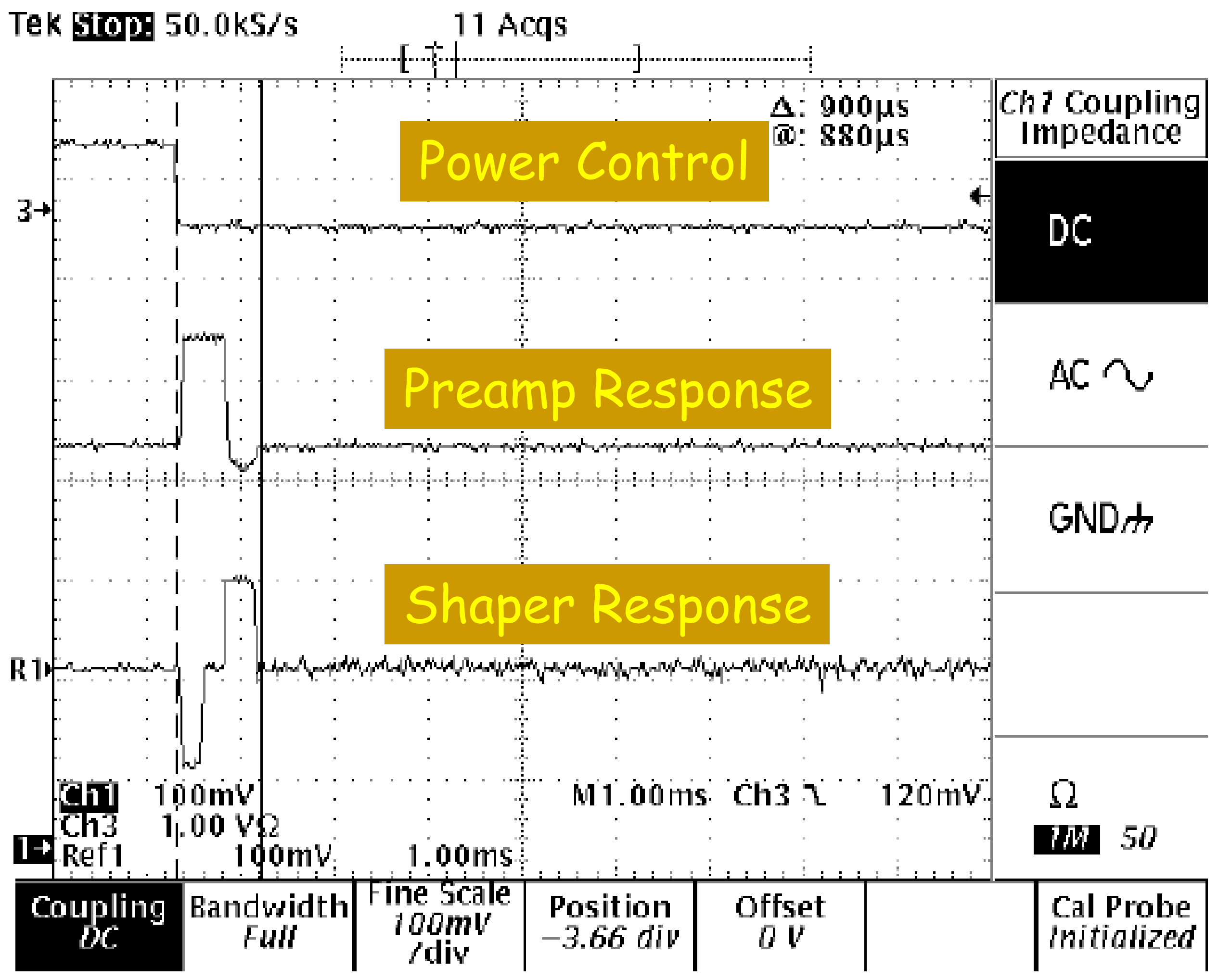
Idea (roughly): Latch operating bias points and isolate chip from outside world.

- Per-channel power consumption reduces from ~1 mW to ~10 μW.
- Restoration to operating point should take ~ 1 msec.

Current status:

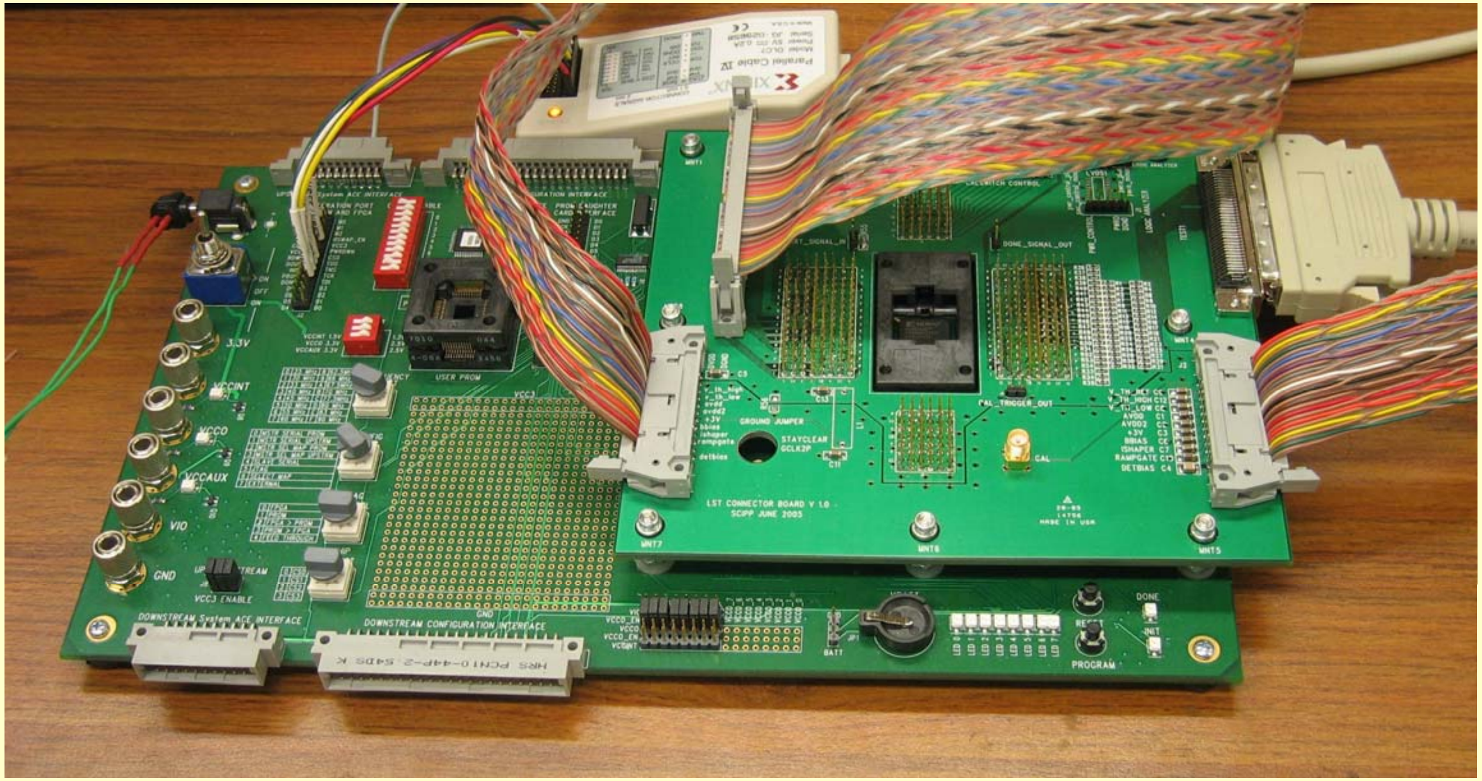
- Internal leakage (protection diodes + ?) degrades latched operating point
- Restoration takes ~40 msec (x5 power savings)
- Injection of small current (< 1 nA) to counter leakage allows for 1 msec restoration.
- Current focus of bench tests.

Power Cycling with Small Injected Current



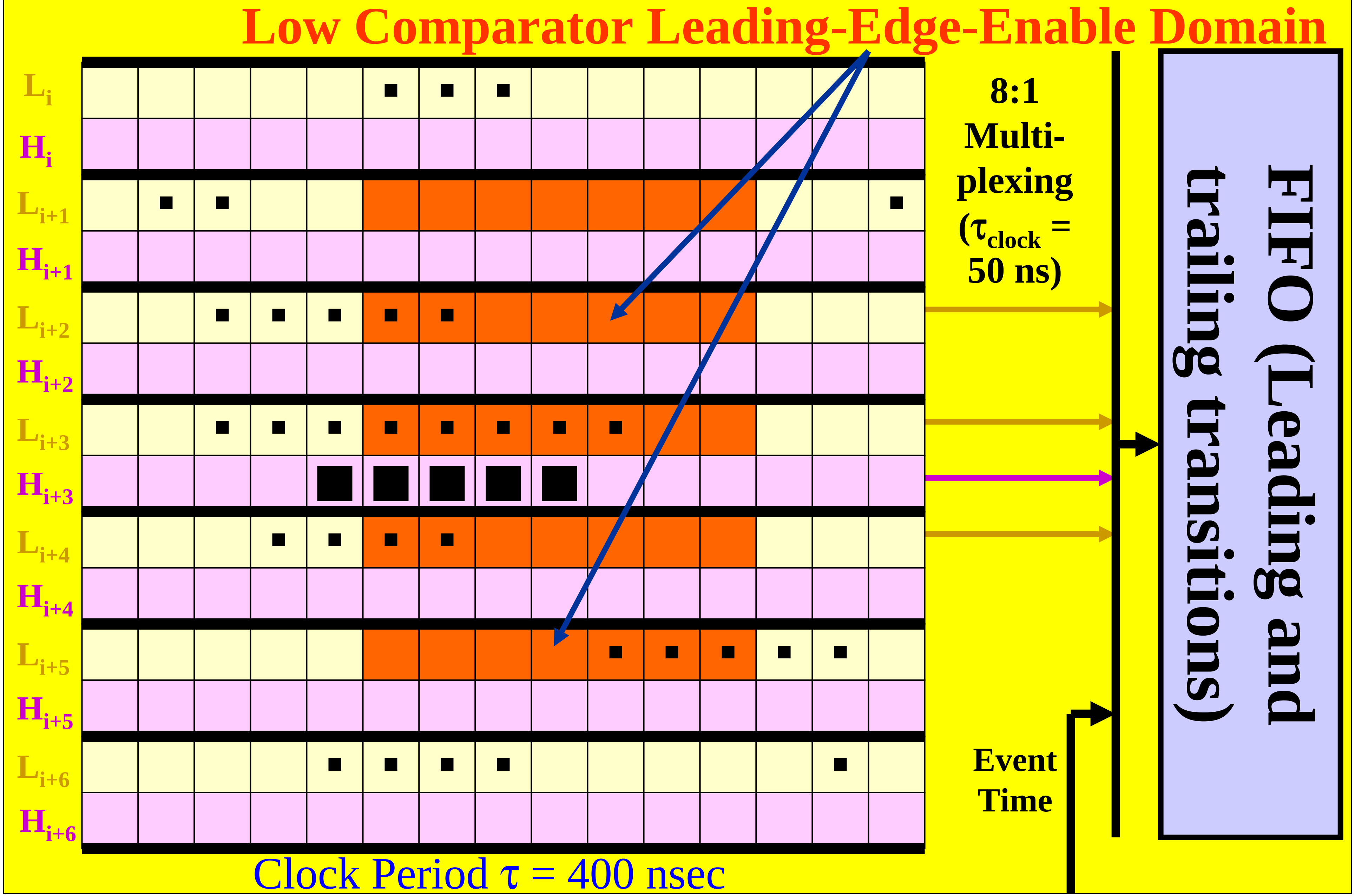
Need to determine whether leakage problem is fundamental (to substrate) or not (protection diode leakage) to understand if we can design around the leakage. Another (vastly inferior) approach would be to design in an injected current (process/temp variation?

DIGITAL ARCHITECTURE: FPGA DEVELOPMENT



Digital logic should perform basic zero suppression (intrinsic data rate for entire tracker would be approximately 50 GHz), but must retain nearest-neighbor information for accurate centroid.

Proposed LSTFE Back-End Architecture



Note on LSTFE Digital Architecture

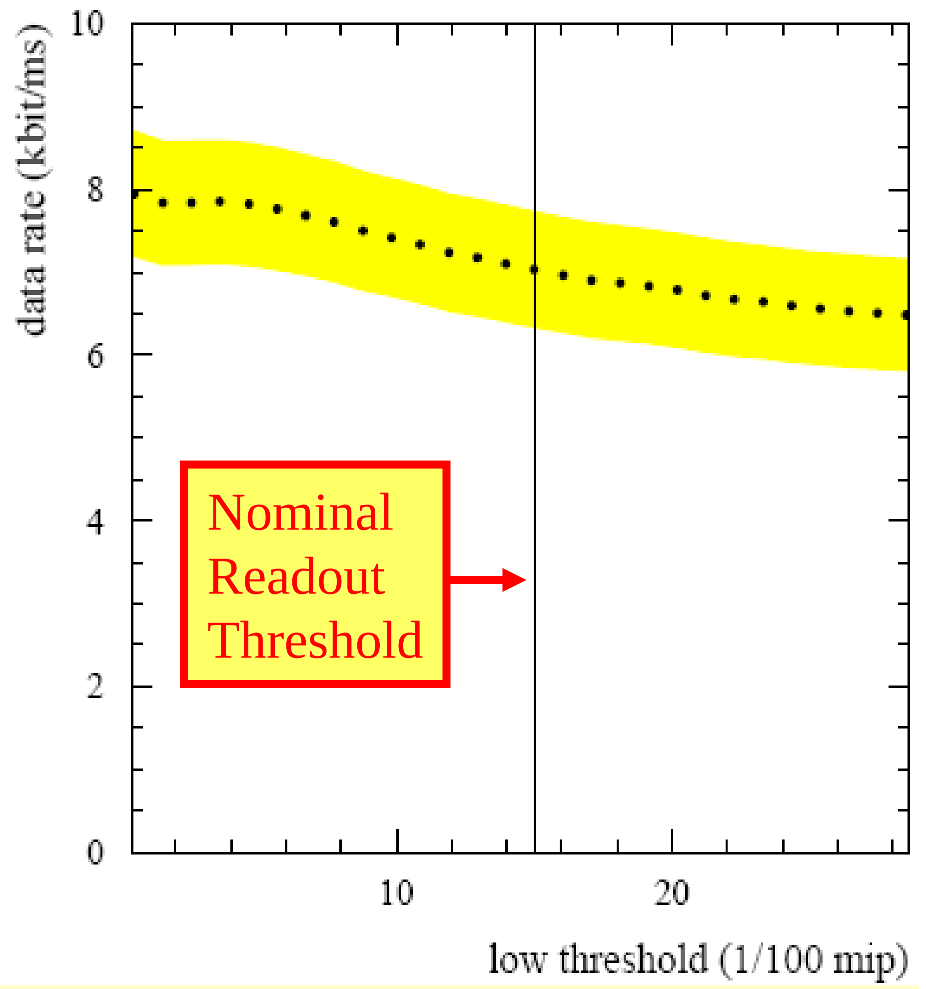
Use of time-over-threshold (vs. analog-to-digital conversion) permits real-time storage of pulse-height information.

➔ No concern about buffering

➔ LSTFE system can operate in arbitrarily high-rate environment; is ideal for (short ladder) forward tracking systems.

DIGITAL ARCHITECTURE VERIFICATION

ModelSim package permits realistic simulation of FPGA code (signal propagation not yet simulated)

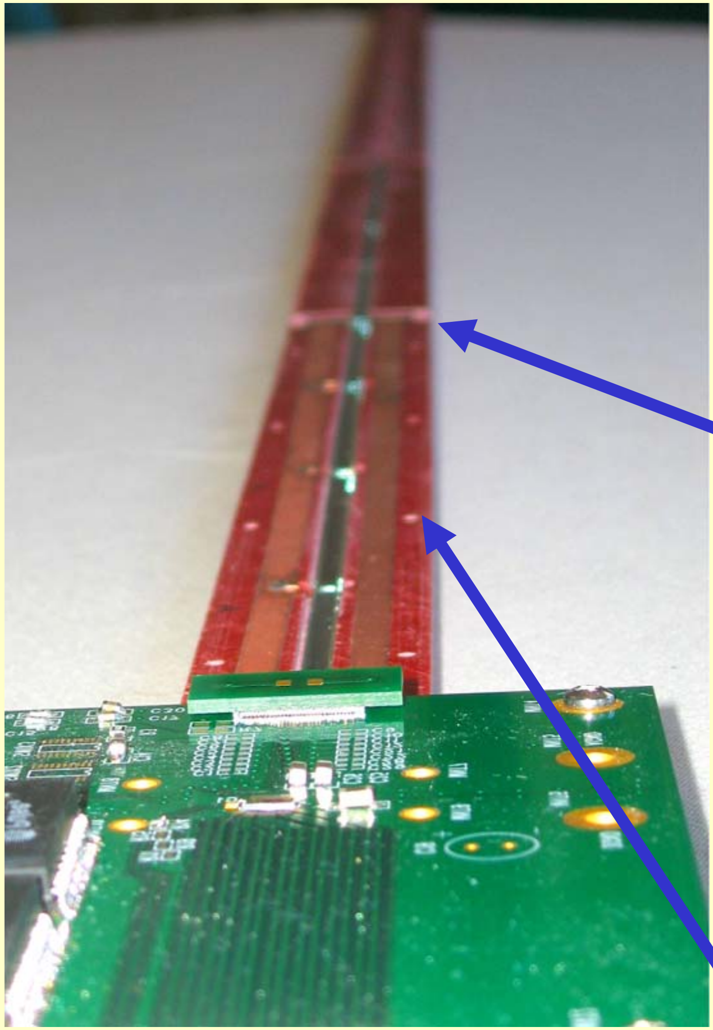


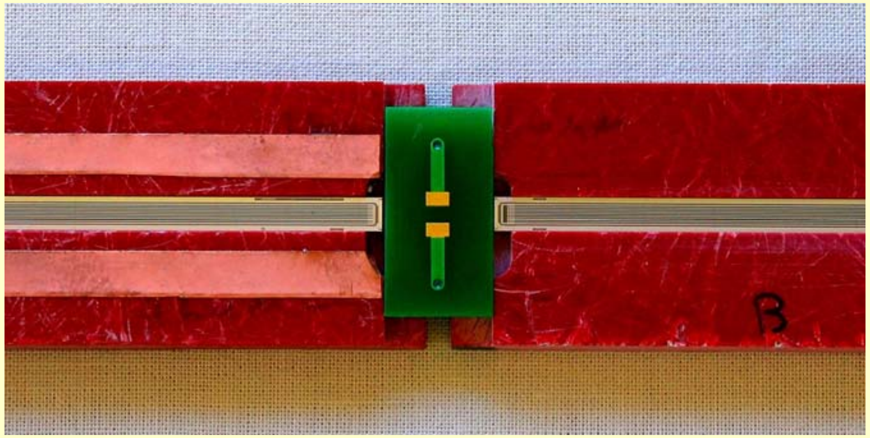
Simulate detector background and noise rates for 500 GeV running, as a function of read-out threshold.

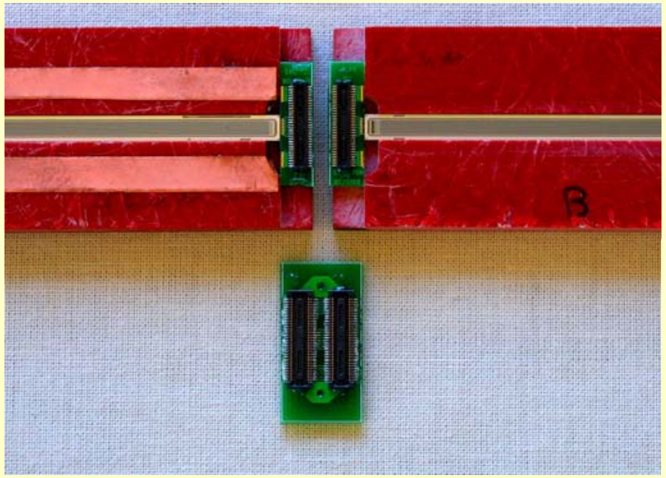
Per 128 channel chip ~ 7 kbit per spill ➔ 35 kbit/second

For entire long shaping-time tracker ~ 0.5 GHz data rate (x100 data rate suppression)

LONG LADDER CONSTRUCTION







LSTFE SUMMARY

The LSTFE readout system is:

- Universally applicable (long strips, short strips, central, forward, SiD, LDC, GLD)
- Specifically and carfully optimized for ILC tracking
- Relative simple (reliability, yield)
- In a relatively advanced stage of development
  - Amplifier/comparator looks functional
  - Headway being made on fast power cycling
  - Digital architecture soon available on FPGA
- Hoping to join SiLC testbeam run in late 2007