

Fast feedback/feedforward systems

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Overview

LCABD: Daresbury, Oxford, (QMUL)

Collaborators: SLAC, KEK, Tokyo Met, DESY, CERN

Task: prototype beam-based (intra-train) feedback system

Completed: ultra-fast analogue feedback prototypes

FONT2 / NLCTA: 54ns latency

FONT3 / ATF: 23ns latency

Ongoing: ILC digital feedback prototypes

FONT4 / ATF: 1st digital FB processor

FONT@ESA: EM background impact on FB BPMs

FONT goals

Prototype components required for ILC intra-train beam feedback system(s):

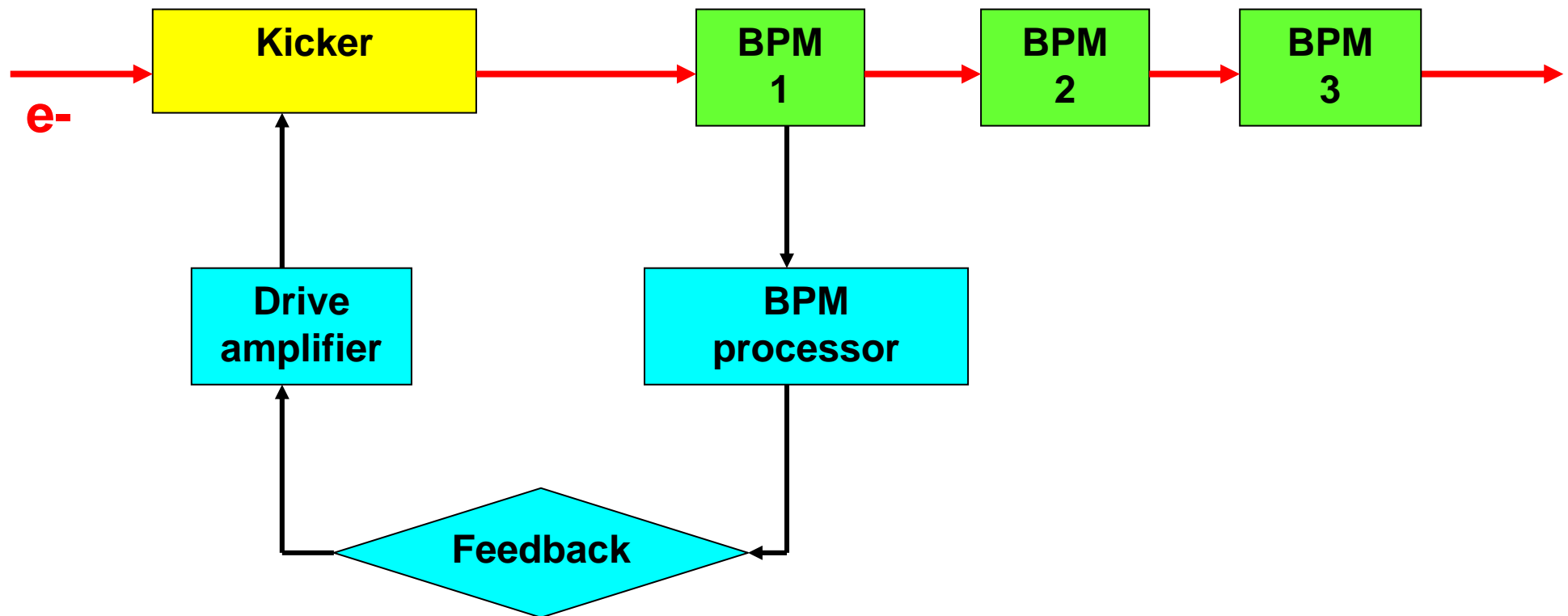
BPMs, signal processor, feedback circuit, amplifier, kicker

and demonstrate **system performance with **real beam****

NB technology applicable more widely through ILC:

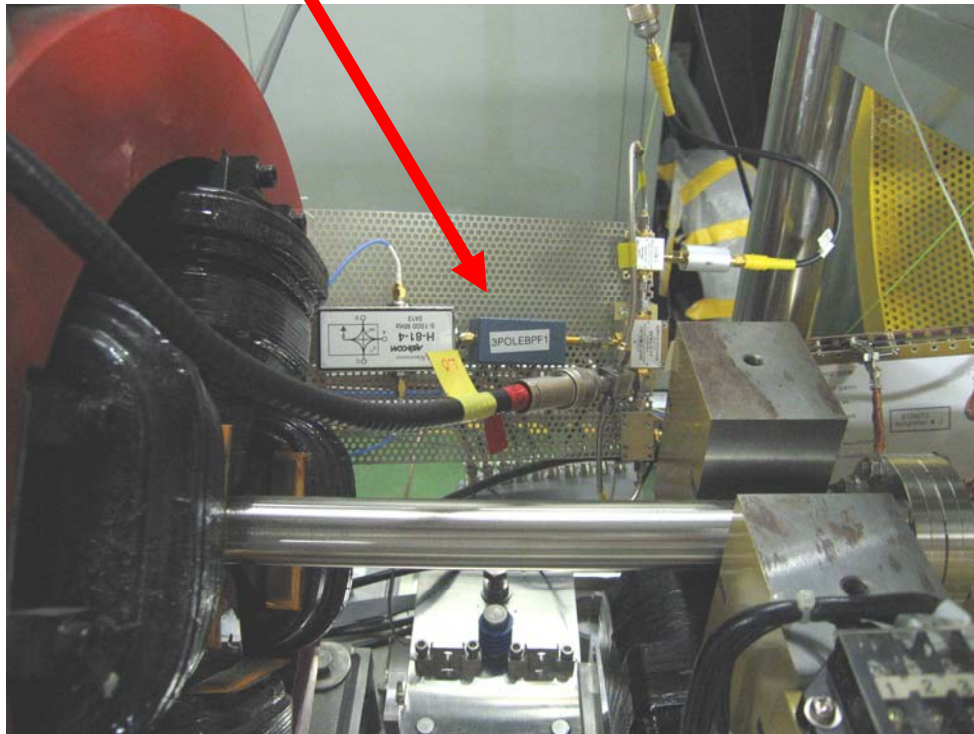
**RTML feed-forward, linac orbit FB,
linac train straightener, BDS orbit FB,
IP pulse-pulse FB ...**

Feedback experiments



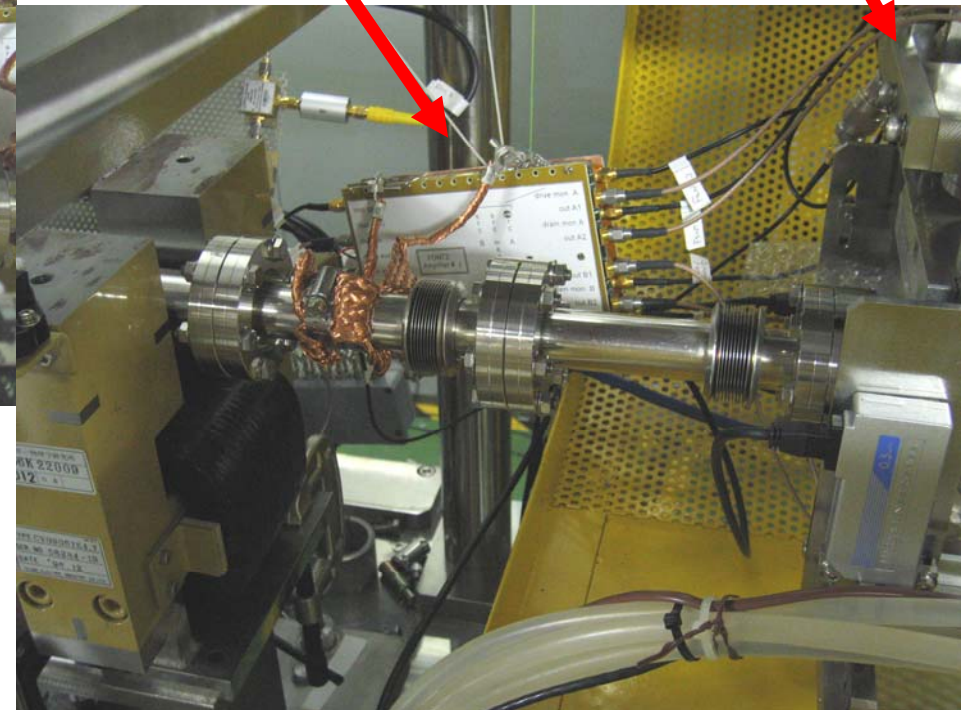
FONT3: beamline at KEK ATF (June 05)

BPM processor board



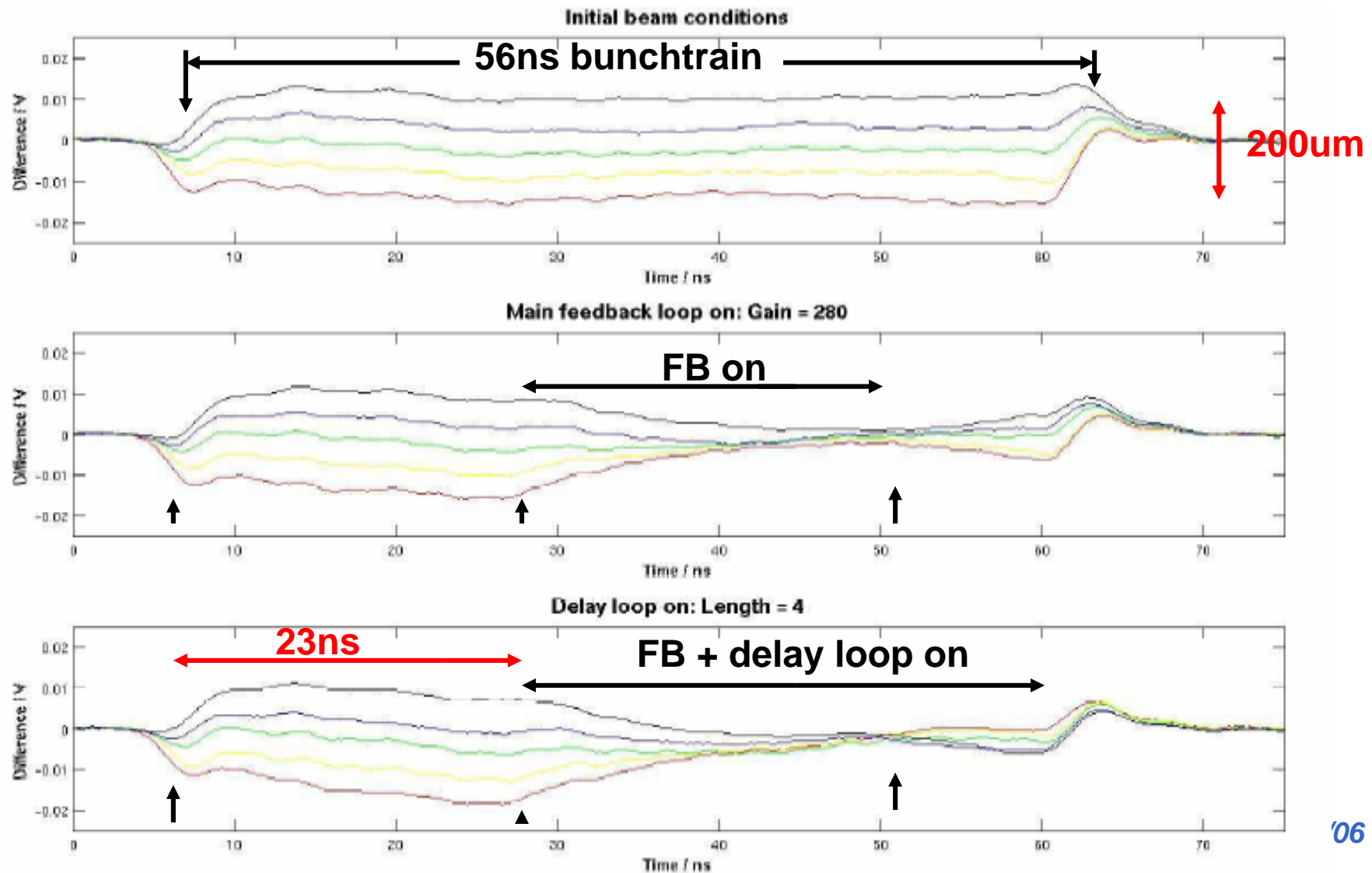
Amplifier/FB board

FEATHER Kicker

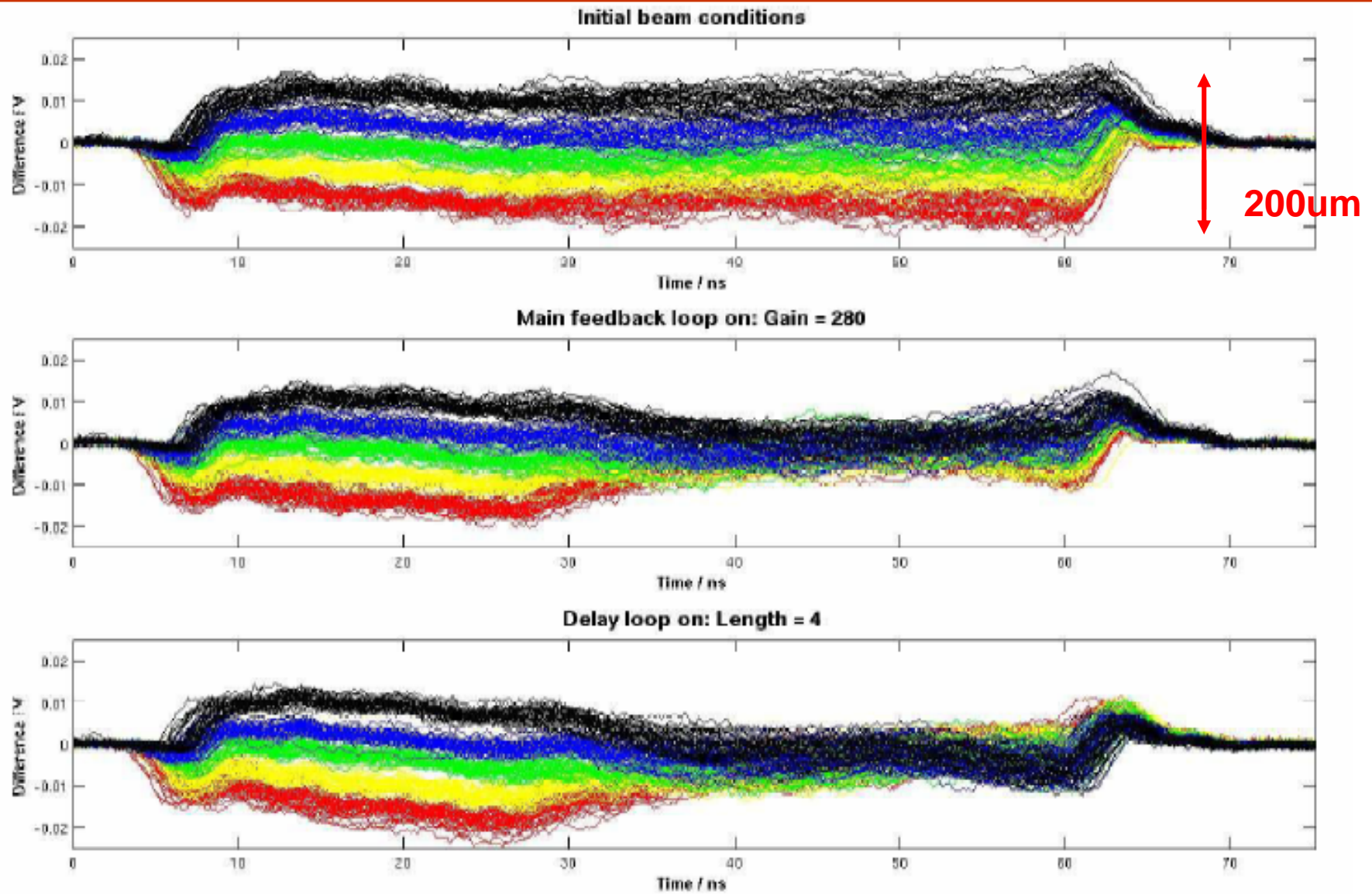


FONT3 position correction performance

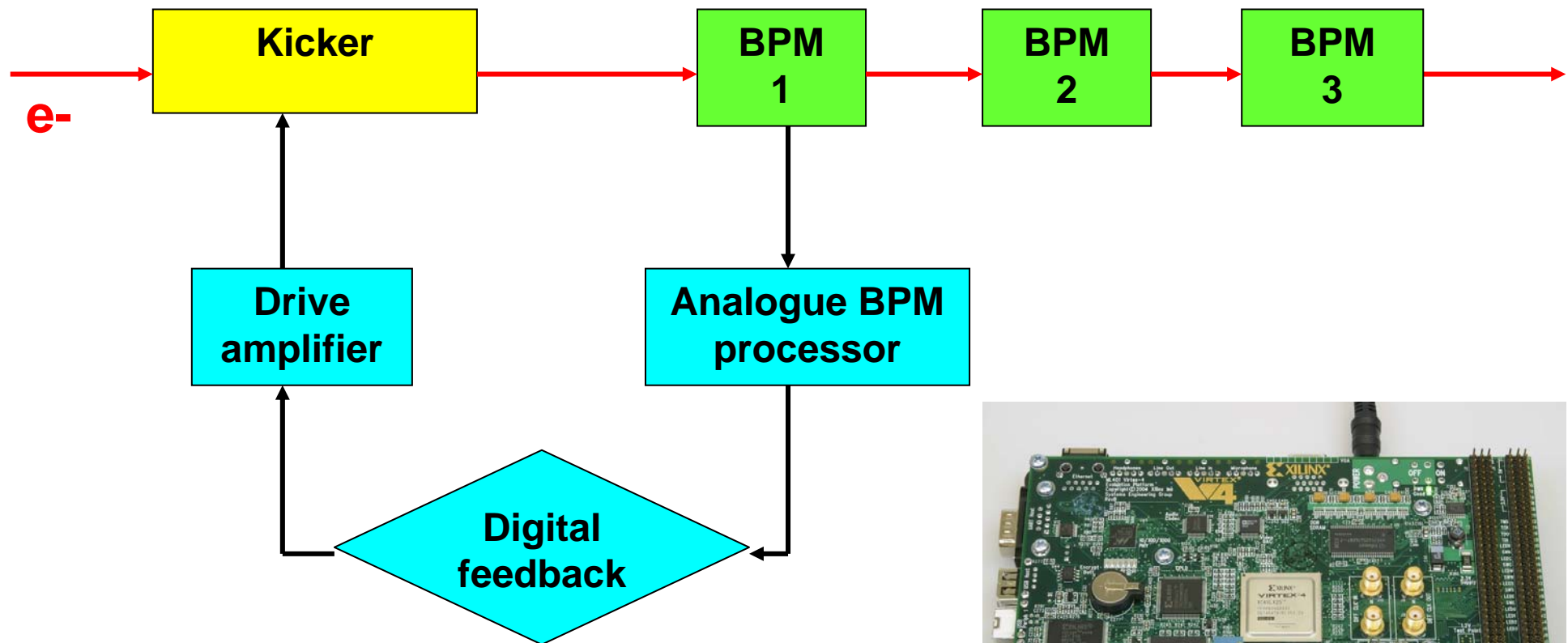
(June 3 2005)



FONT3: raw data (June 3 2005)



ILC digital feedback prototype tests



P.N. Burrows



Digital system test plan

FONT4 (2005-6):

modified FONT3 BPM processor
digital FB processor
solid-state amplifier
adjustable-gap kicker

ATF: initial tests with

3 bunches with spacing c. 150ns

**aiming for latency <120ns (electronics);
stabilisation of 3rd bunch at um level**

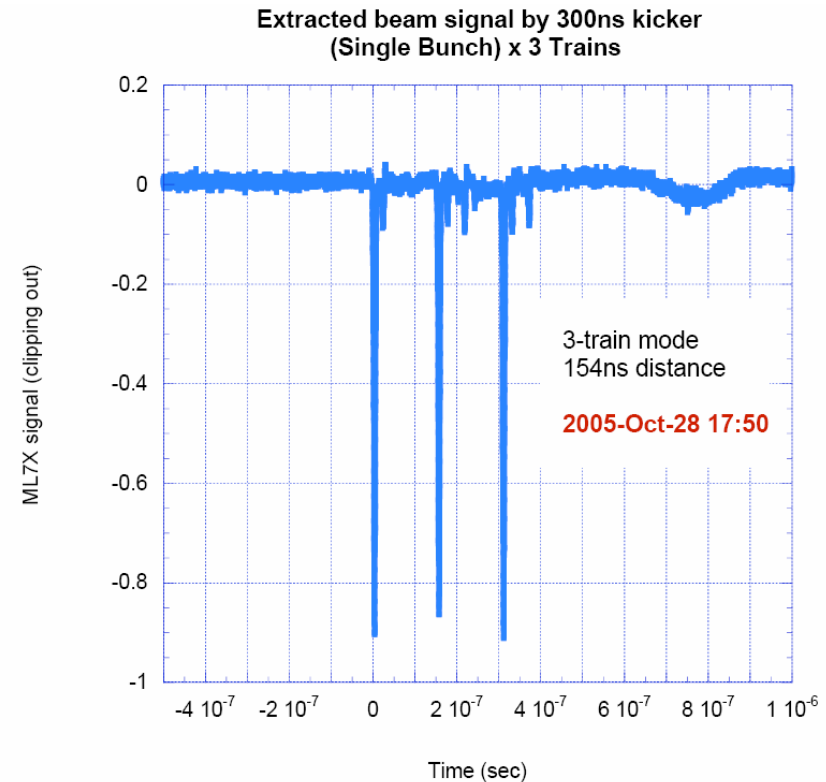
Digital board tests April, June 2006

Closed-loop tests Dec 2006

FONT5 (2008-9):

improved FB system + algorithm development; **+ feed-forward?**
tests with 20-60 bunch trains at ATF(2), or TTF2

P.N. Burrows



ATF2 Project Meeting, KEK, 30/5/06

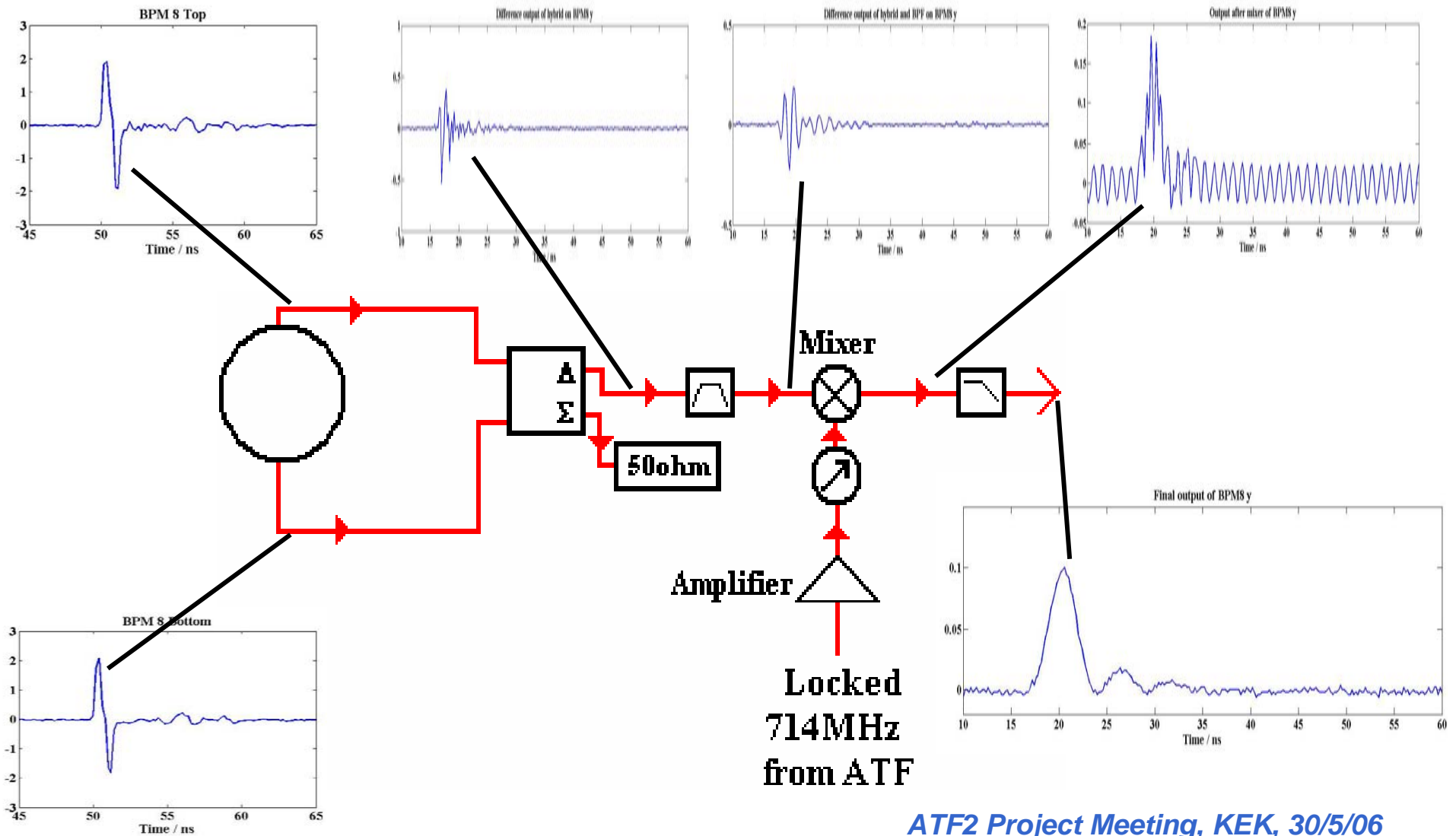
FONT4: latency budget

- Time of flight kicker – BPM: 7ns
- Signal return time BPM – kicker: 15ns
- **Irreducible latency: 22ns**

- BPM processor: 7ns
- ADC/DAC (3.5 89 MHz cycles) 40ns
- Signal processing (8 357 MHz cycles) 25ns
- FPGA i/o 3ns
- Amplifier 40ns
- Kicker fill time 3ns
- **Electronics latency: 118ns**

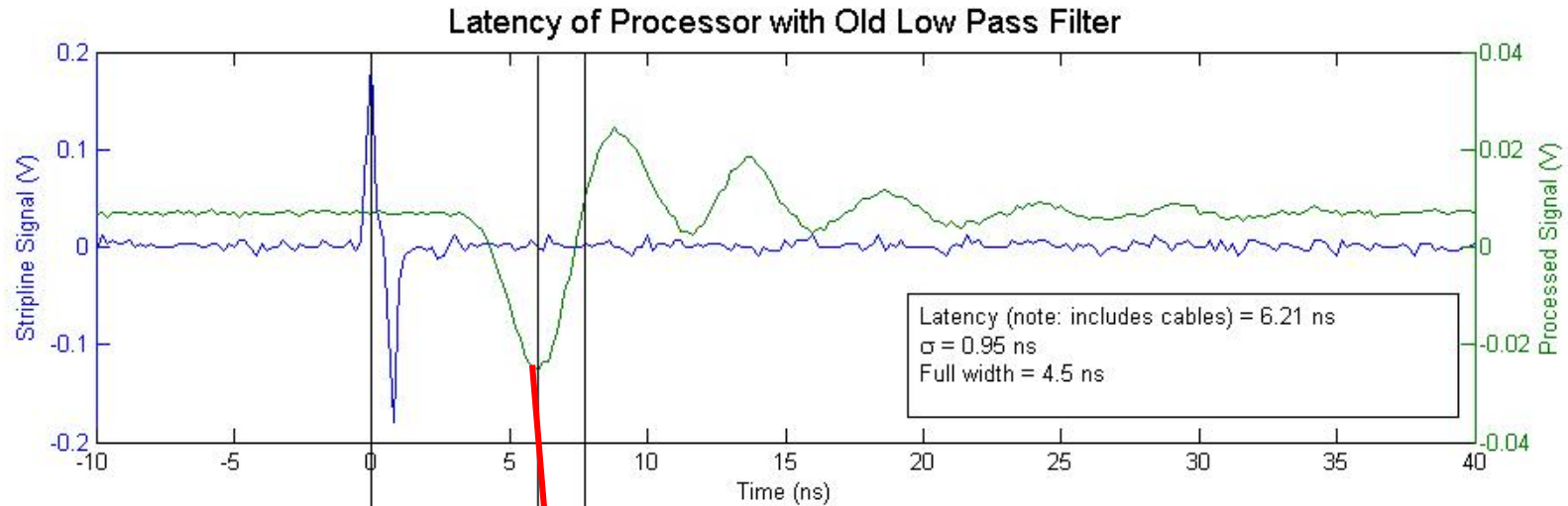
- **Total latency budget: 140ns**

FONT4: BPM analogue signal processor

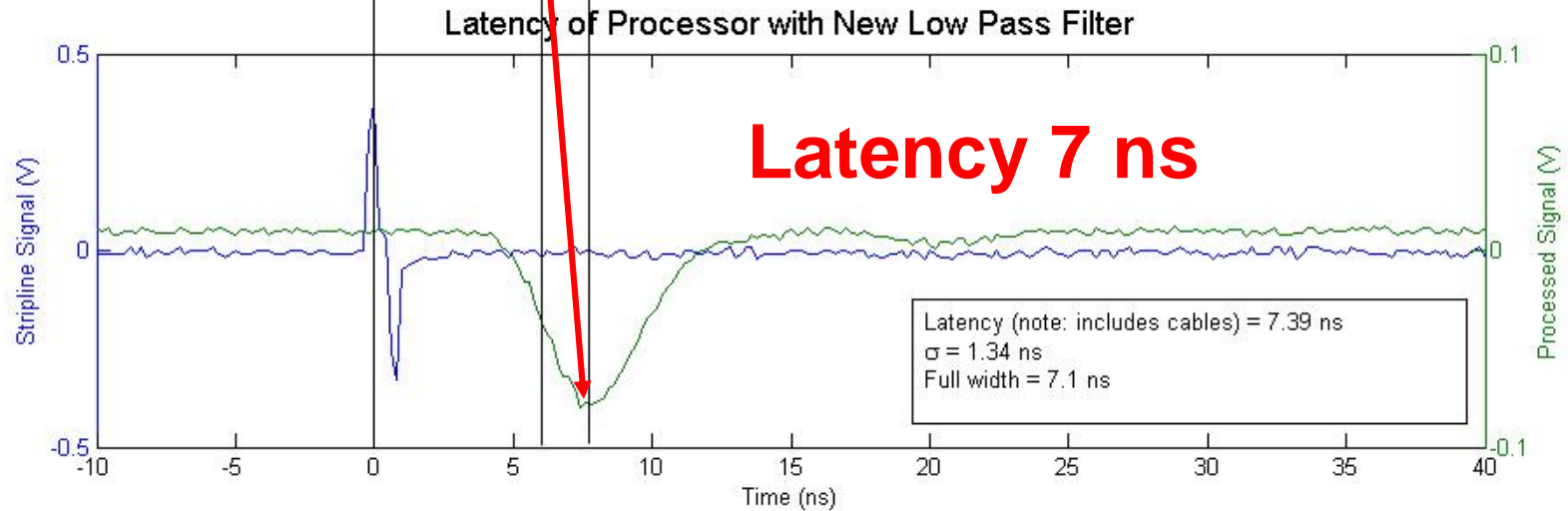


FONT4: BPM processor latency measurement (December 2005)

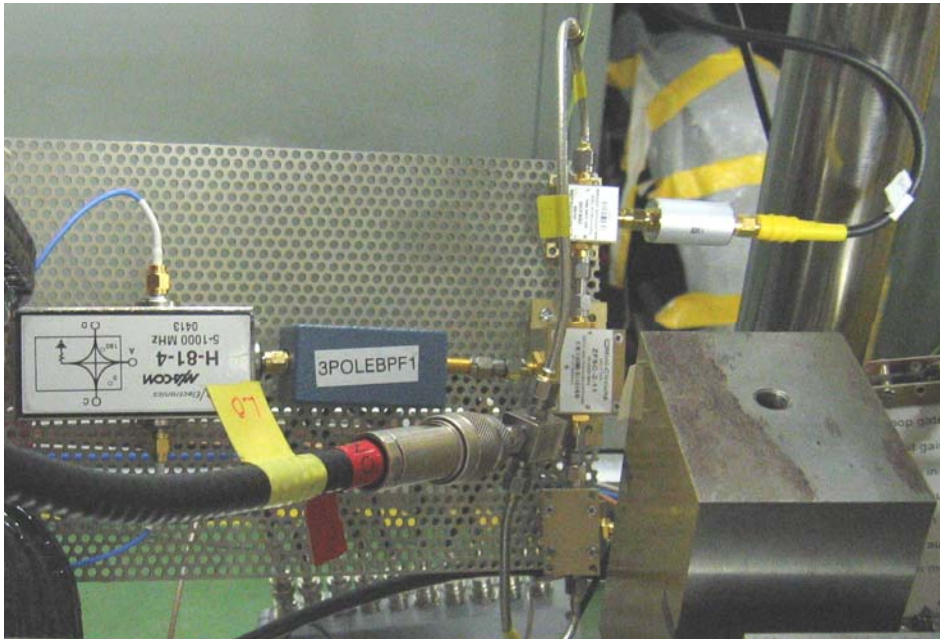
FONT3



FONT4



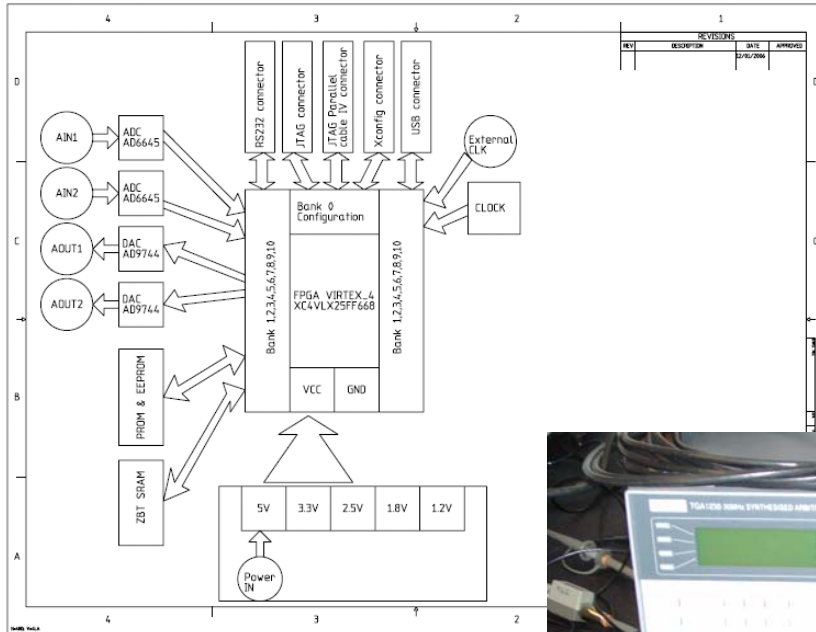
FONT4: new BPM analogue signal processor



**We are replacing
connectorised version
with PCB:**

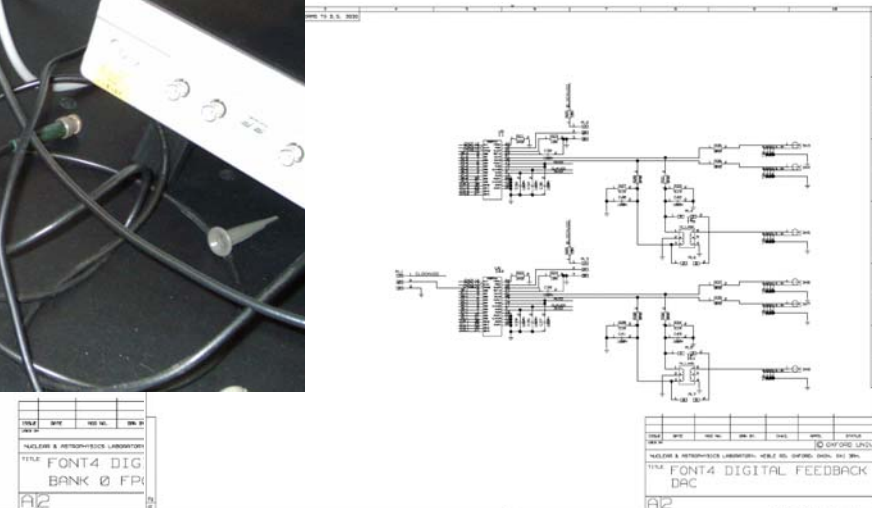
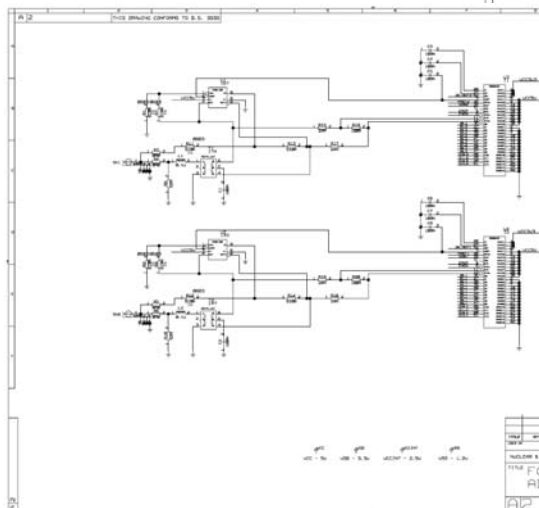
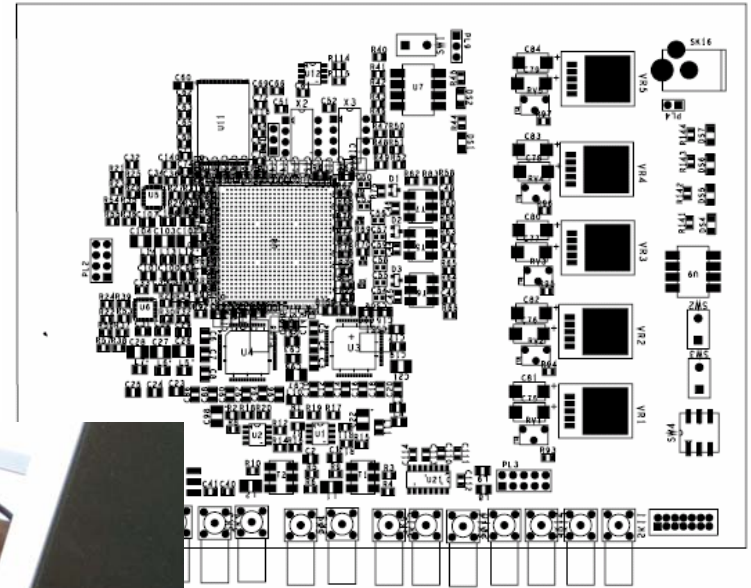
- **Order placed 28/5/06**
- **Boards loaded 5/6/06**
- **Test at ATF 12/6/06**

FONT4: digital feedback processor

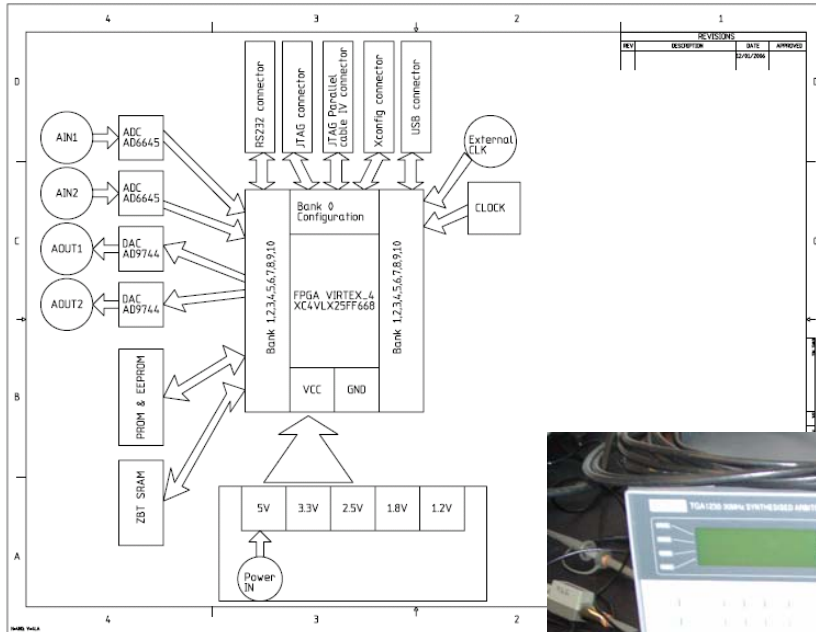


PCB loaded
April 4

Bench tests
April 5-14

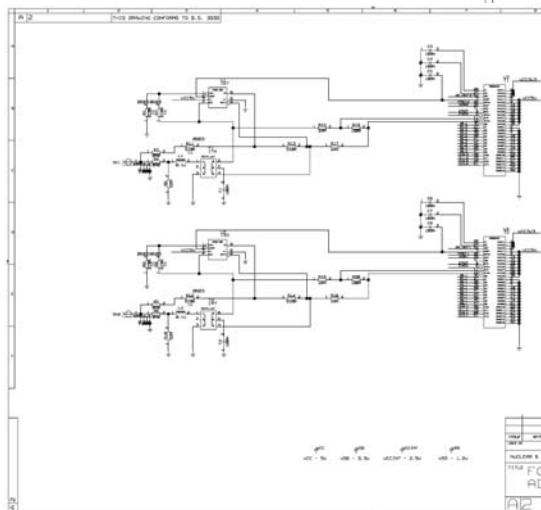
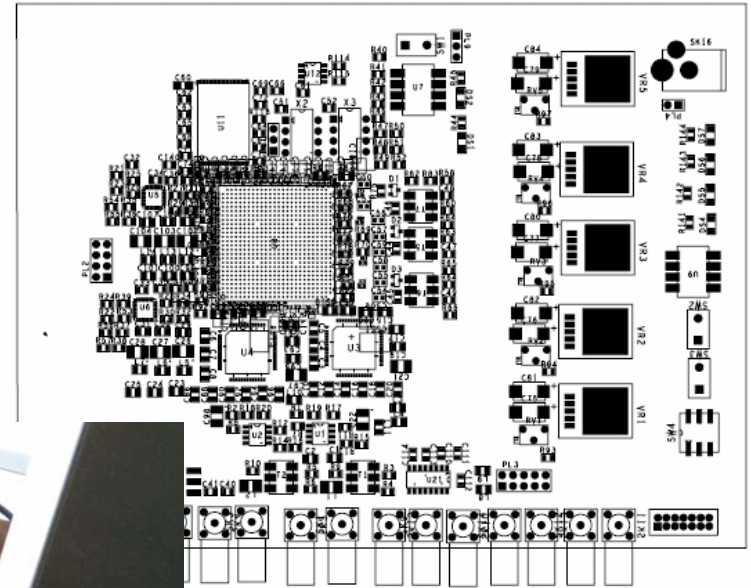


FONT4: digital feedback processor

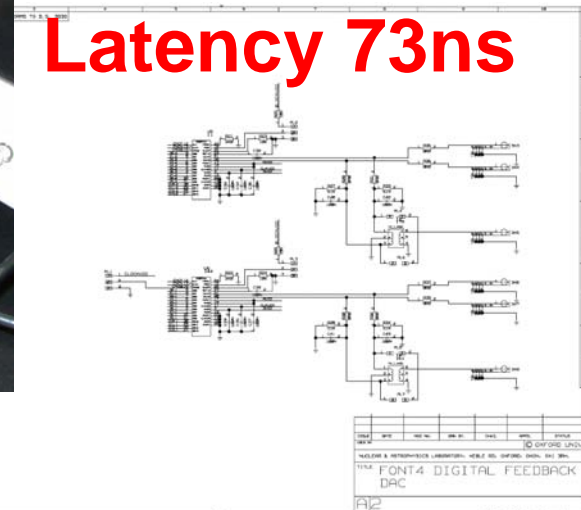


PCB loaded
April 4

Bench tests
April 5-14



Latency 73ns

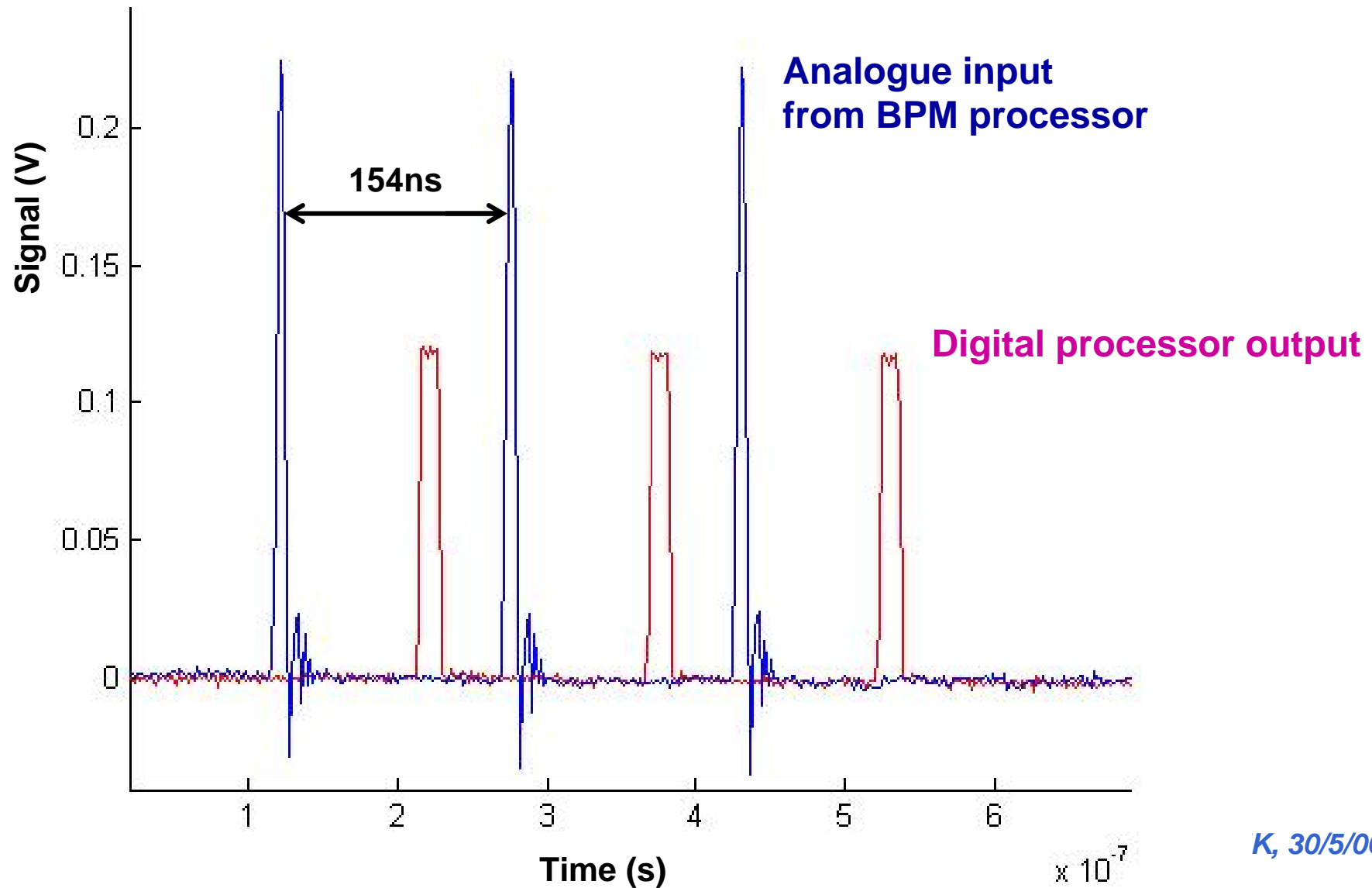


REV: 1
DATE: 2/6/2006
DESCRIPTION: FONT4 DIGITAL FEEDBACK ADC
DESIGNED BY: [Name]
CHECKED BY: [Name]
APPROVED BY: [Name]

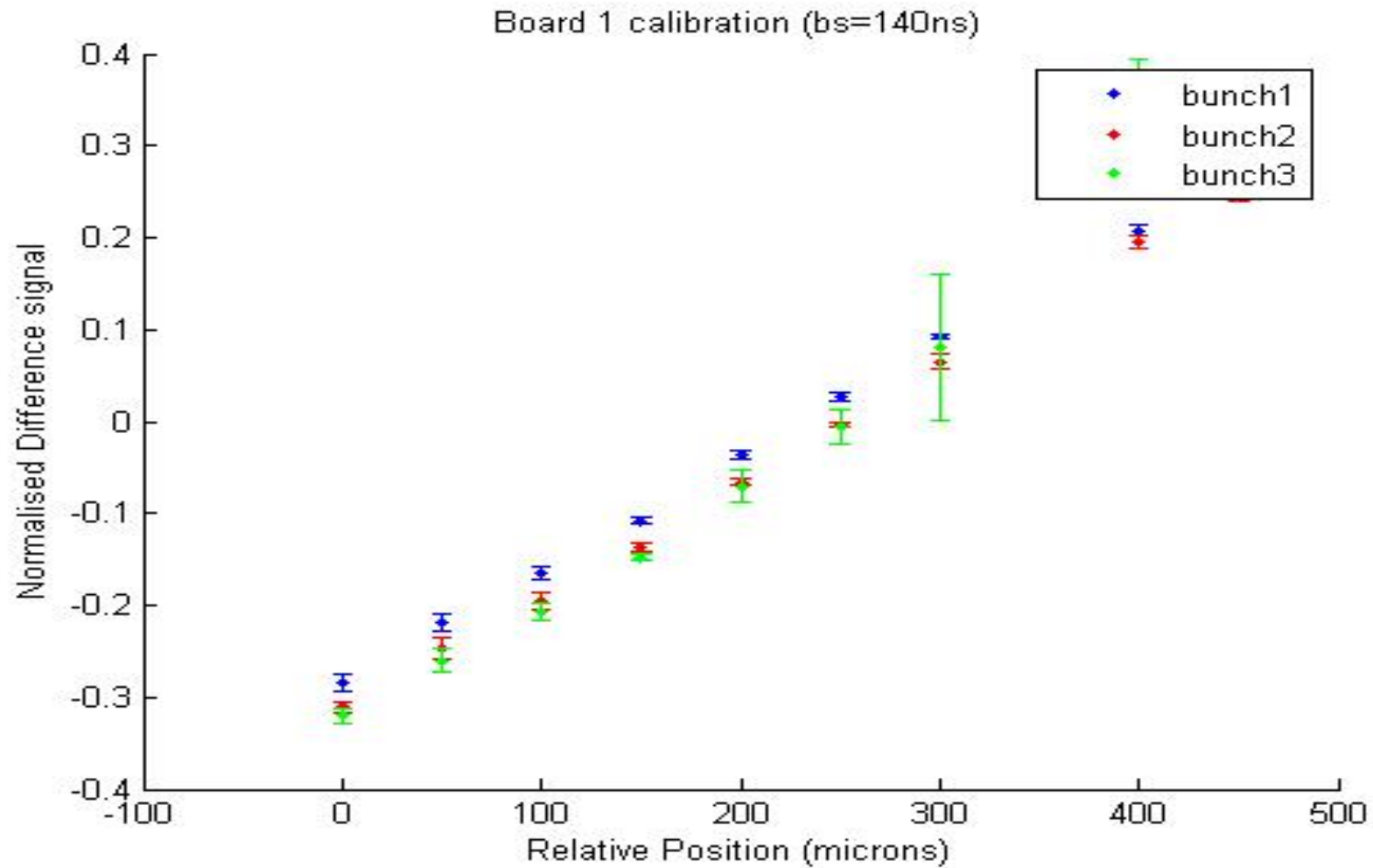
REV: 1
DATE: 2/6/2006
DESCRIPTION: FONT4 DIG BANK 0 FPGA
DESIGNED BY: [Name]
CHECKED BY: [Name]
APPROVED BY: [Name]

REV: 1
DATE: 2/6/2006
DESCRIPTION: FONT4 DIGITAL FEEDBACK DAC
DESIGNED BY: [Name]
CHECKED BY: [Name]
APPROVED BY: [Name]

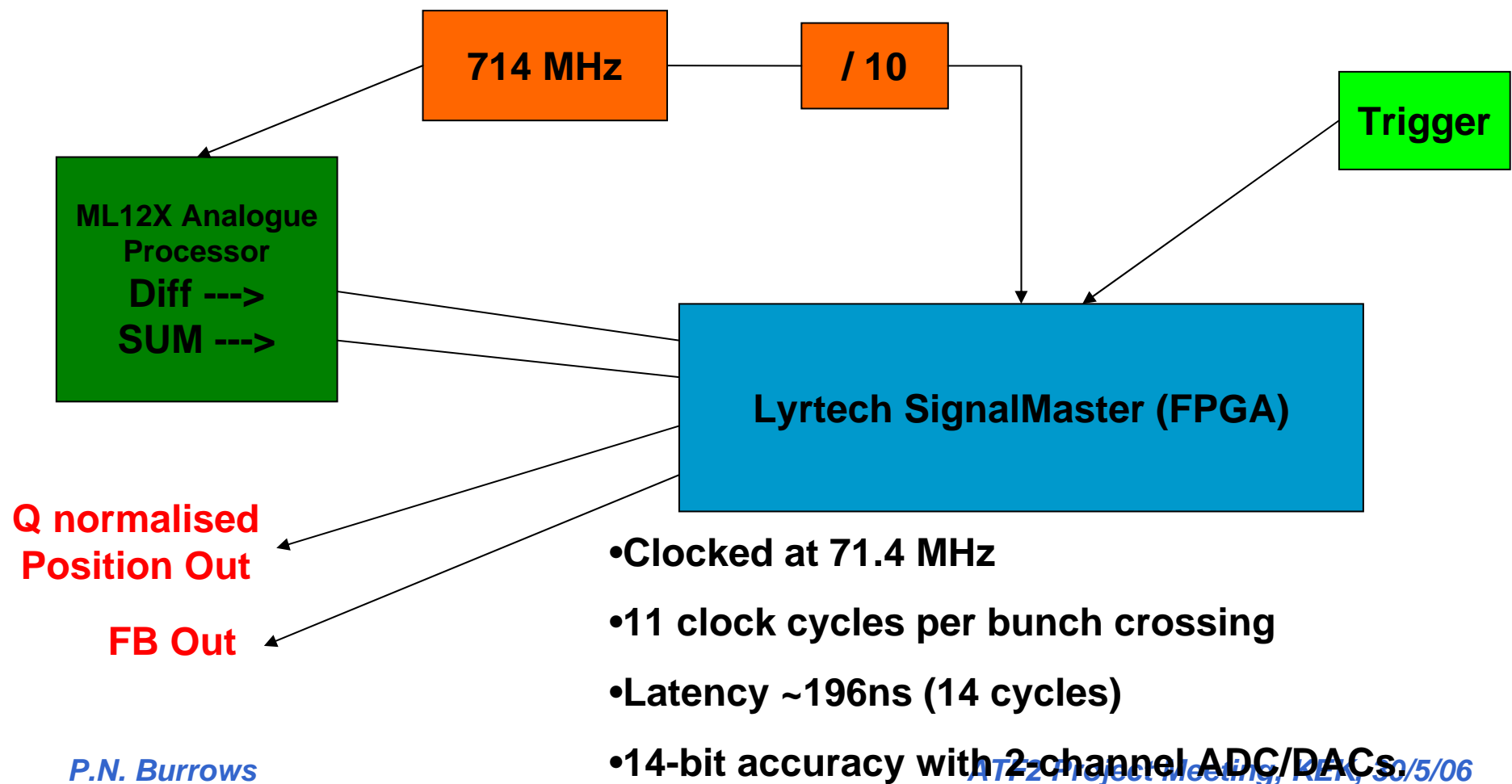
1st beam test results (20 April 2006)



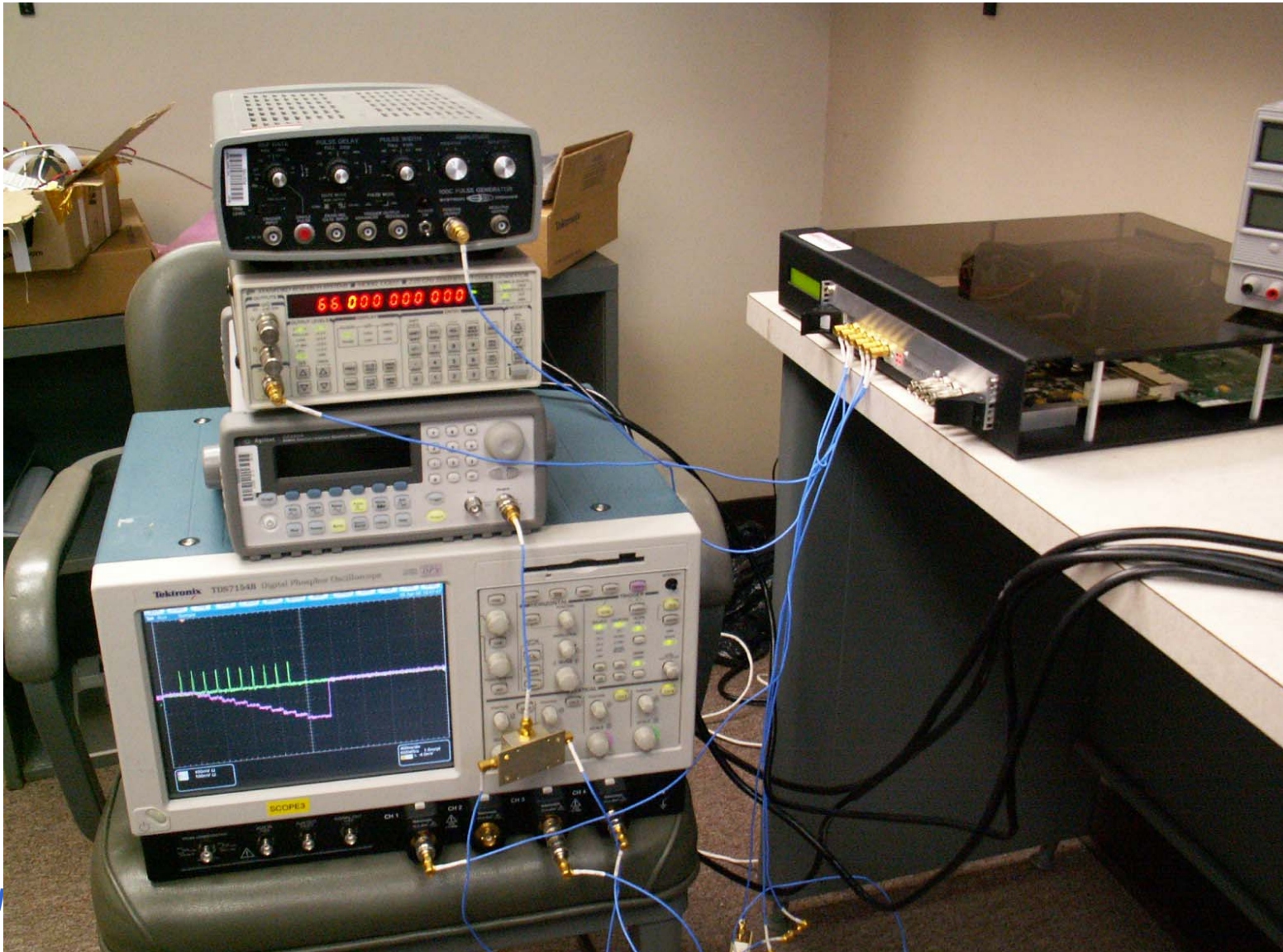
Position calibration



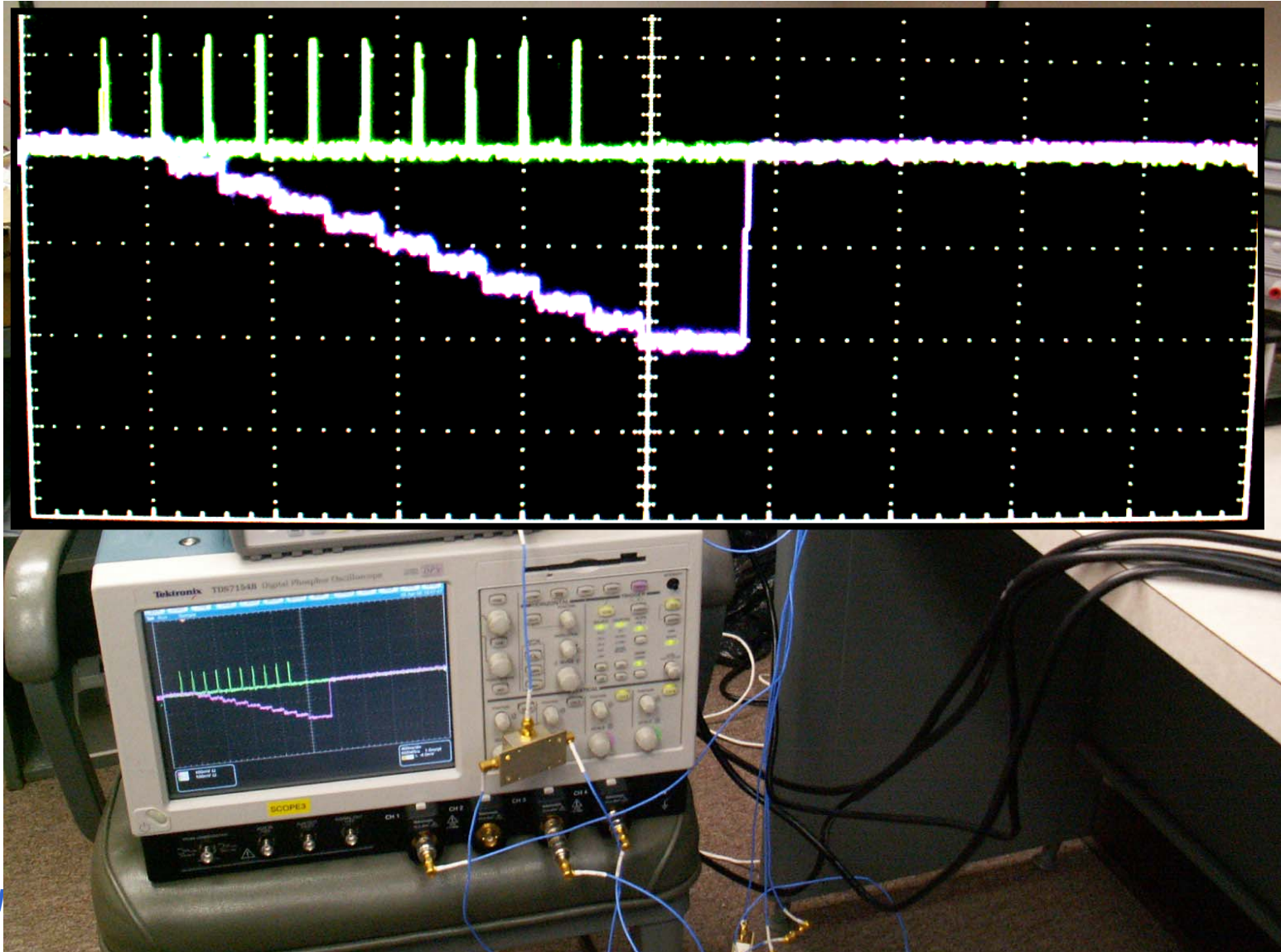
Lyrtech Signalmaster Board + Xilinx FPGA



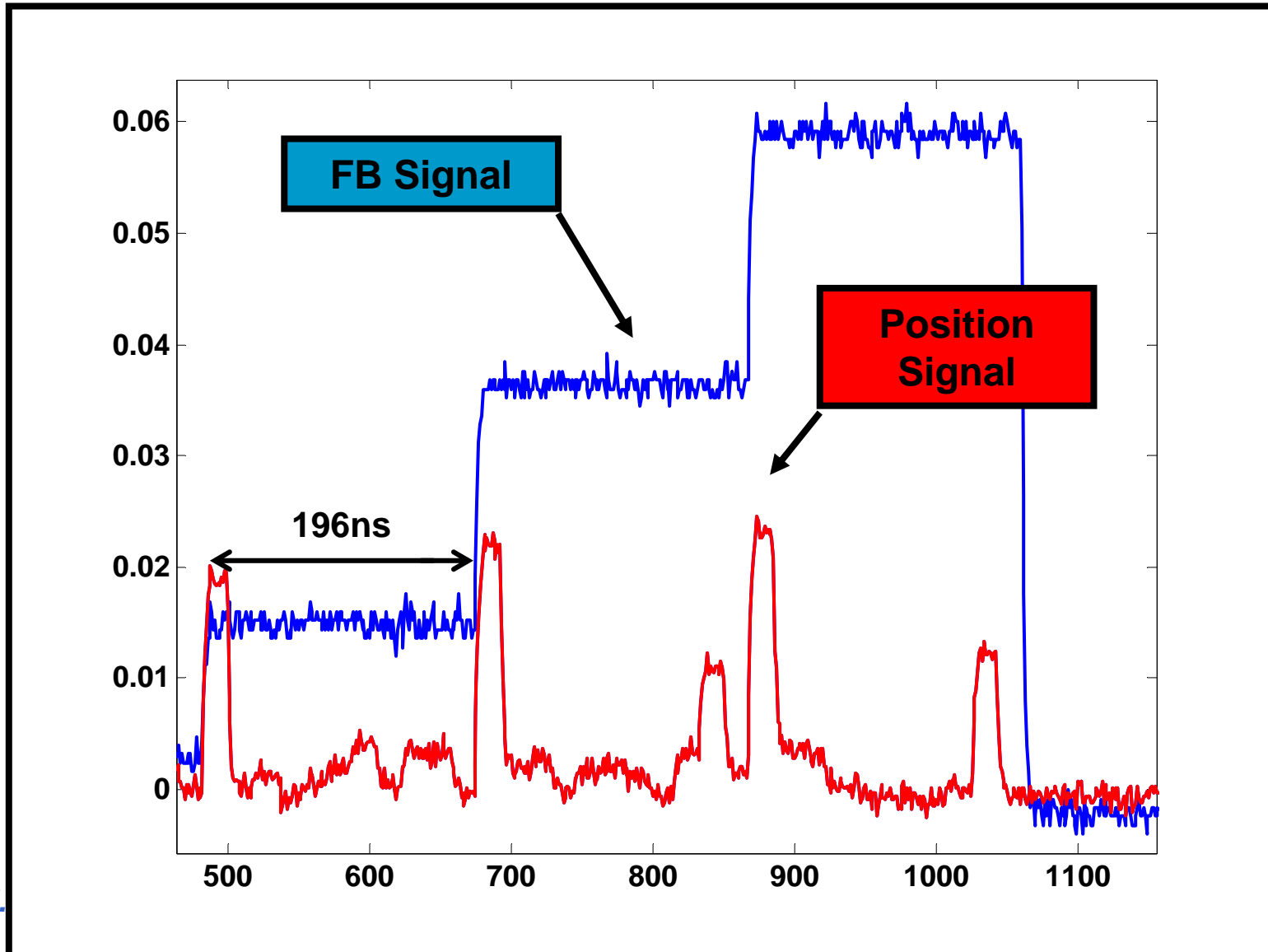
Lyrtech bench test



Lyrtech bench test results



Lyrtech beam test results (14/4/06)



FONT4 test plan

June 2006:

1st test of PCB version of analogue BPM processor

2nd tests of digital FB: timing, synchronisation, triggering,
gain adjustment in FPGA
(ADC clocking @ $714/10 = 71$ MHz)

December 2006:

1st test of FONT4 amplifier

3rd tests of digital FB: ADC clocking @ $357/4 = 90$ MHz

2nd tests of PCB BPM processor

Closed-loop FB

March/April 2007:

Closed-loop FB

FONT5 test plan

The next major development would be FB tests using a long ILC-like train of 20-60 bunches

Depends on success of fast-extraction kicker tests

2008/9?

I will discuss ATF2-specific needs in next talk ...

FONT bench test system

Dedicated bench test lab being set up in Oxford:

fast impulse generator for simulation of beam signals

signal generator for machine-phased clocks (714MHz)

analogue front-end + digital board

fast scope for DAQ

-> bench test complete FB system

Develop and test robust feedback algorithms:

include noise effects, long-range bunch correlations,

'adaptive' gain, feed-forward ...

Feed-forward system (1)

A feed-forward system has been discussed in vague terms for some time!

A ring -> extraction line system is conceivable based on FONT/FEATHER-type technology

In multi-bunch mode a feed-forward system JUST in extraction line is also conceivable (operationally like a feedback)

Is feed-forward necessary?

1) ATF / ATF2 operations?

2) ILC prototype (eg. RTML system)?

Feed-forward system (2)

- **What do we want to stabilise?**

Energy? (Kalinin idea)

Vertical position/angle?

Horizontal position/angle?

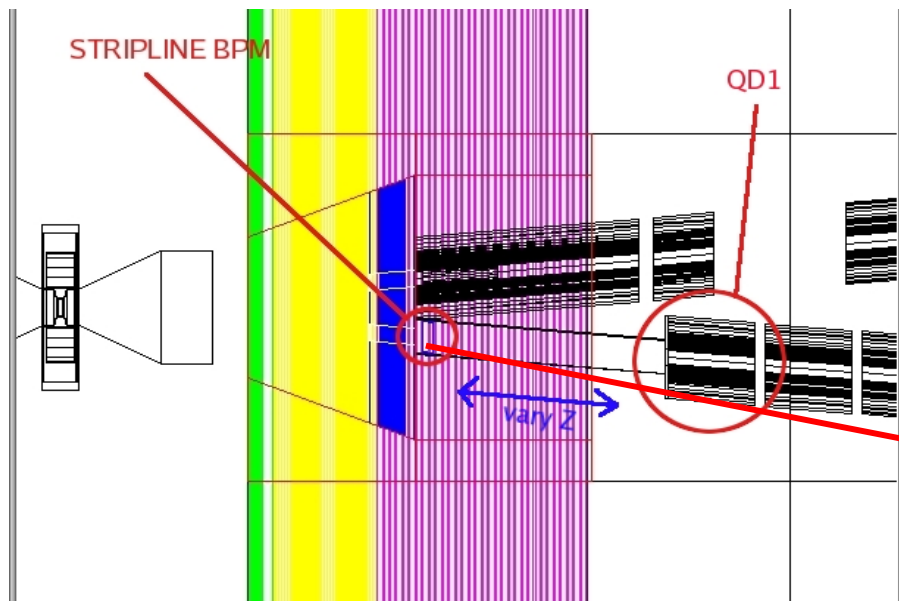
- **Need to know dominant jitter source(s):**

Eg. if extraction kicker,

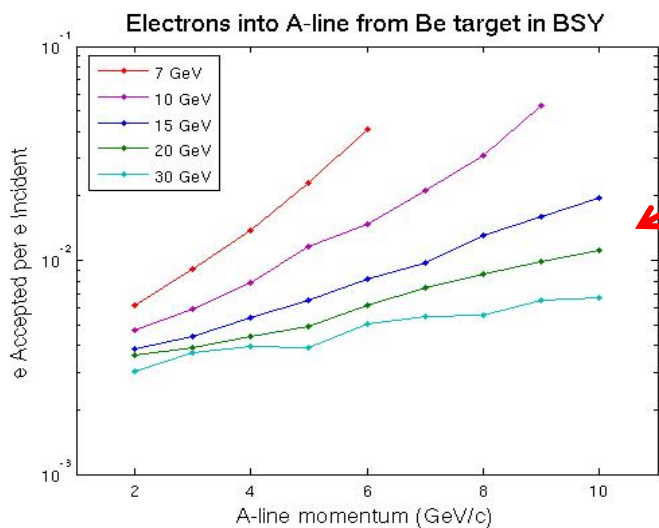
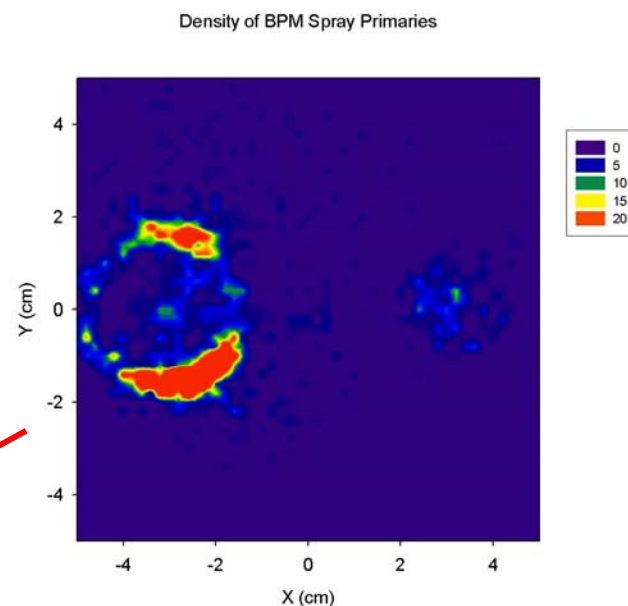
ring -> extraction line no use!

upstream -> downstream in extr. line (multi-bunch mode) OK

EM Background Environment for FB BPM

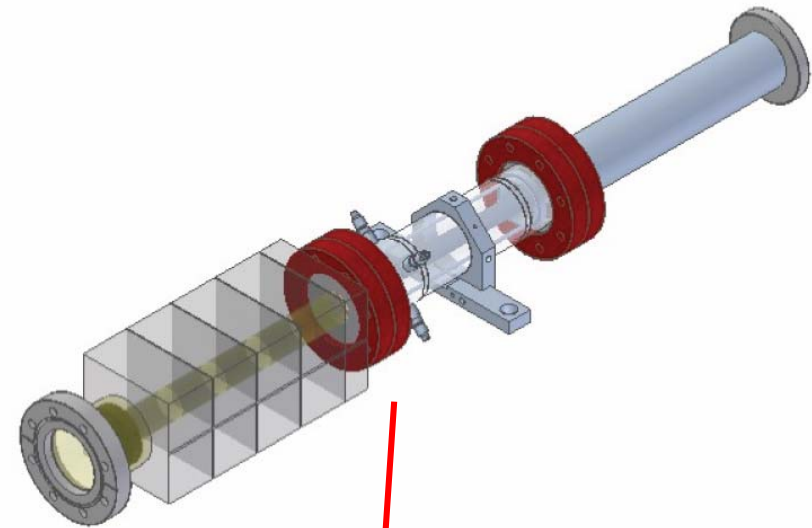
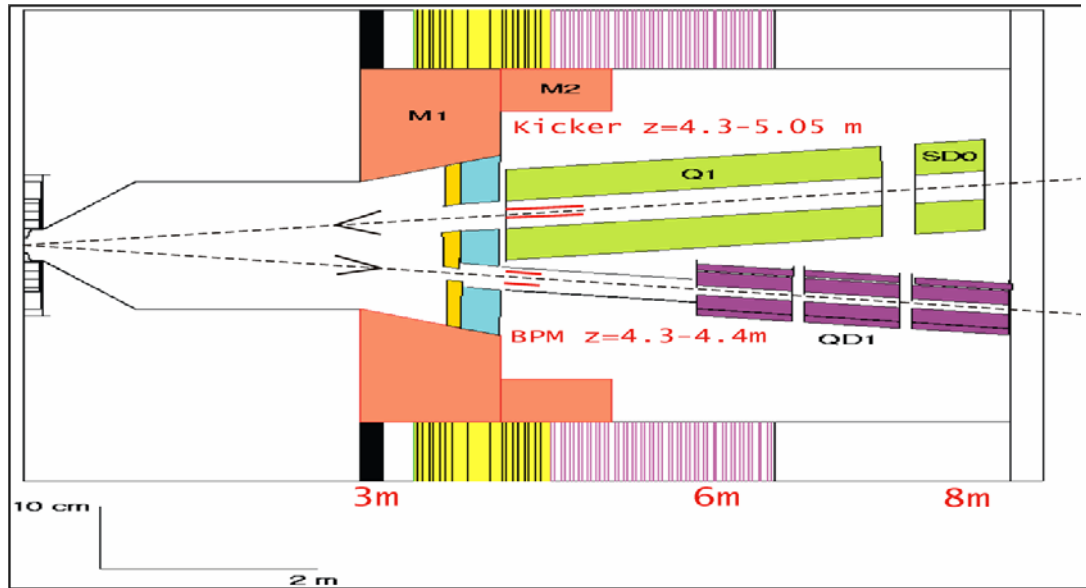


Energy deposition on mask:



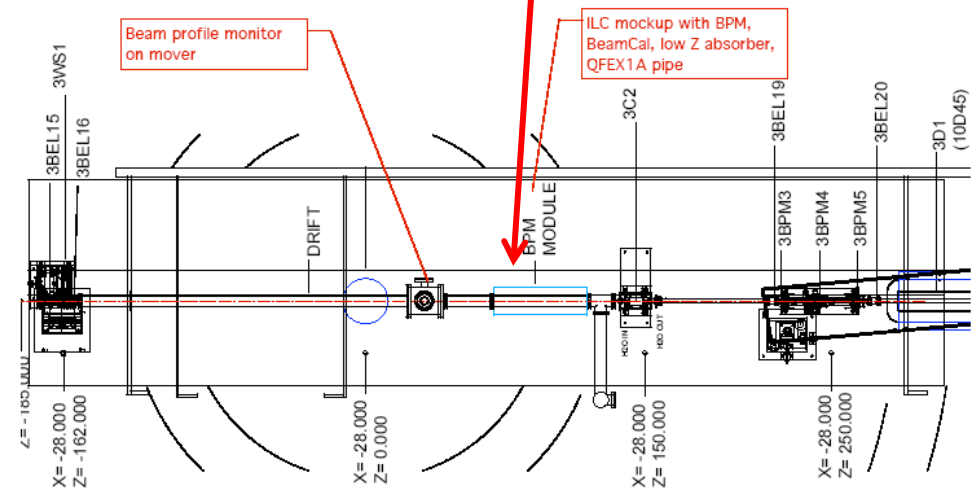
Create using ESA 'spray beam' for experimental test

FONT Test Module for ESA



FONT Spray Beam Test Layout in SLAC ESA

First beam tests
July 7 – 21 2006

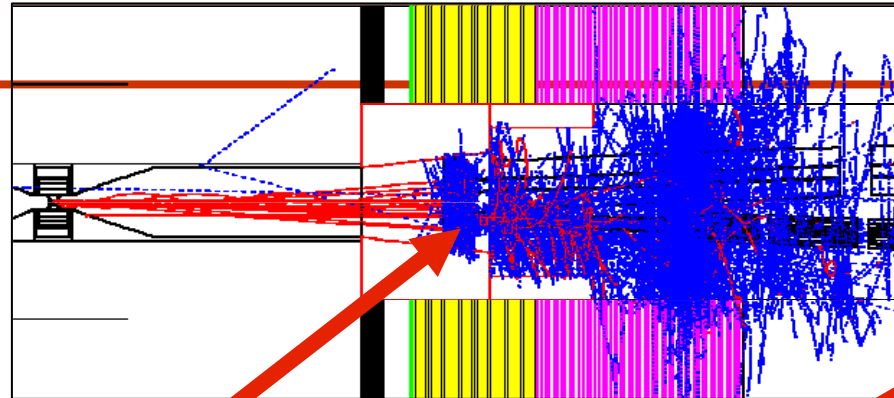


Strategic ILC FB outlook

- Continuing intra-train IP FB hardware prototyping deemed 'critical' in BCD – **FONT programme ongoing at ATF, ESA, ATF2**
- **Optimisation of BPM design(s) for feedback/feed-forward systems**
- **Need to design bunch-by-bunch luminosity signal into IP FB**
- **Intra-train FB technology required for BDS, linac, RTML FF ...**
- **Hardware directly applicable to 5Hz feedbacks throughout machine**
- **Development of robust algorithms critical – test setup in Oxford**
- **Integrated design of whole alignment + feedback strategy critical**

BeamStrahlung (White)

ILC IR



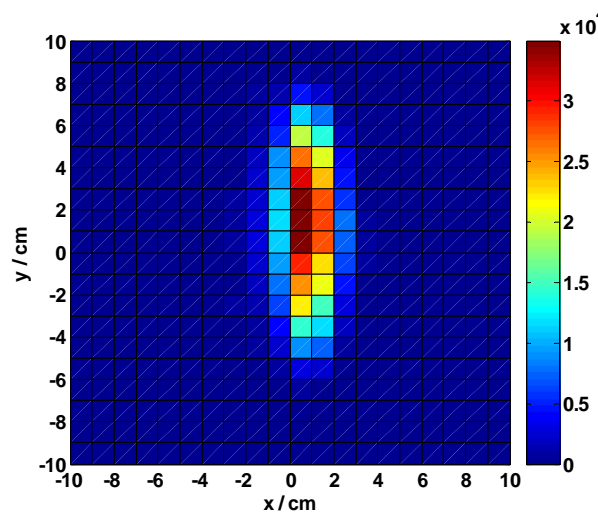
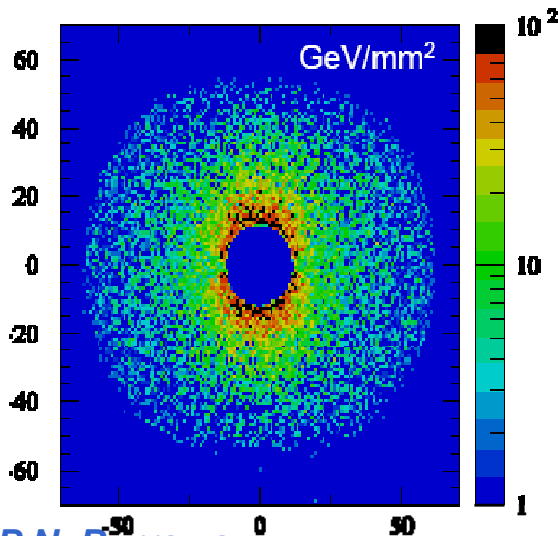
200m

Diagnostics of bunches at IP.

BeamCal

Photon Detector

3 potential sources of information:



1. Energy-distribution of Pairs.
2. Number-distribution of Pairs.
3. Energy-distribution of Photons.

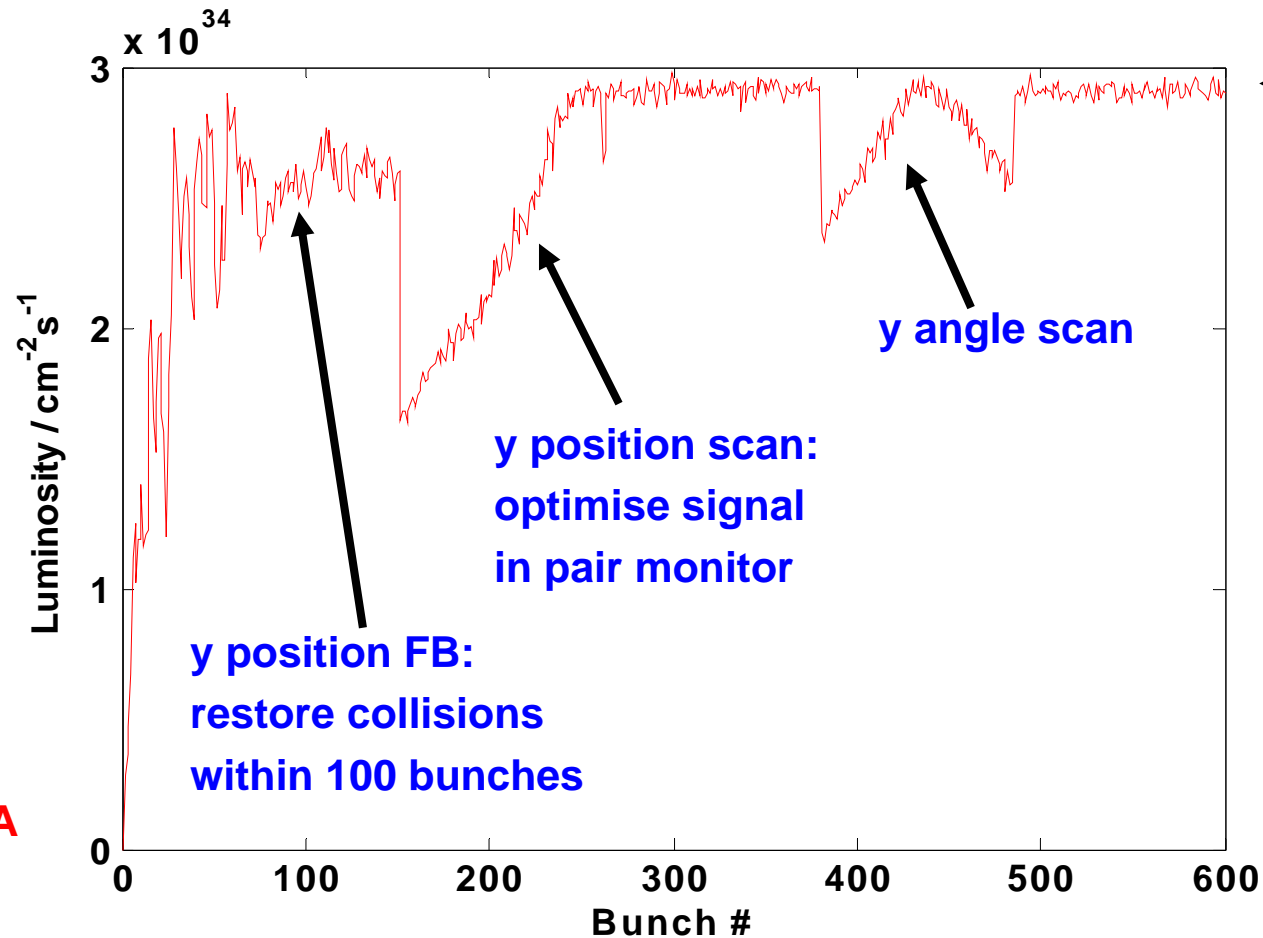
Possible additional developments

Add (beam related?) 'luminosity' signal input to FB system at ATF(2)

Add angle FB

Extra material

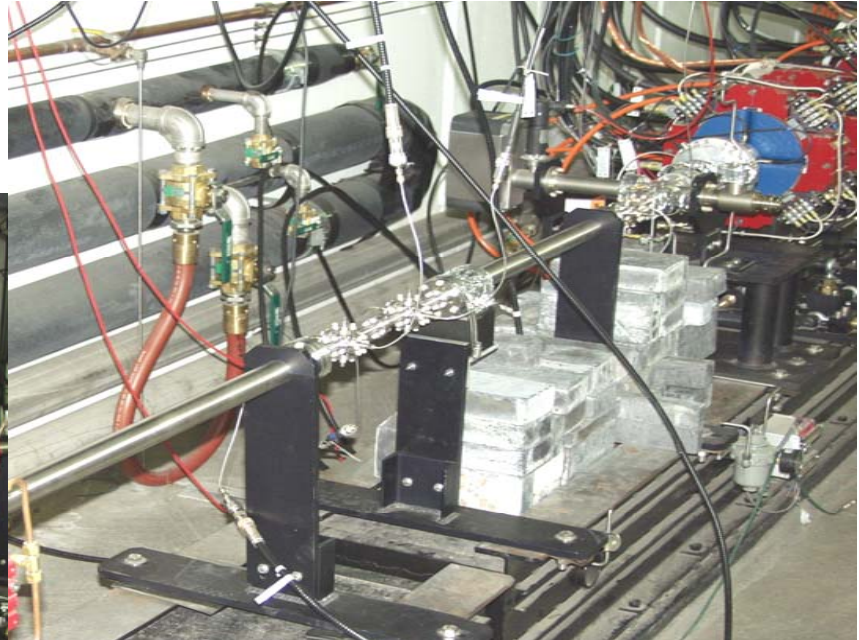
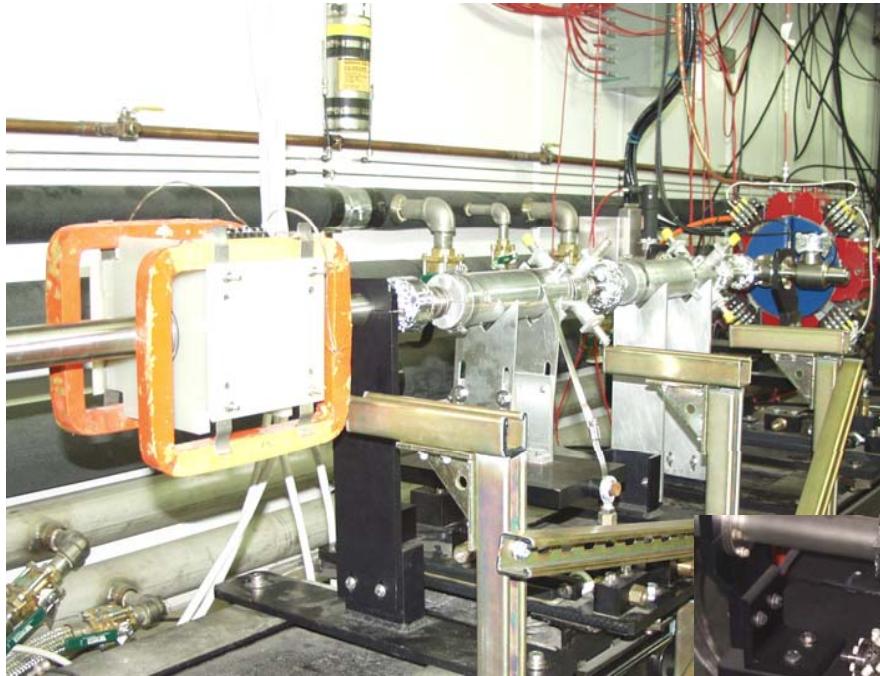
Intra-train feedback simulations



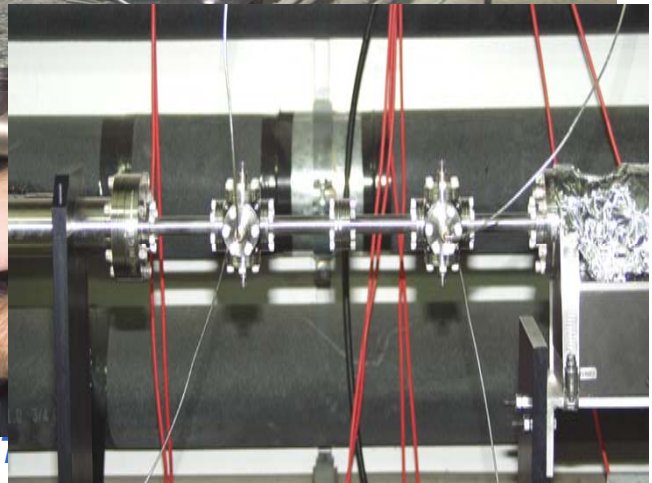
1 seed:
post-BBA
+ GM
+ wakes

FONT2 beamline at SLAC NLCTA

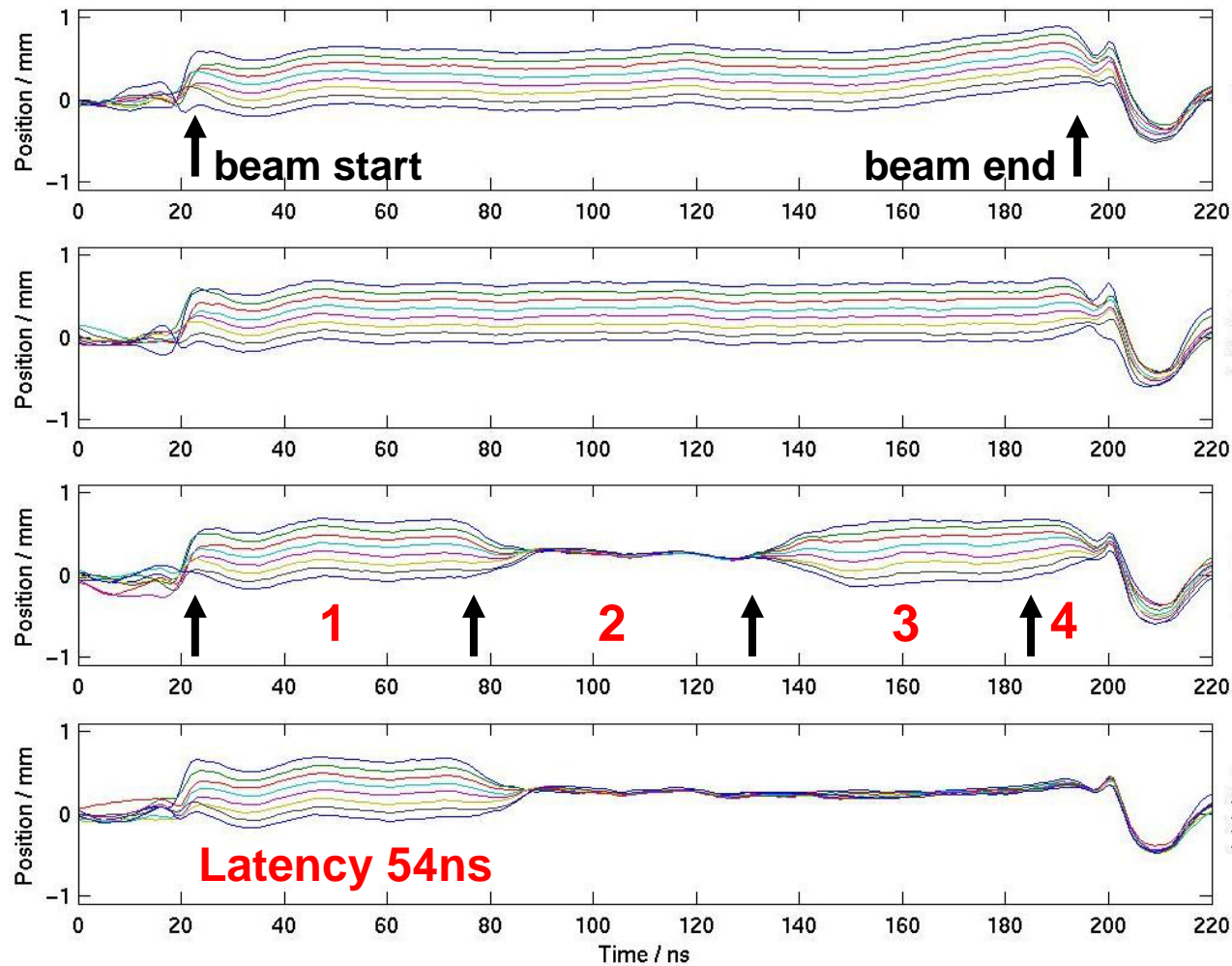
Dipole and kickers



BPMs



FONT2 position correction performance



Beam starting positions

Beam flattener on

Feedback on

Delay loop on