

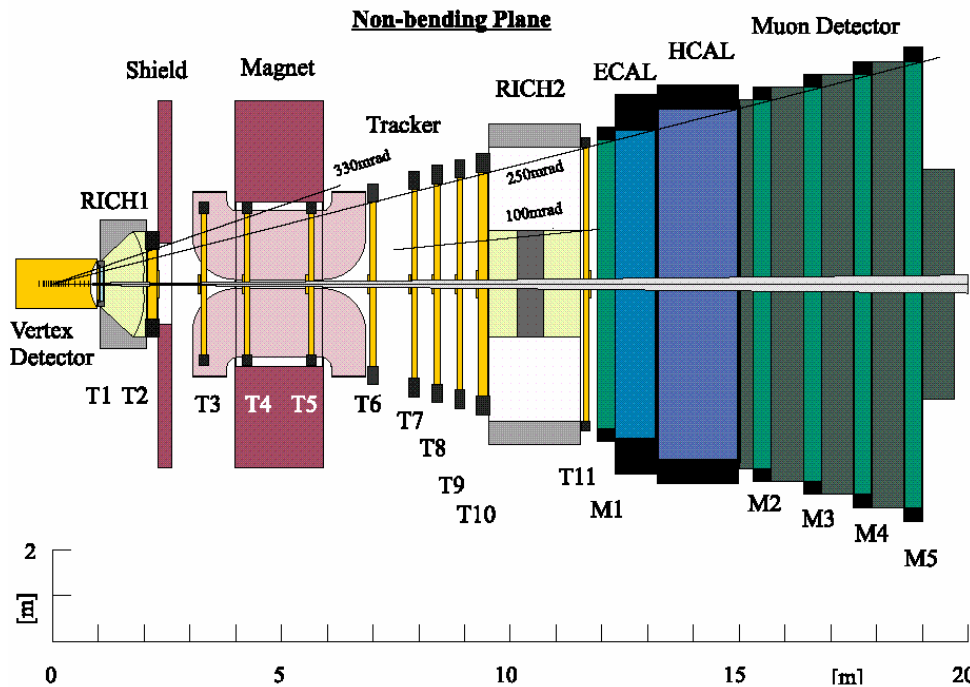
# *SPD Very Front End Electronics*

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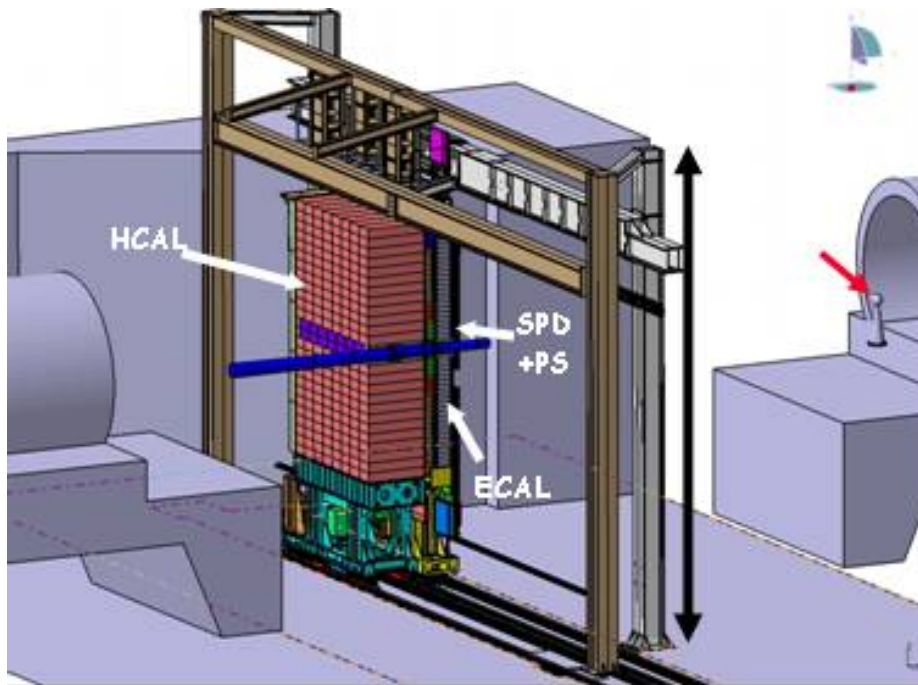
- LHCb Detector
- Calorimeter system
- Scintillator Pad Detector (SPD)
- Pulshape Characteristics
- Situation
- Readout Electronics
- VFE Design Solution
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The LHCb spectrometer comprises:

- **Vertex detector:** provides information on the production and decay vertices of b-hadrons and the trajectories of the particles close to the interaction point.
- **Tracking system:** provides reconstruction and precise momentum measurement of charged tracks and information for the triggers.
- **Rich detectors:** identify charged particles with a momentum over a threshold.
- **Calorimeter system:** provides identification of electrons and hadrons for trigger analysis with measurements of position and energy.
- **Muon detector:** identifies muons or the trigger information.

# Calorimeter System



The LHCb calorimeter has four elements:

- ***Hadronic calorimeter*** (HCAL)
- ***Electromagnetic calorimeter*** (ECAL)
- ***Preshower detector*** (PS)
- ***Scintillator Pad Detector*** (SPD).

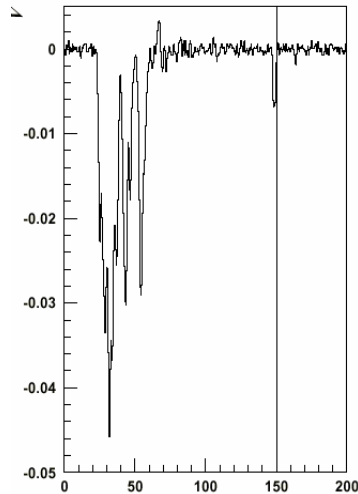
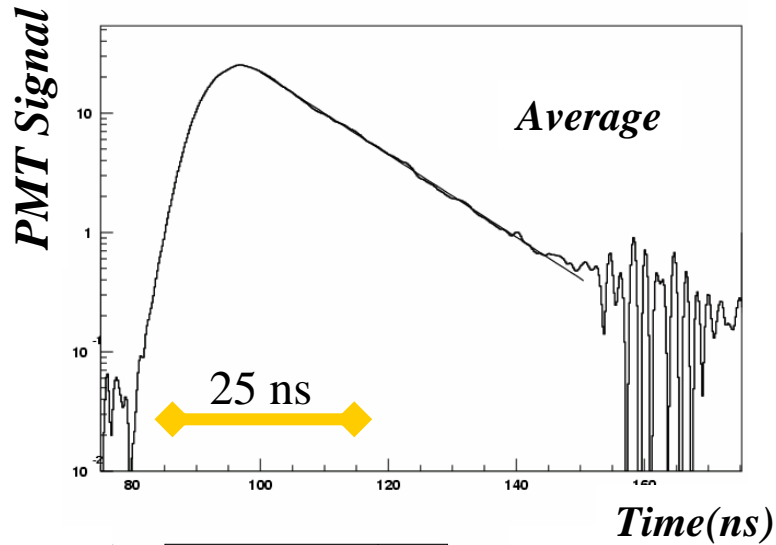
The system provides high energy hadrons, electron and photons candidates for the first level trigger.

Scintillator Pad Detector (SPD) performs the  $e^-/\gamma$  separation at the Level 0 trigger.

Characteristics:

- It is a plastic scintillator layer, divided in about 6000 cells of different size in order to obtain better granularity near the beam.
- Charged particles will produce, and photons will not, ionization on the scintillator.
- This ionization generates a light pulse that is collected by a WaveLength Shifting (WLS) fiber that is twisted inside the scintillator cell.
- The light is transmitted through a clear fiber to the readout system.
- In order to have low costs, these 6000 cells are divided in groups using a MAPMT of 64 channels for receiving information in the readout system

Cosmic rays 12x12 Pad Test



## Signal Characteristics outing the MAPMT:

- Low photo-statistics: 20-30 phe.
- Only ~80 % of signal in 25 ns -> Pile Up Correction is needed
- No dead time on integration

Readout system is divided into three different blocks:

**Front-end Racks:** L0 Front-End Cards, Power Supplies (HV and LV) and SPD control cards

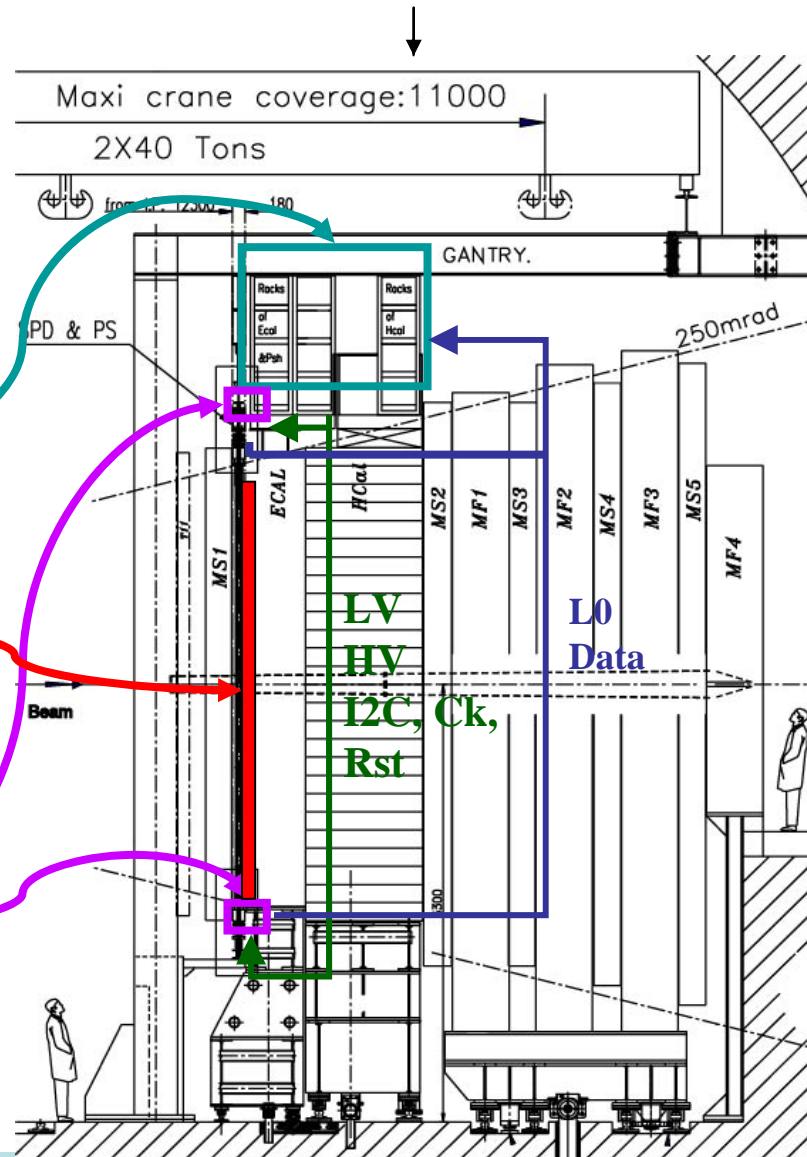
**Scintillating Pad Det (SPD)**

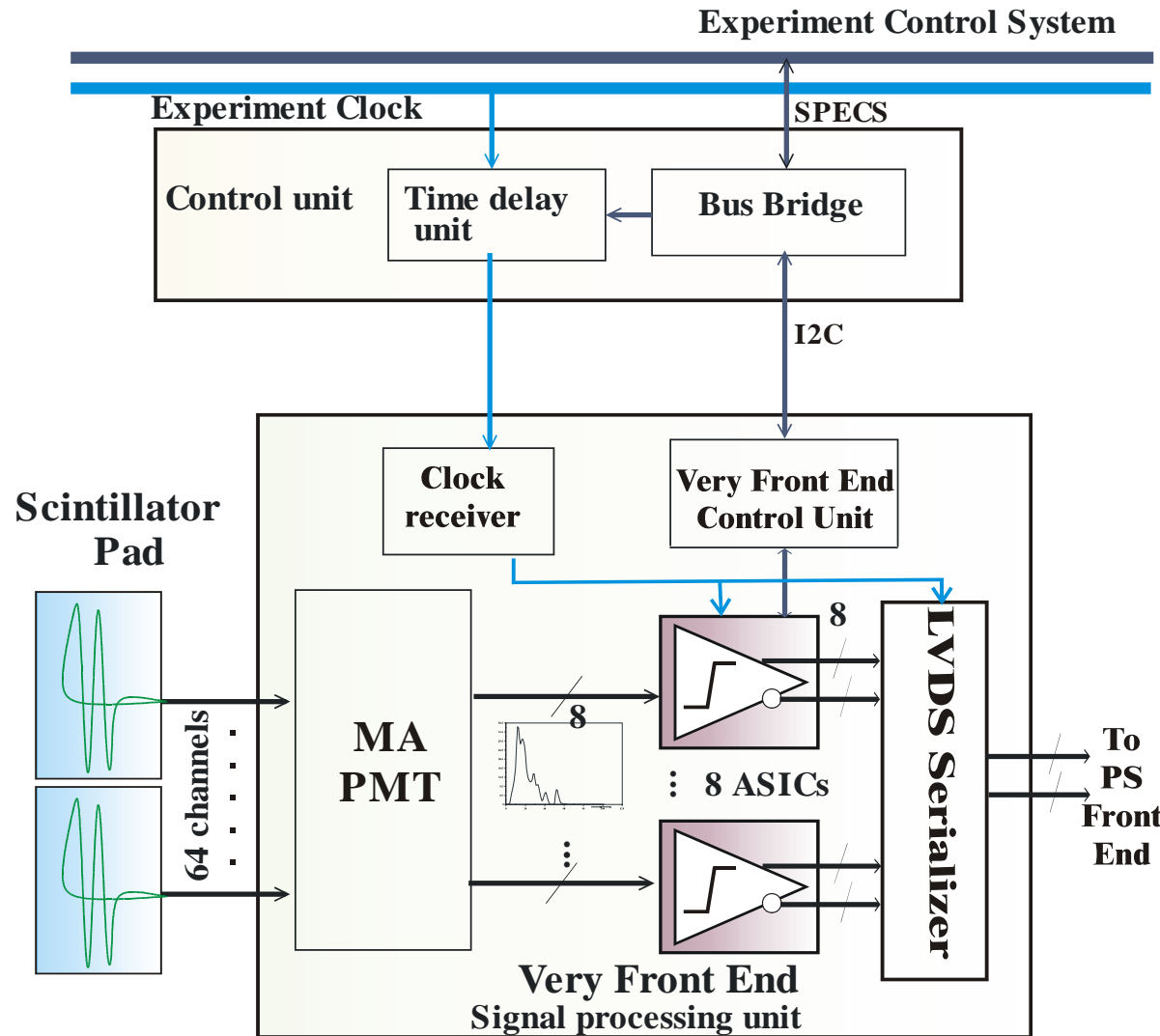
Scint. Pad + Fibres+ MaPMT  
**5953 cells**

**VFE SPD**

Metallic boxes: top and bottom ends of the detector

- VFE units
- Regulation cards





Functional design for the SPD readout is split into :

- *Very Front End board* hosting a PMT with its corresponding 8 ASICs

- *Control board* sitting at the calorimeter front end crates and interfacing the experiment control system and the VFE cards

- *LV Regulator Board* that feeds the VFE Card

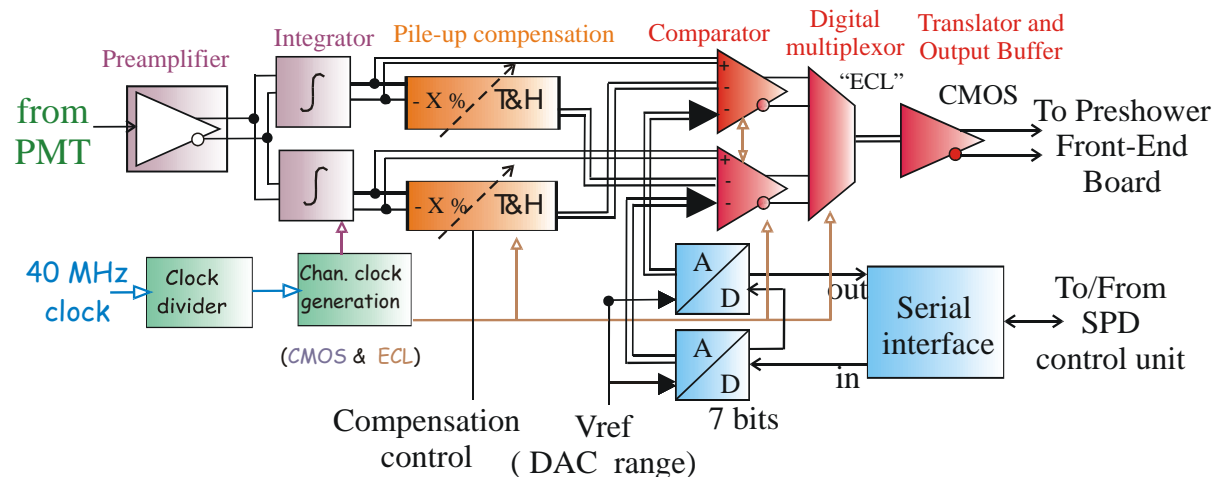




The analogue processing is made by an ASIC, which has a working frequency of 40MHz divided in two subchannels that work at 20MHz.

The processing involves:

- integrating each signal,
- Subtracting and adjustable fraction of the charged integrated in the previous 25ns period (in order to correct pile-ups due to the tail of the expected signal is longer than 25ns),
- comparing the result to programmable thresholds for each subchannel a digital output is obtained: '1' if above the threshold, '0' otherwise.



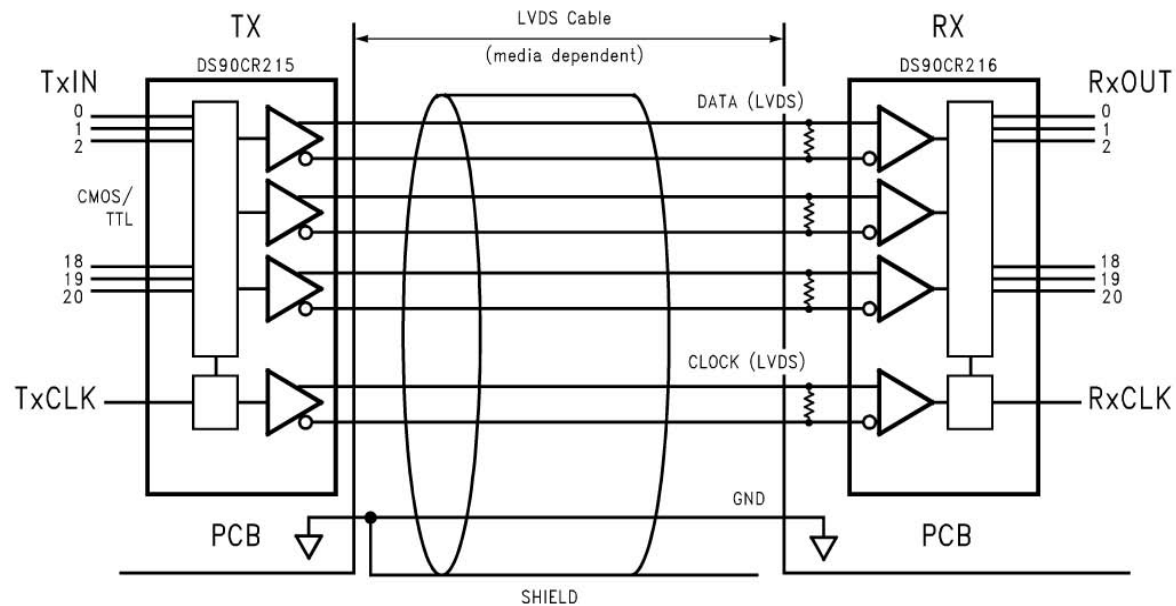
Communication with the Control Card (in the racks) is made with an **FPGA**, an APA300 (Actel FPGA, **flash based** not antifuse based)

Some functionalities:

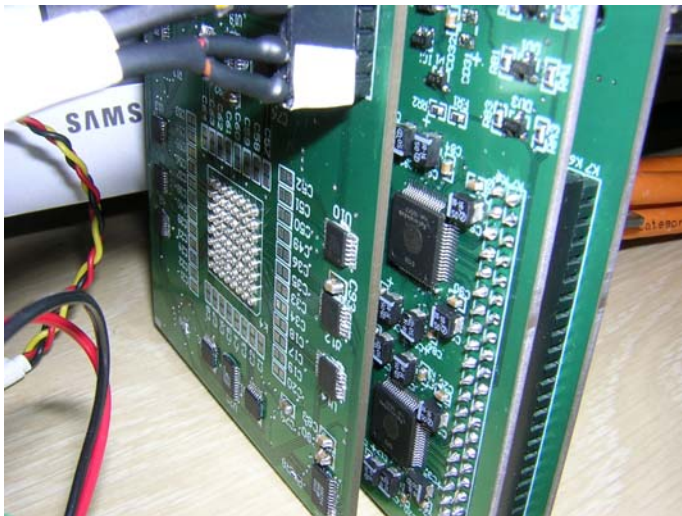
- I2C bidirectional communication with the control board.
- Write and read ASIC registers.
- Write and read DACs (Vref i Vbias) via a local I2C bus.
- ASIC SEUs: Checking, correction and signalling.
- DAC SEUs: Checking, correction and signalling.
- DAC no longer responding: checking, reset and signalling.

The output of the SPD goes to the FE Card of the PreShower detector that is hosted in the racks, 20-25 meters far away: a critical link is needed.

This link is made by LVDS Serializers that prepared the ASICs digital outputs to be transmitted to the high speed LVDS(280Mbit/s) link: A special cable has to be made for accomplishing the skew requirements

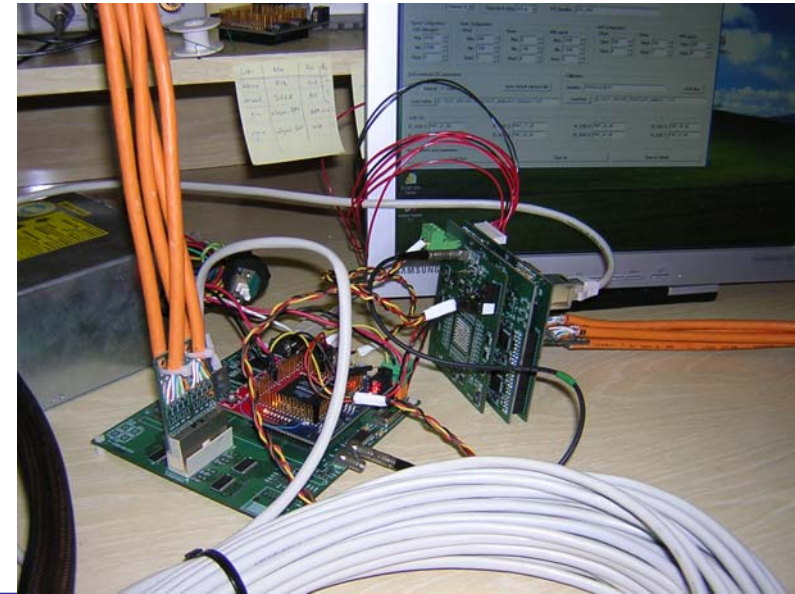
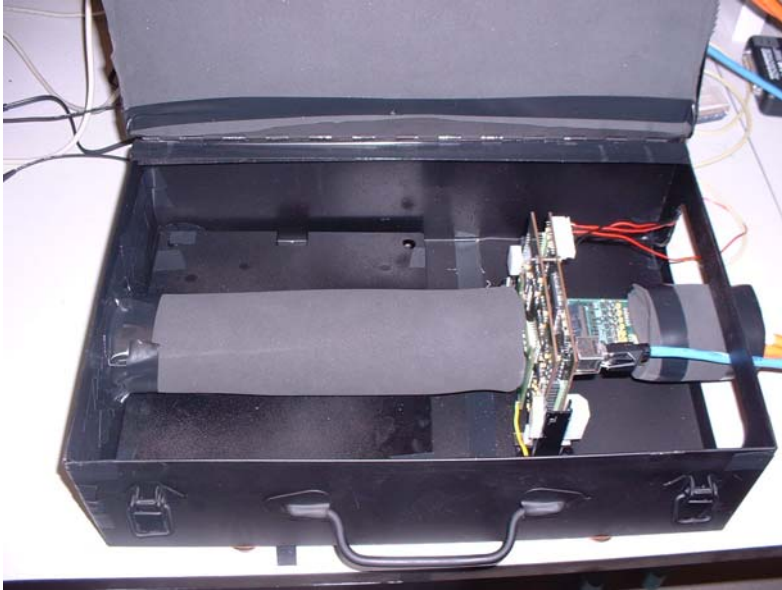


# SPD VFE Final Prototype



As a first attempt, the original design was only one 15cmx15cm size. As a result of the mechanical problem( MAXIMUM SIZE 12x9cm) and the functionalities added, the design has been split to three different cards:

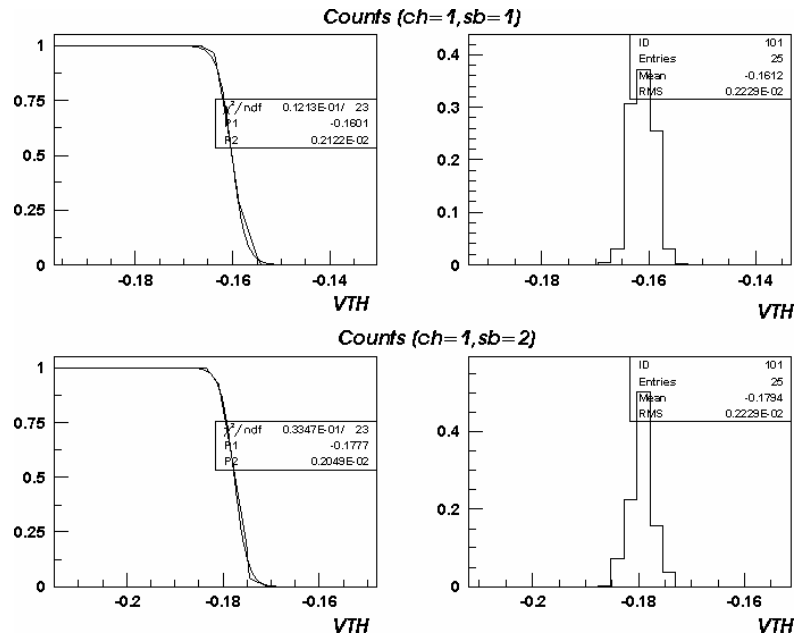
- *Base card* which contains MAPMT[8], and the active base of the MAPMT.
- *ASICs card* which involves the 8 ASICs (discriminator in the figure) and all the analogue part (subtractor reference for compensating the pile up, threshold reference for the whole card).
- *Serializers card* which contains the LVDS serializers, for the multiplexed LVDS link mentioned before, the FPGA as a control unit, LVDS transceivers.



Laboratory Set Up

*Functionality tests* show the good performance of the card. The items tested:

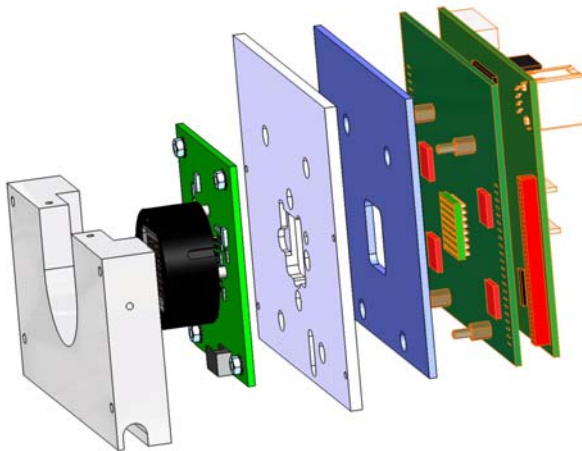
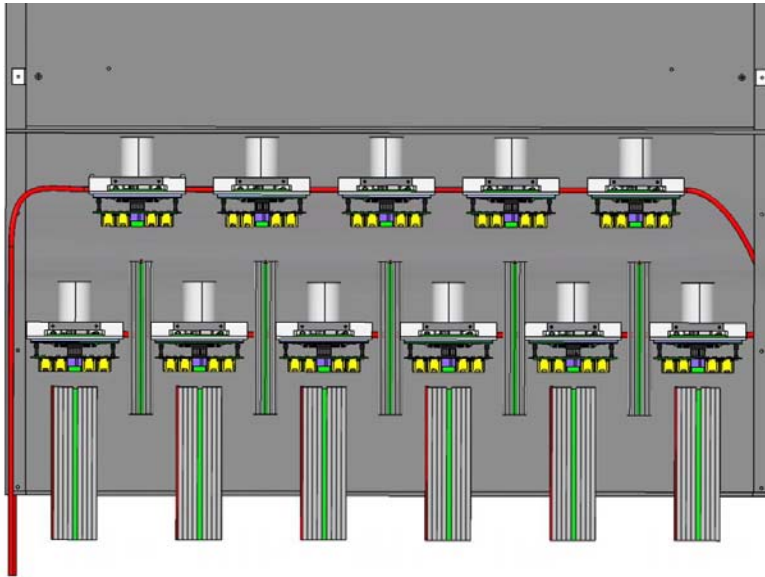
- Programming internal threshold references for each subchannel in ASICs
- Programming DACs for external threshold reference and subtractor reference (pile up compensation)
- Power consumption. It is important to notice that the consumption of the card is an important point for the design of the whole system : a regulator card is needed to feed each VFE.



## Results

- Mapping. The SPD is not a subdetector alone, it belongs to the LHCb Calorimeter, and map each PMT channel from the Photomultiplier to the other detector has become a tedious task, as a result of the asymmetry of the detector itself.
  - Noise. Its value is around 2mV and it is acceptable.
  - Clocks. The shape of the signal has been checked in order to control de jitter.

# SPD VFE Cooling Tests (I)



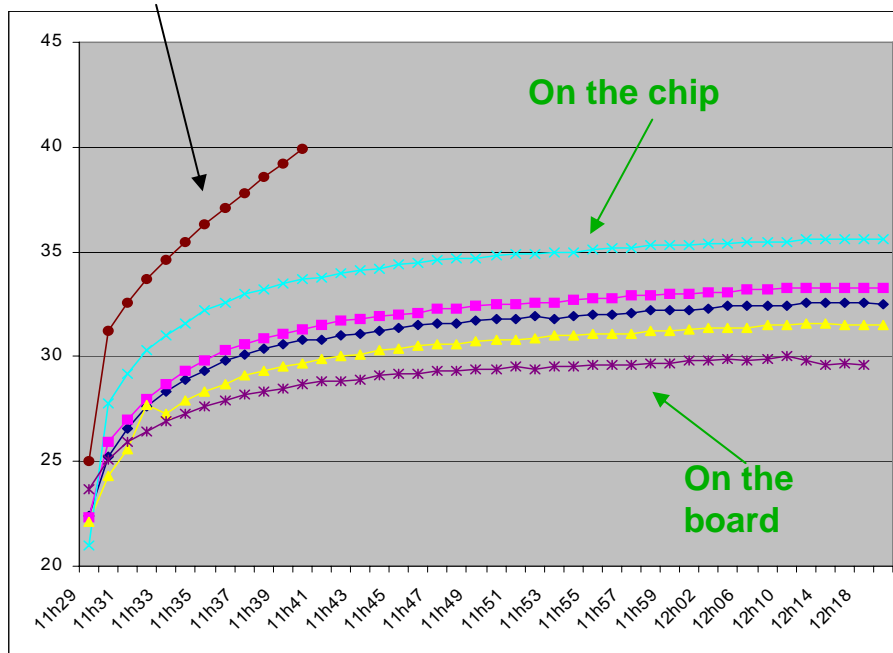
Cooling is made by a cool water circuit around boards. A conductive material of heating is put on the cards and it is in contact with an aluminum platform that contains the water circulating on.

Cooling tests, has been done in Clermont-Ferrand at LPC (Laboratoire Physique Crepusculaire ) between July and September 2005

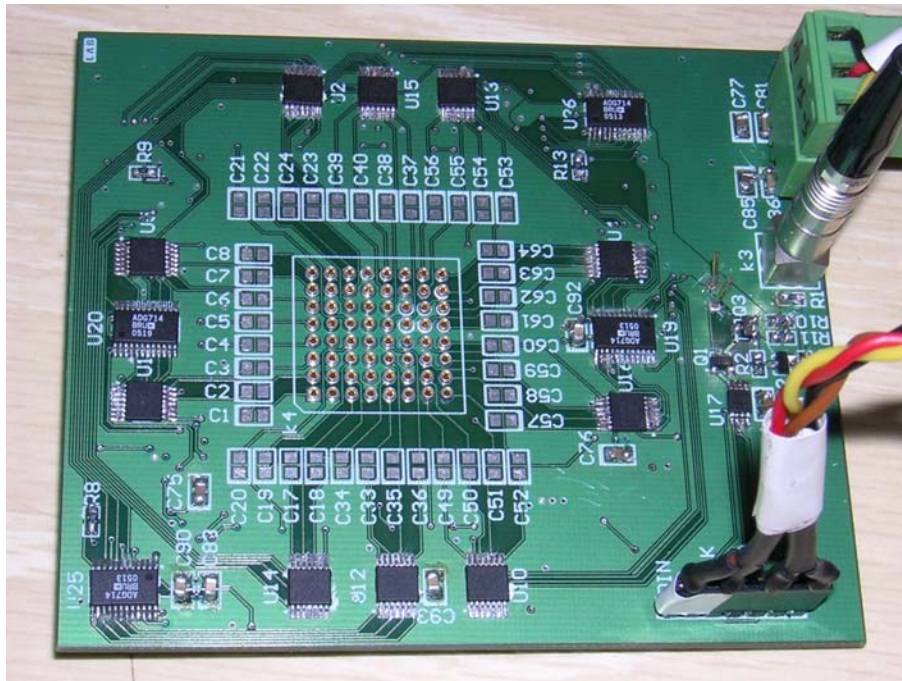


**Without cooling**

**With cooling**



The results showed that the maximum temperature achieved is near the limit of the maximum value of temperature of the FPGA.



## **Pre-Series Tests**

- A pre-series is being done at this moment.
- The results of this pre-series will show the good performance of the card, and it will be used to test all the automatic set-up prepared for the series test.
- An special card for injecting signal has been designed.

## ***EMI and Radiation Tests***

These tests are planned to be done during June-July 2006.

## ***Burn-in Tests***

These tests are done by Applus+, a Certification Technological Center.

The temperature range and time cycles are:

8 cycles of 9h20 between 0 and 70 Celsius degrees with a 2h20 stop at 0 degrees, 40 degrees, and 70 degrees, with slopes of 2 degrees per minute in 'montée' and 1 degree per minute in 'descent'.

## ***Automatic Series Test***

It is planned to be made between September-November

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