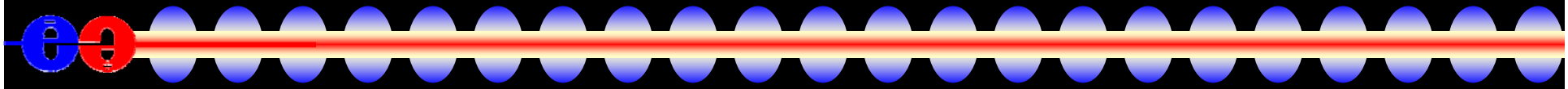


A Silicon-Tungsten EMCAL with Integrated Electronics for the ILC

S. Adloff, F. Cadoux, J. Jacquemier, Y. Karyotakis

LAPP, Annecy

Mechanical Design

V. Radeka

BNL

Electronics

B. Holbrook, R. Lander M. Tripathi

UC Davis

Bump Bonding Mechanical Design Cabling

M. Breidenbach, D. Freytag, N. Graf, G. Haller, R. Herbst

SLAC

Electronics Mechanical Design Simulation

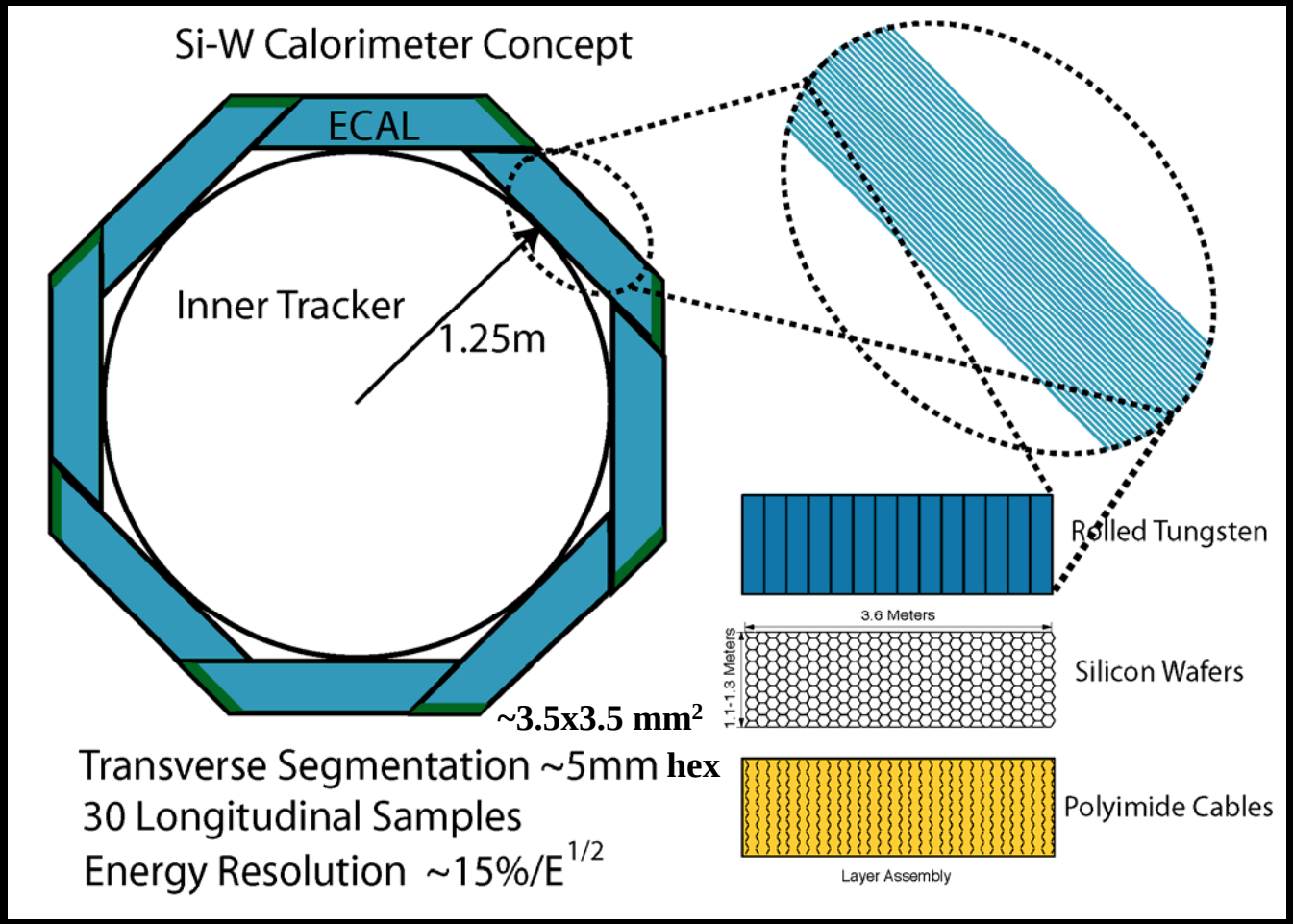
J. Brau R. Frey, M. Robinson D. Strom

U. Oregon

Si Detectors Mechanical Design Simulation

CALOR '06
June 9, 2006

Overview



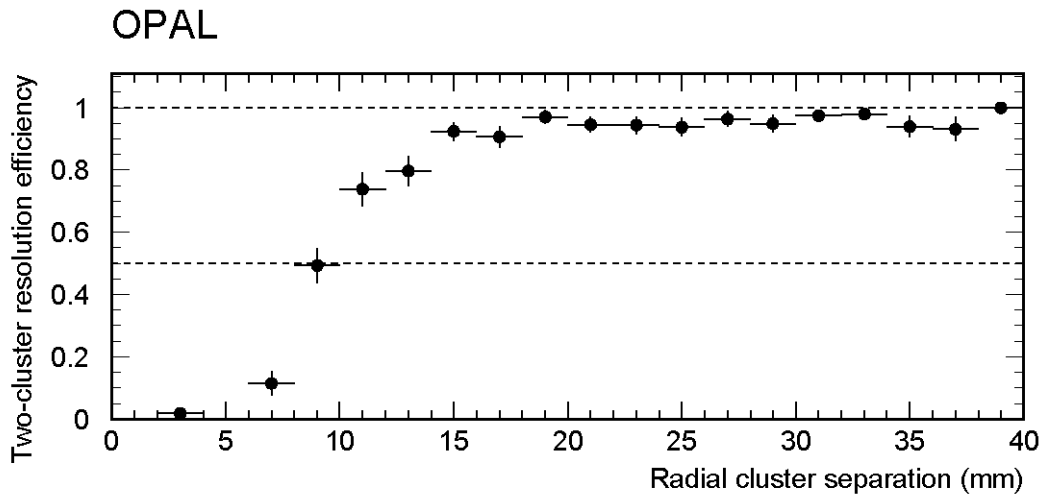
Baseline configuration:

- transverse seg.: 12 mm² pixels
- longitudinal: (20 x 5/7 X_0) + (10 x 10/7 X_0)
- ≈ 1 mm readout gaps

Optimized for the SiD concept

Segmentation requirement

- We wish to resolve individual photons from jets, tau decays, etc.
- The resolving power depends on Moliere radius and segmentation.
- Want segmentation significantly smaller than R_m = ~10 mm

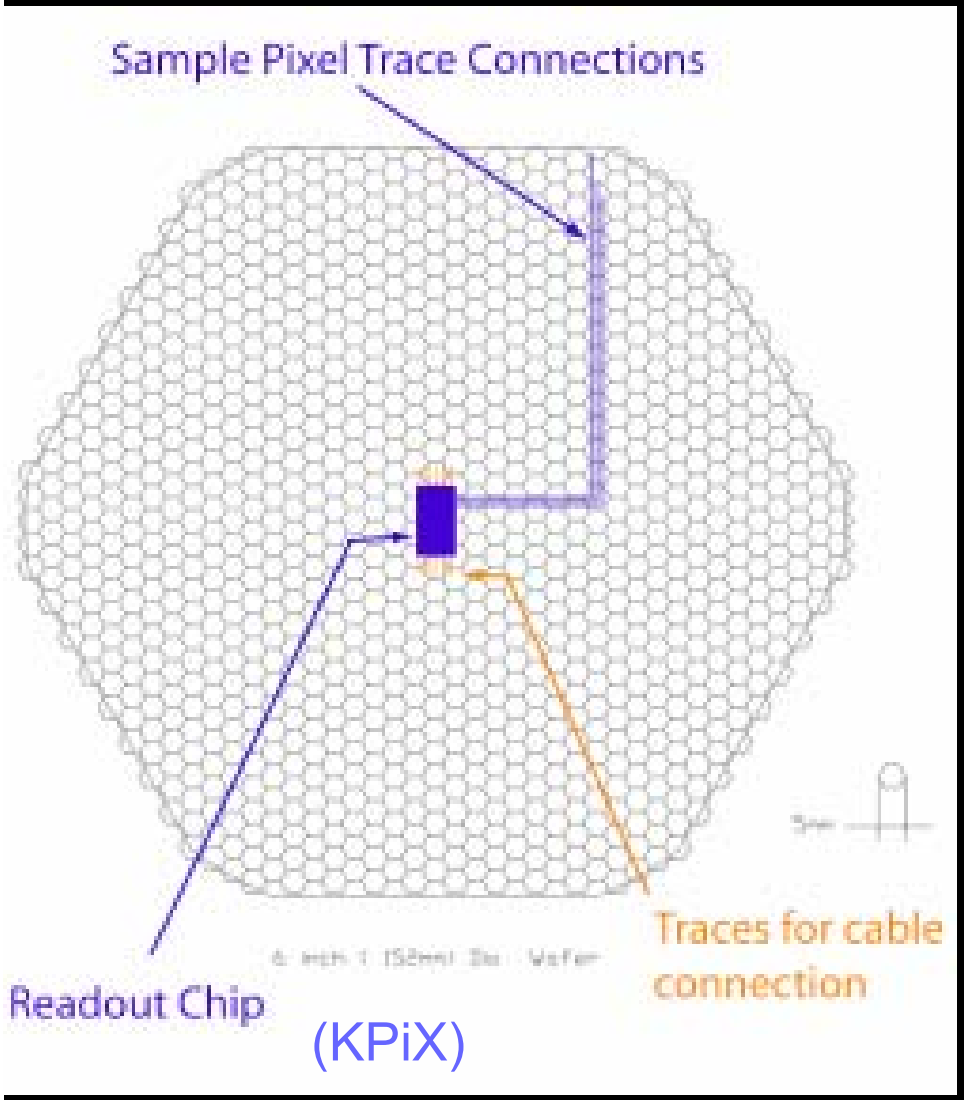


$d = 2.5\text{mm}$, $R_M \sim 17\text{mm}$

$$f_E \simeq \frac{R_{cal}}{\sqrt{R_M^2 + (4d_{pad})^2}}$$

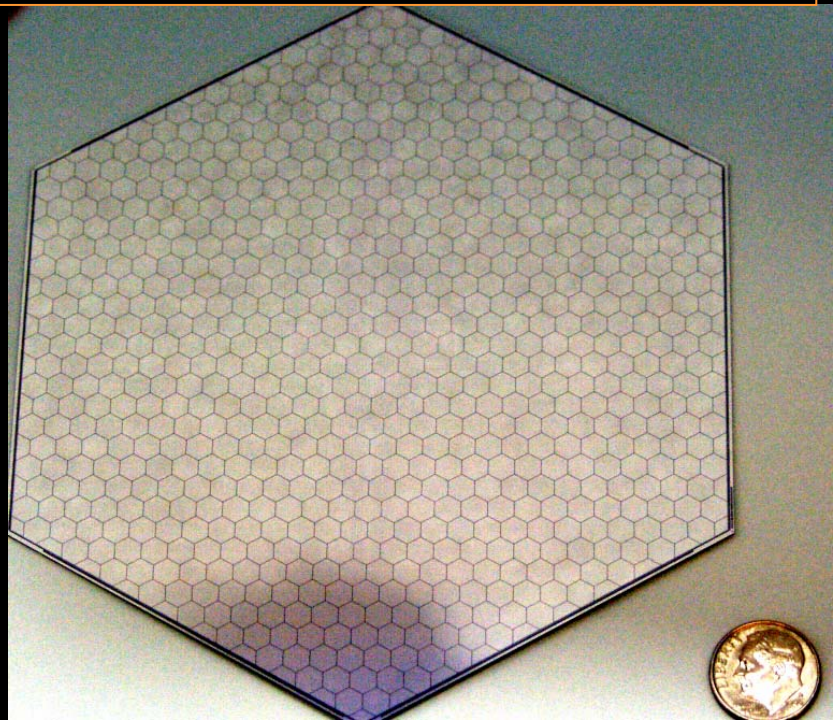
Two EM-shower separability in LEP data with the OPAL Si-W LumCal (David Strom)

Silicon detector layout and segmentation



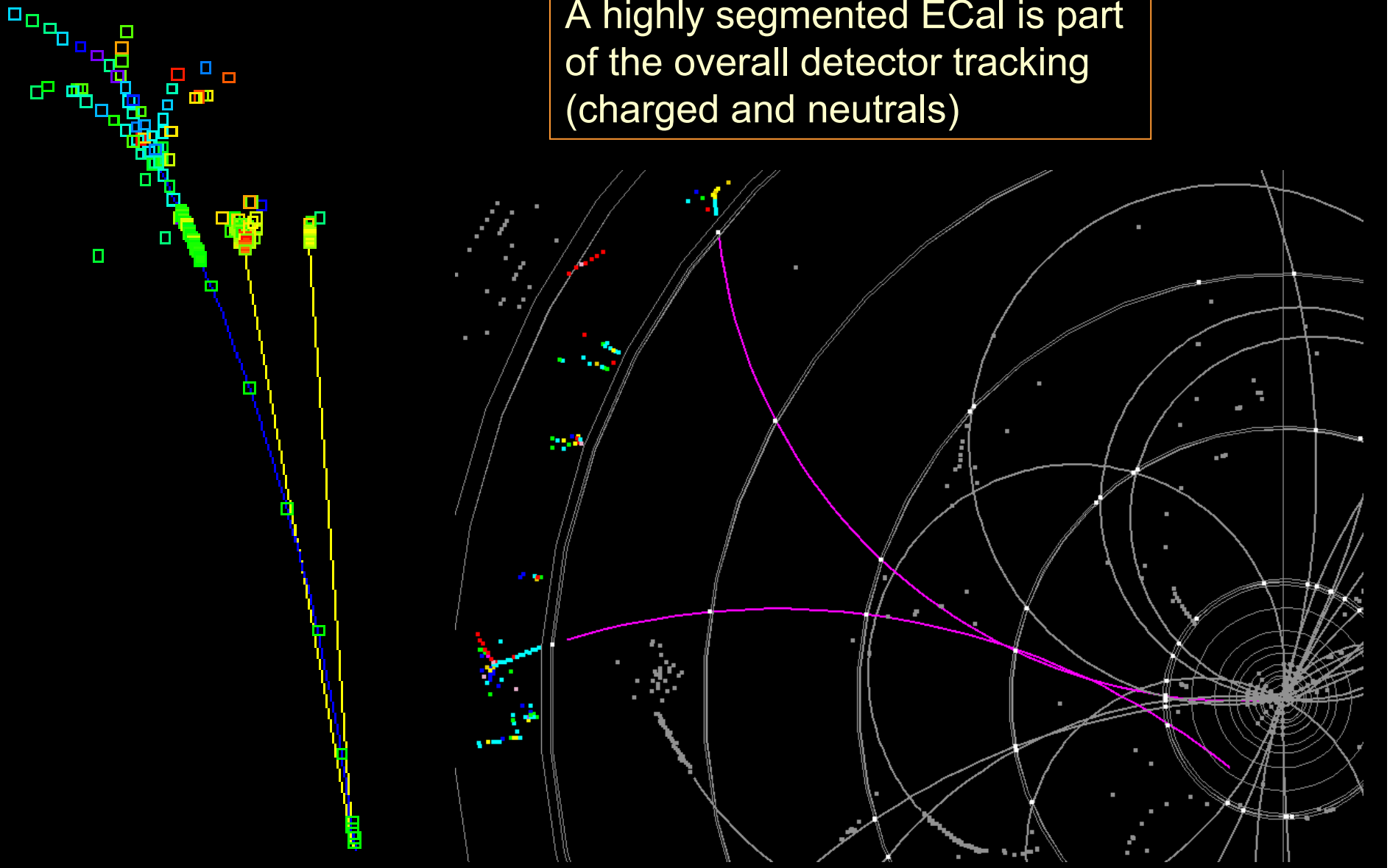
- Silicon is easily segmented
- KPiX readout chip is designed for 12 mm^2 pixels (1024 pixels for 6 inch wafer)
- Cost nearly independent of seg.
- Limit on segmentation comes from chip power (minimum $\approx$ 2 mm^2)

Fully functional prototype (Hamamatsu)



An "Imaging Calorimeter"

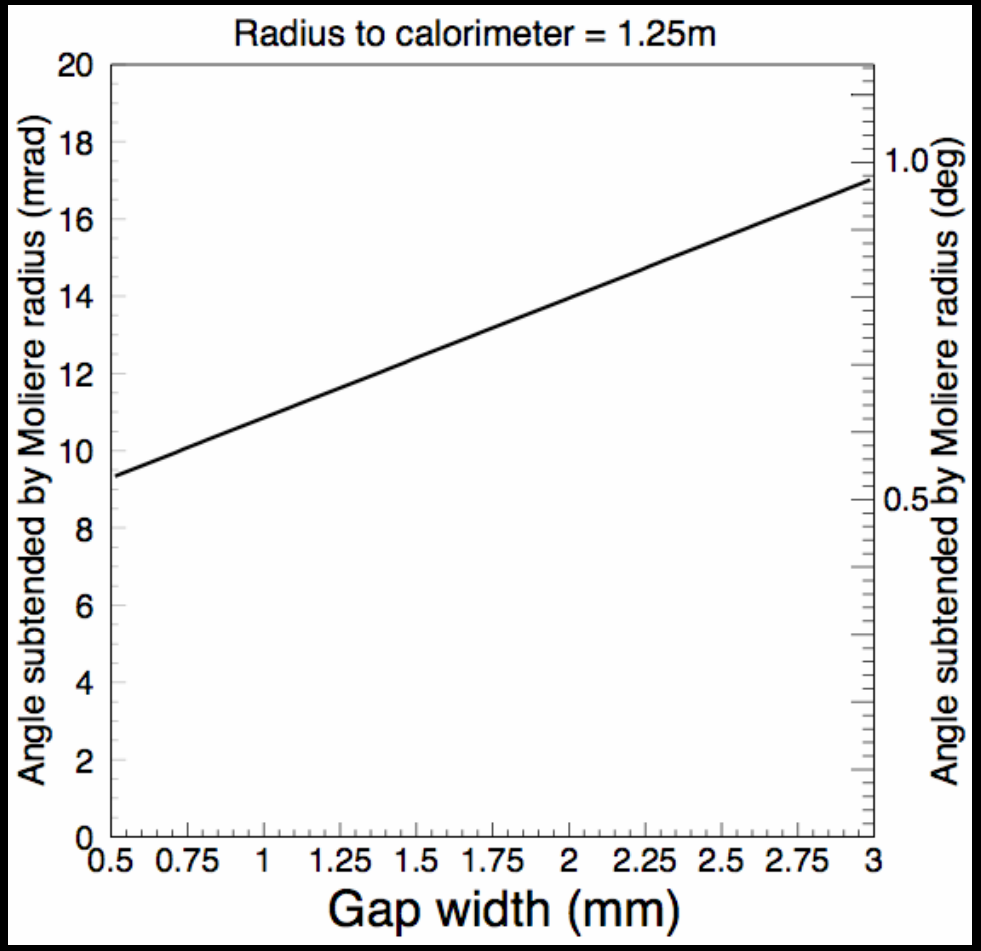
A highly segmented ECal is part of the overall detector tracking (charged and neutrals)



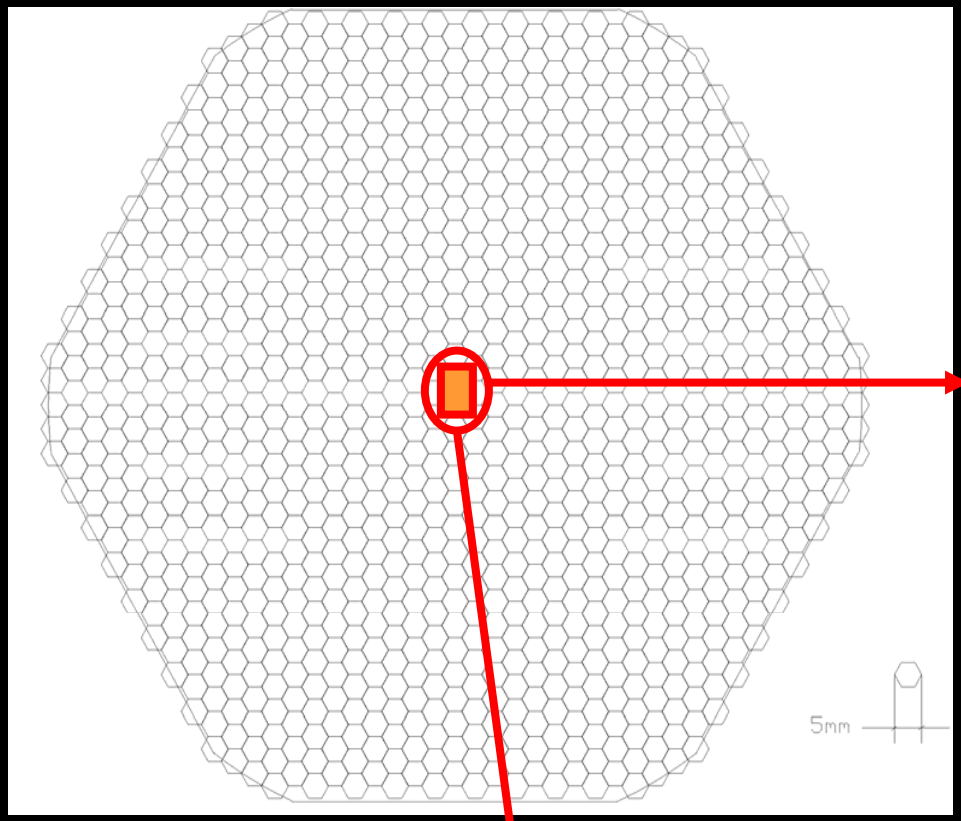
Critical parameter for R_M is the gap between layers

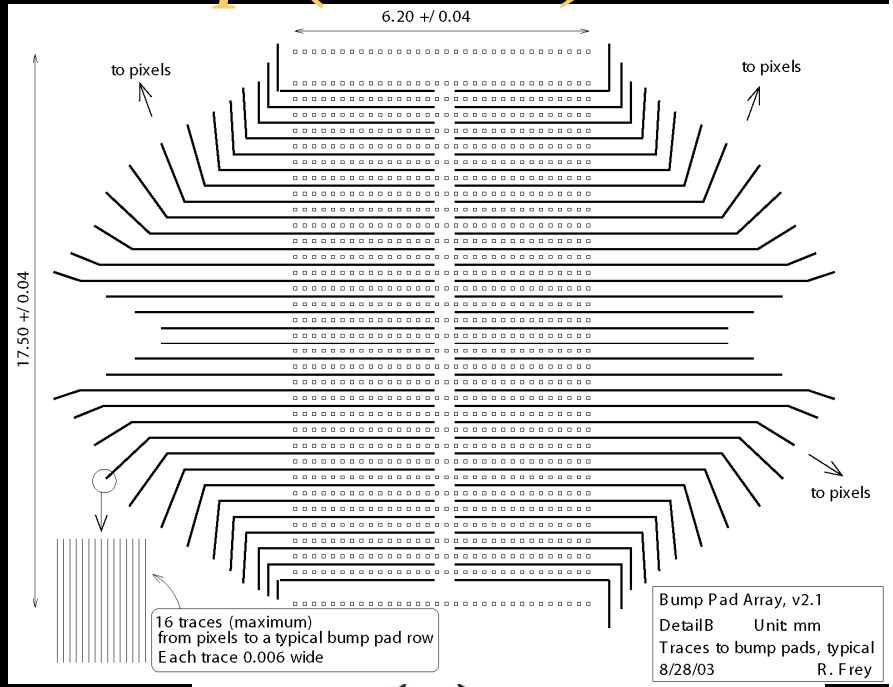
Config.	Radiation length	Molière Radius
100% W	3.5mm	9mm
92.5% W	3.9mm	10mm
+1mm gap	5.5mm	14mm
+1mmCu	6.4mm	17mm

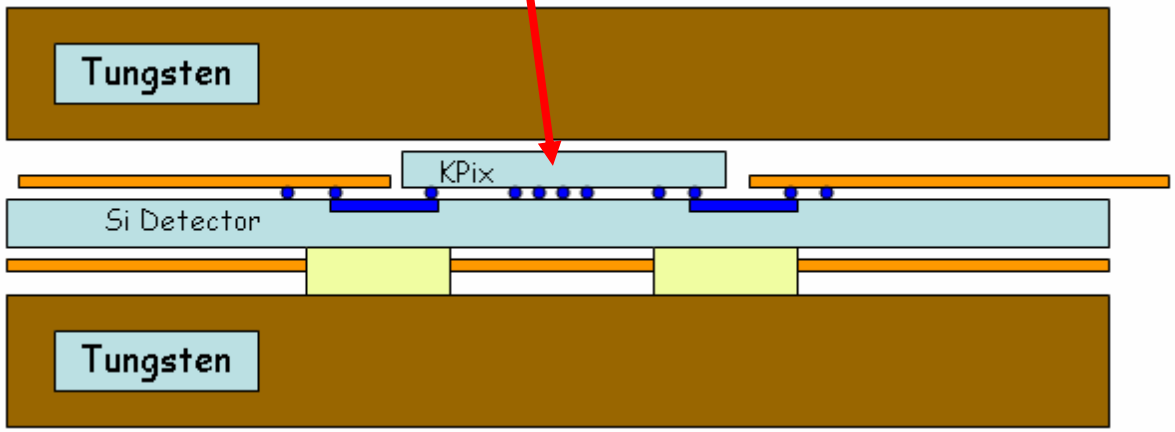
Assumes 2.5mm thick tungsten absorber plates

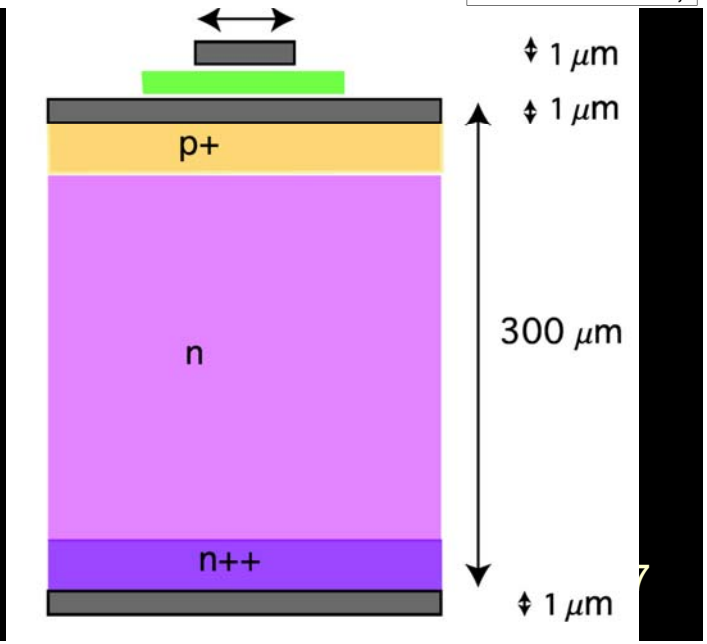


Wafer and readout chip (KPiX)







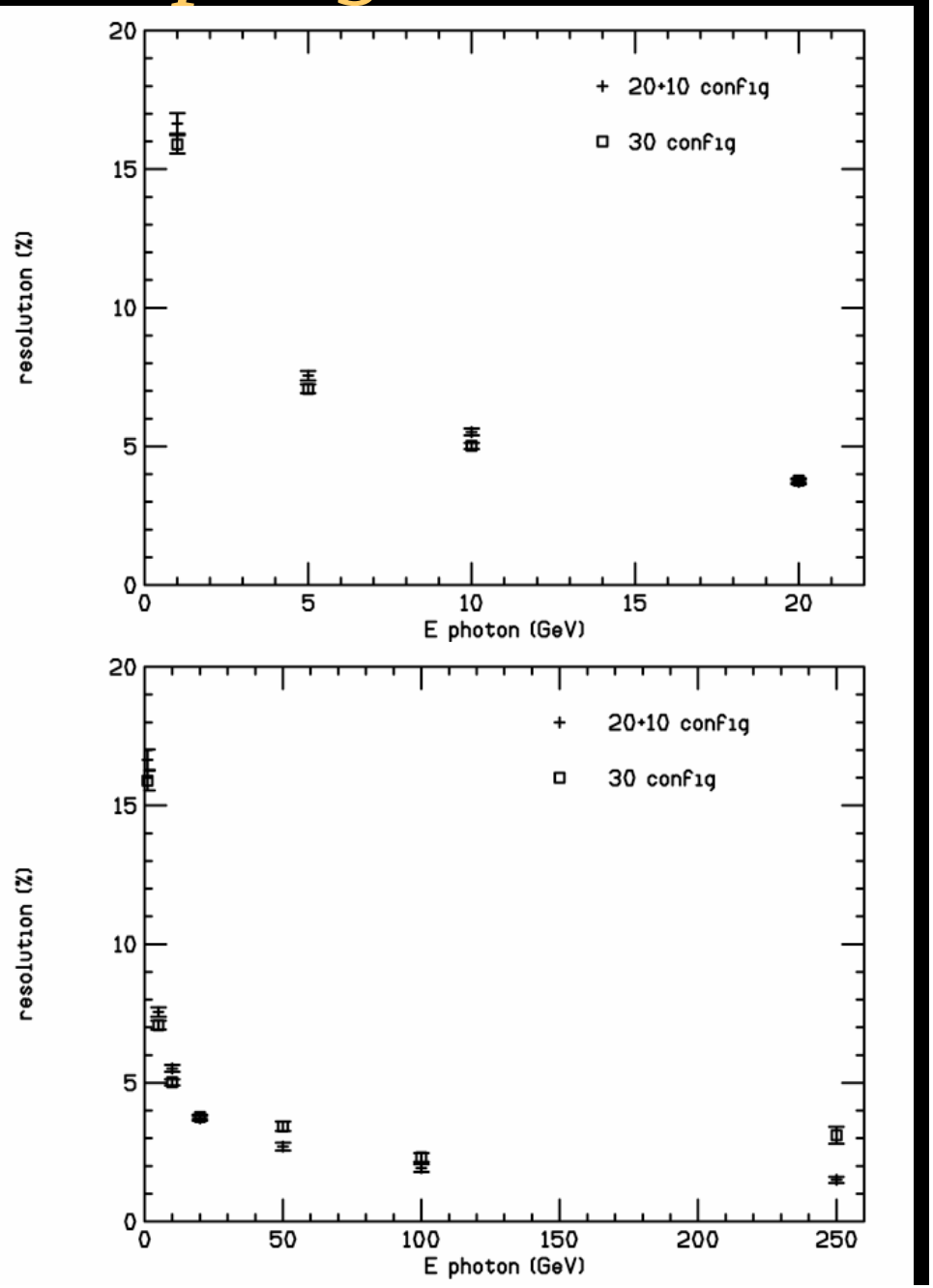


Longitudinal Sampling

Compare two tungsten configurations:

- 30 layers x 5/7 X_0
- (20 x 5/7 X_0) + (10 x 10/7 X_0)

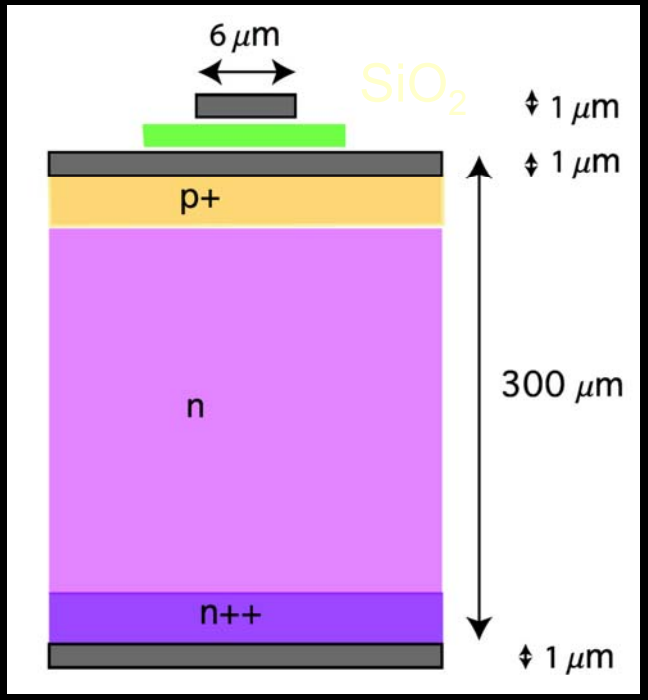
- Resolution is 17% / √E , nearly the same for low energy (photons in jets)
- Better for the 20+10 config. at the highest energies (leakage) ⇒ adopt as baseline



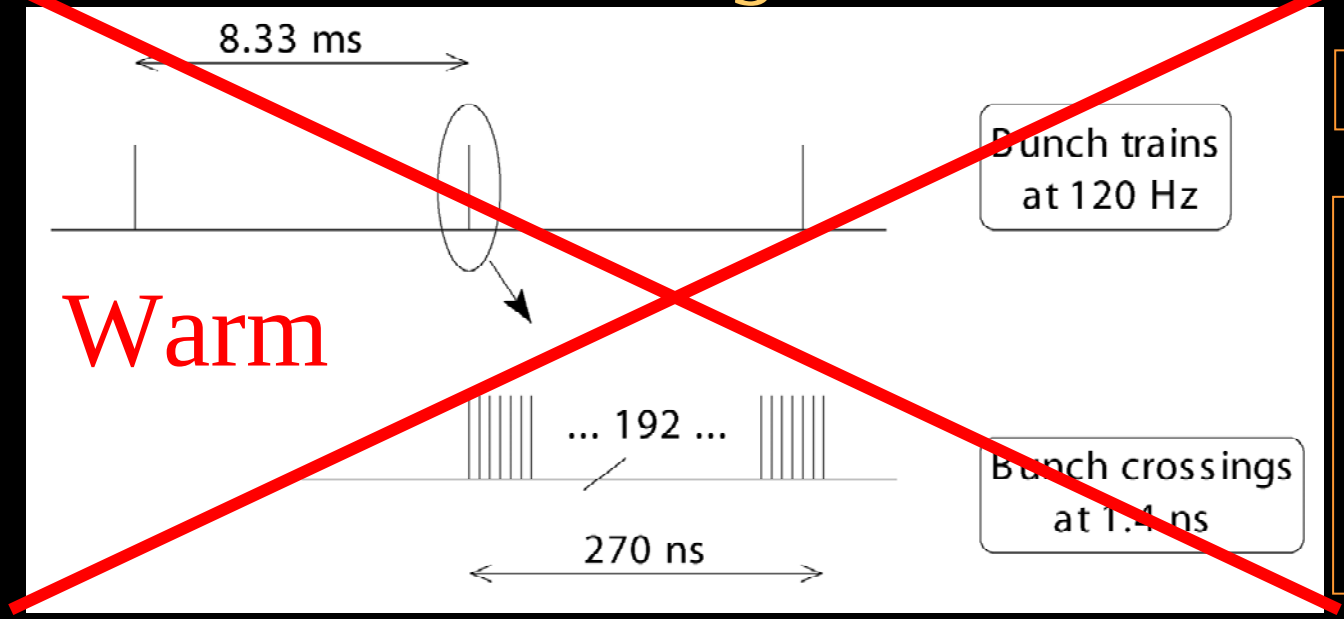
Electronics requirements

- Signals
  - <2000 e noise
  - MIP (300μm Si) → 25,000 e
  - Require MIPs with S/N > 7
  - Large dynamic range: Max. signal is ≈2500 MIPs (for 5mm pixels) 500GeV Bhabha @ shower max.
- Capacitance
  - Pixels: 5.7 pF
  - Traces: ~0.8 pF per pixel crossing
  - Crosstalk: 0.8 pF/Gain x Cin < 1%
- Resistance (traces)
  - designed to be 300 ohm max
- Power
  - If < 40 mW/wafer ⇒ allows passive cooling (as long as power is cycled off between bunch trains)
- Provide fully digitized, zero suppressed outputs of charge and beam crossing (bx) time on one ASIC for every wafer.

Use DC-coupled detectors: only two metal layers (reduces cost)

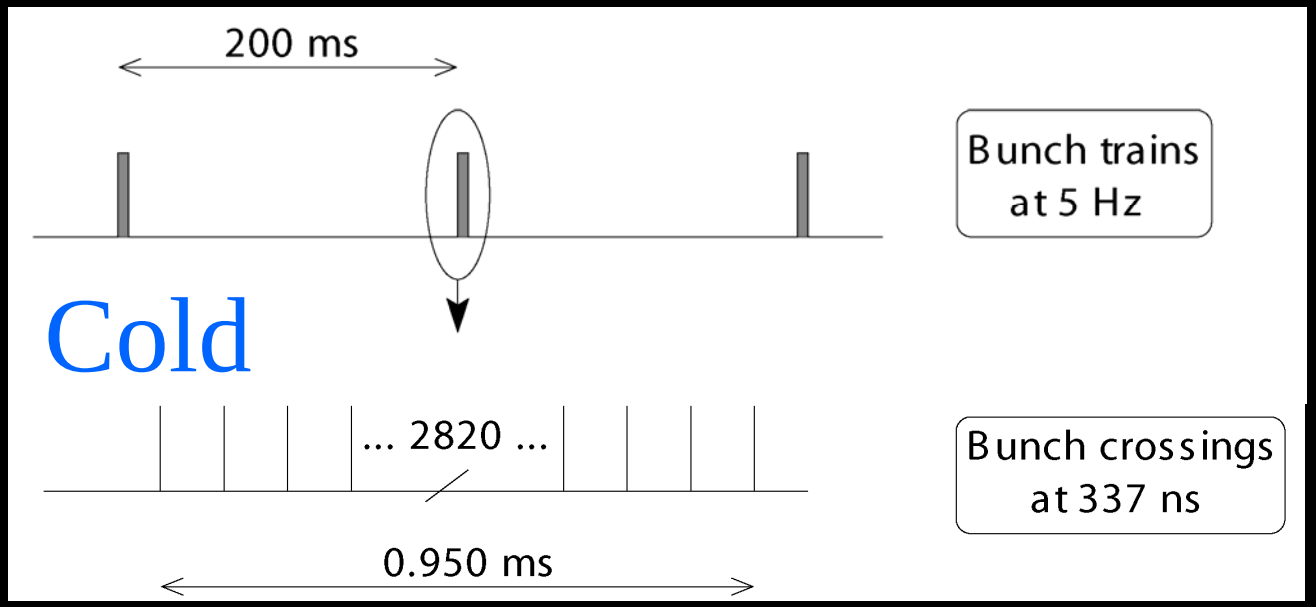


Beam crossing time structure



CALOR04

- Pileup over bunch train
- Or fast timing
- bx live: 3×10^{-5}
- $\Rightarrow$ power pulse



CALOR06

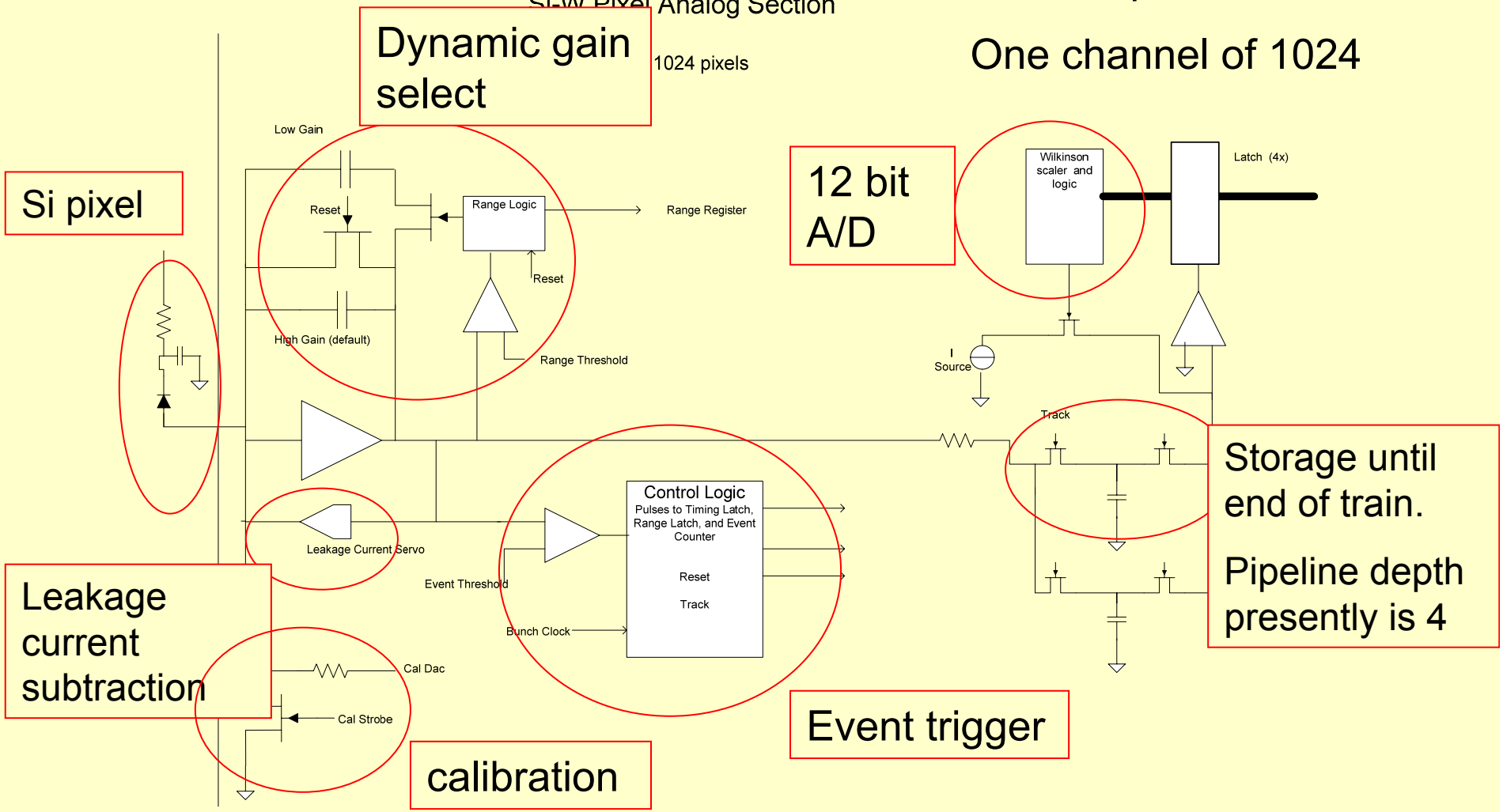
- Fast readouts: OK, no pileup
- pipeline
- bx live: 5×10^{-3}

KPiX chip

One channel of 1024

Si-W Pixel Analog Section

1024 pixels



Simplified Timing:

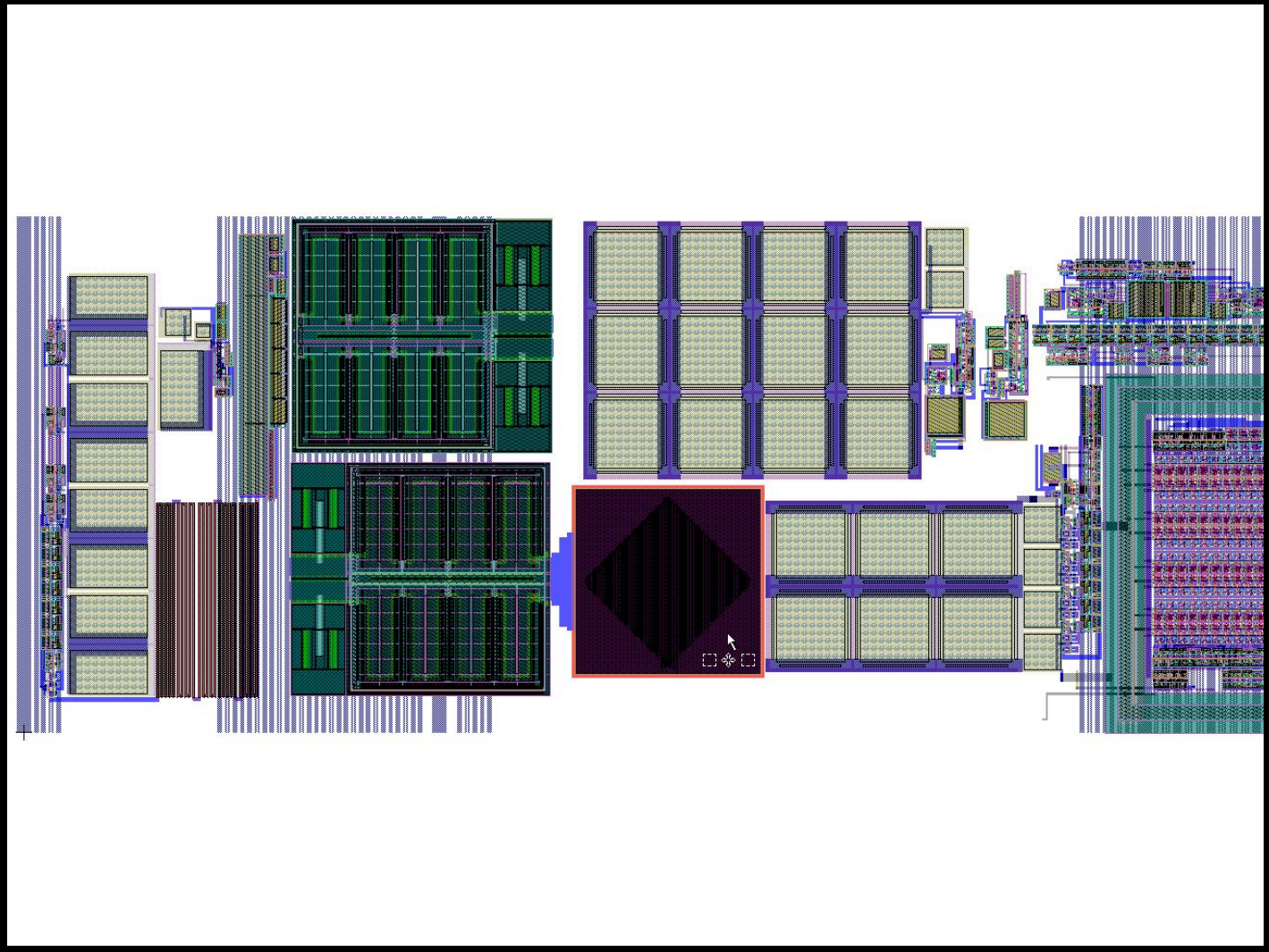
There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit), range latch (1 bit) and Event Counter (5 bits).
The Range discriminator triggers in ~100 ns if the signal exceeds the Range Threshold.
When the glitch from the Range switch has had time to settle, Track connects the sample capacitor to the amplifier output. (~150 ns)
The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor .
Reset is asserted (synched to the bunch clock) . Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.

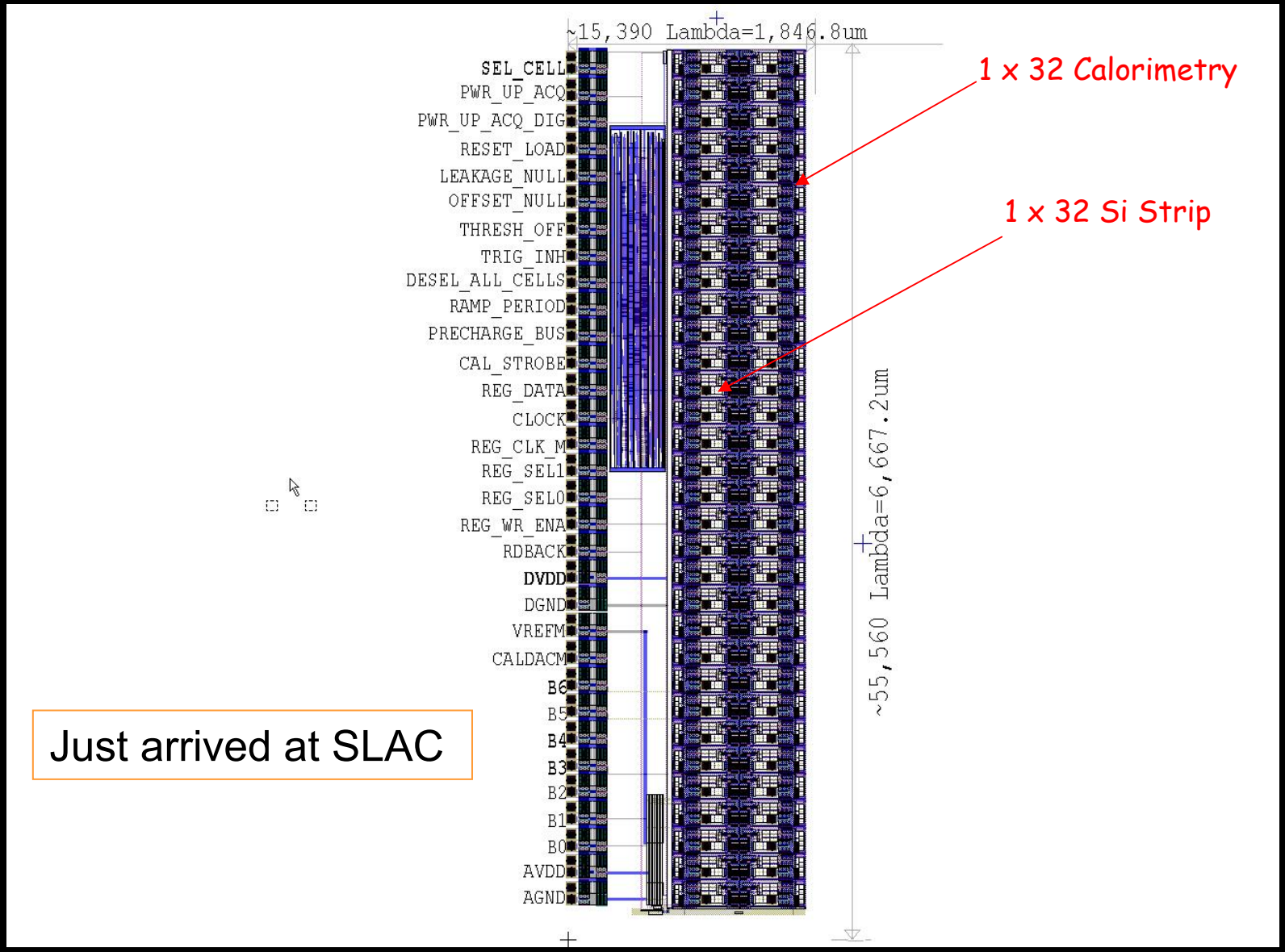
Power

			Cold Train/Bunch Structure				
Phase	**Current (ma)**	**Instantaneous Power (mw)**	**Time begin (us)**	**Time End (us)**	**Duty Factor**	**Average Power (mw)**	**Comments**
All Analog "on"	370.00	930.00	0.00	1,020.00	5.10E-03	4.7	Power ok with current through FET's
Hold "on", charge amp off	85.00	210.00	1,021.00	1,220.00	9.95E-04	0.2	
Analog power down	4.00	10.00	1,020.00	200,000.00	9.95E-01	9.9	
LVDS Receiver, etc		3.00	0.00	200,000.00	1.00E+00	3.0	Receiver always on.
Decode/Program		10.00	1.00	100.00	4.95E-04	0.0	Sequencing is vague!
ADC		100.00	1,021.00	1,220.00	9.95E-04	0.1	
Readout		50.00	1,220.00	3,220.00	1.00E-02	0.5	
Total						18.5	Total power OK

KPix Cell 1 of 1024

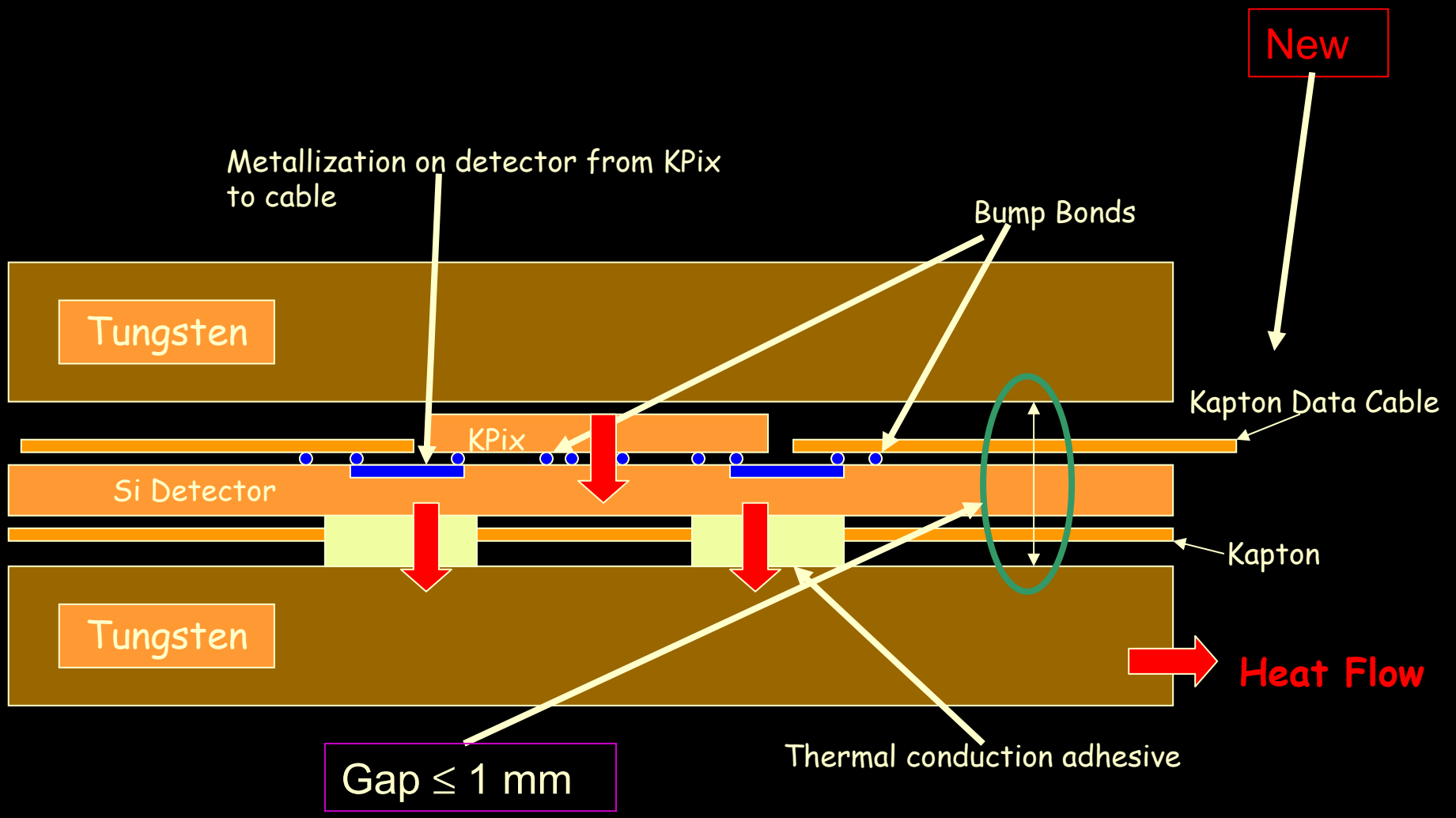


Prototype Layout 1x32

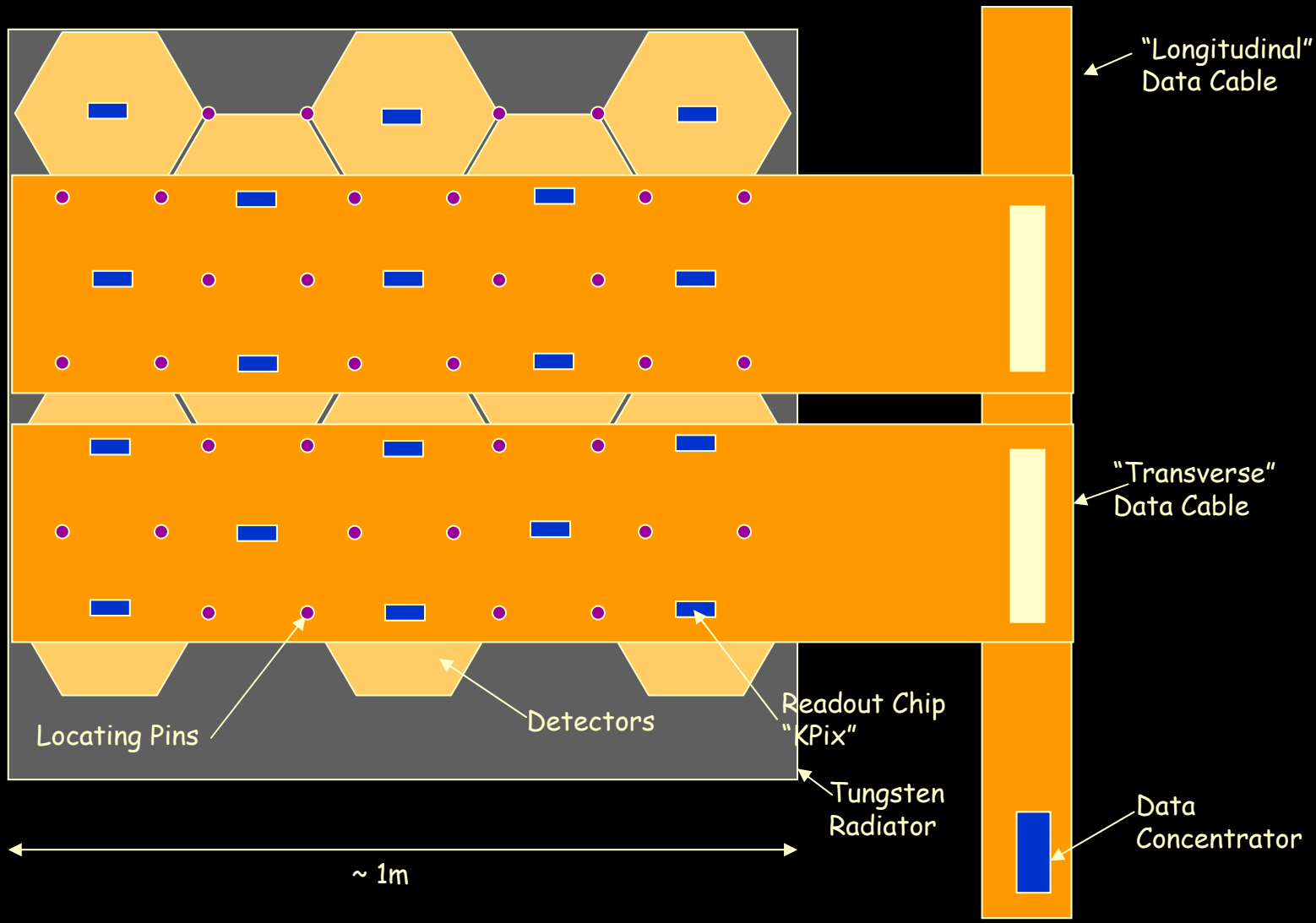


Just arrived at SLAC

ECal schematic cross section

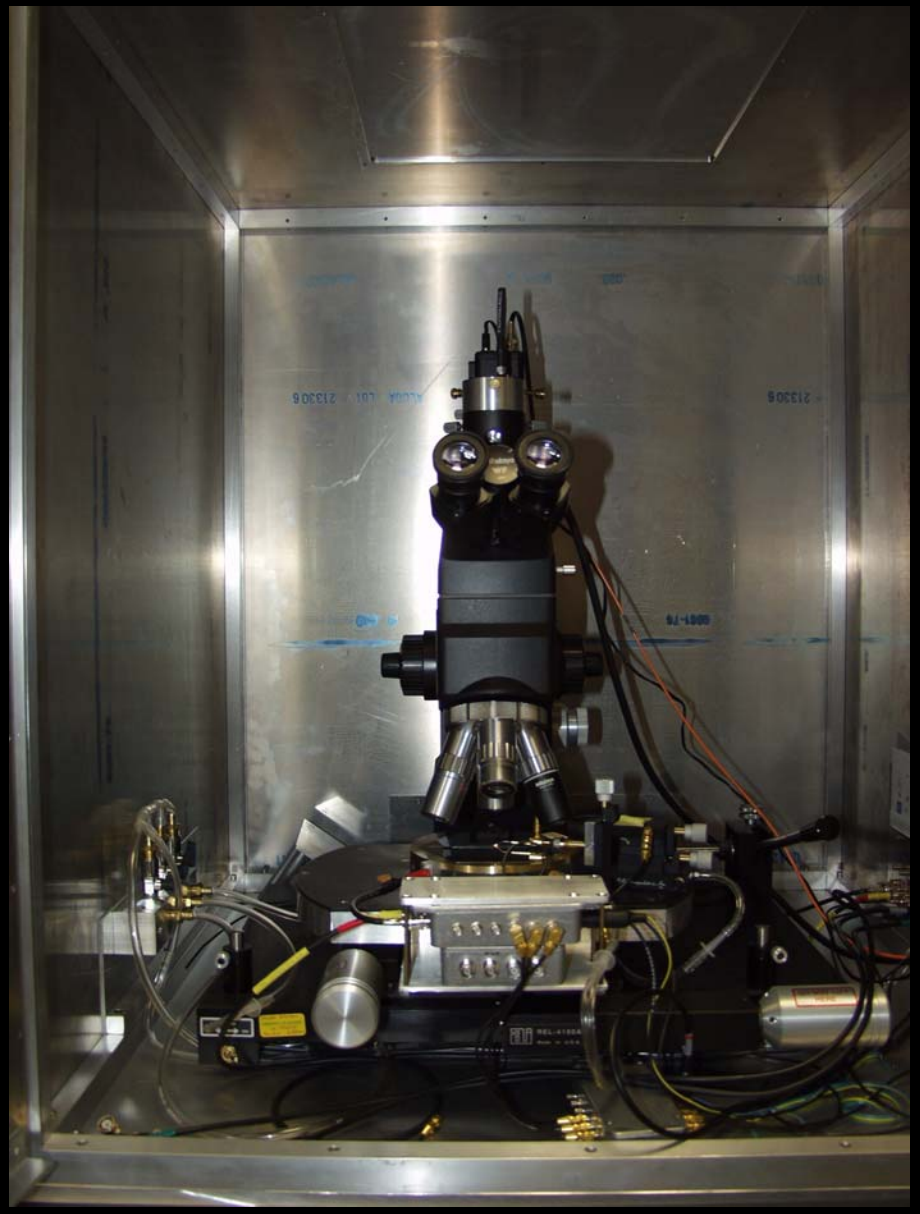


Conceptual Schematic – Not to any scale!!!



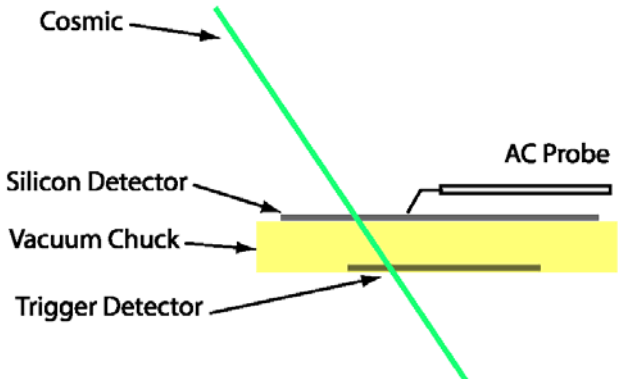
Teststand for cosmics, laser and sources

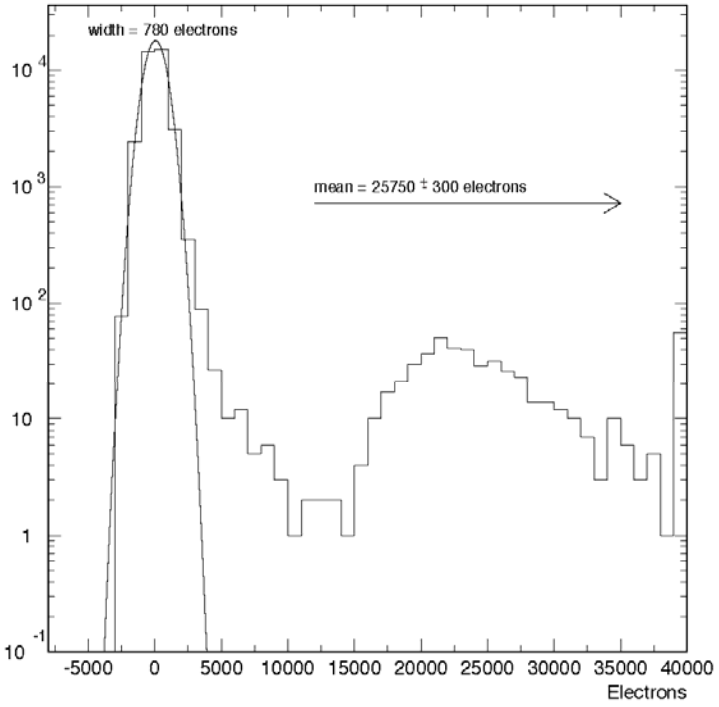
- Modified probe station, allows laser to be target on entire detector
- IR microscope objective used to focus laser to ~10micron spot
- Bias applied to backside of detector using insulated chuck

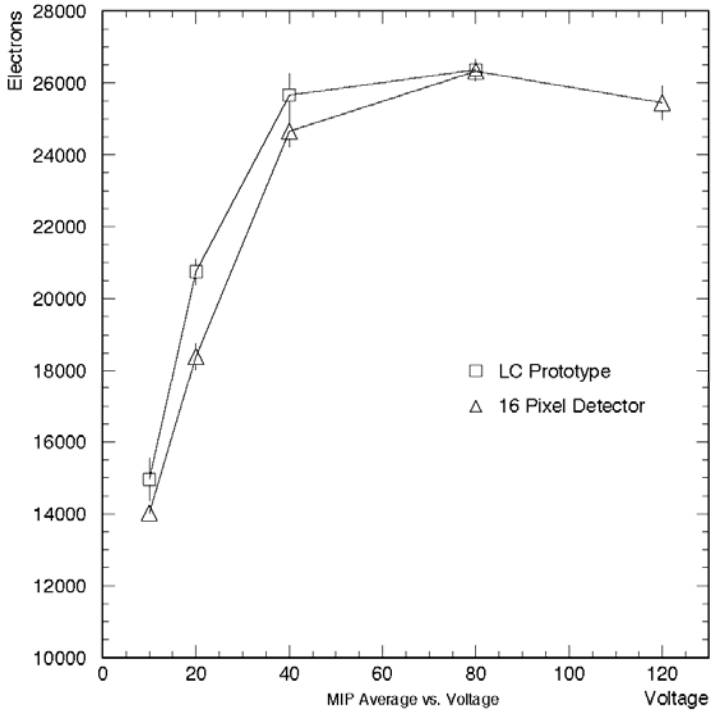


Prototype Si detector studies

Response of detectors to Cosmics
(Single 5mm pixel)
Simulate LC electronics
(noise somewhat better)

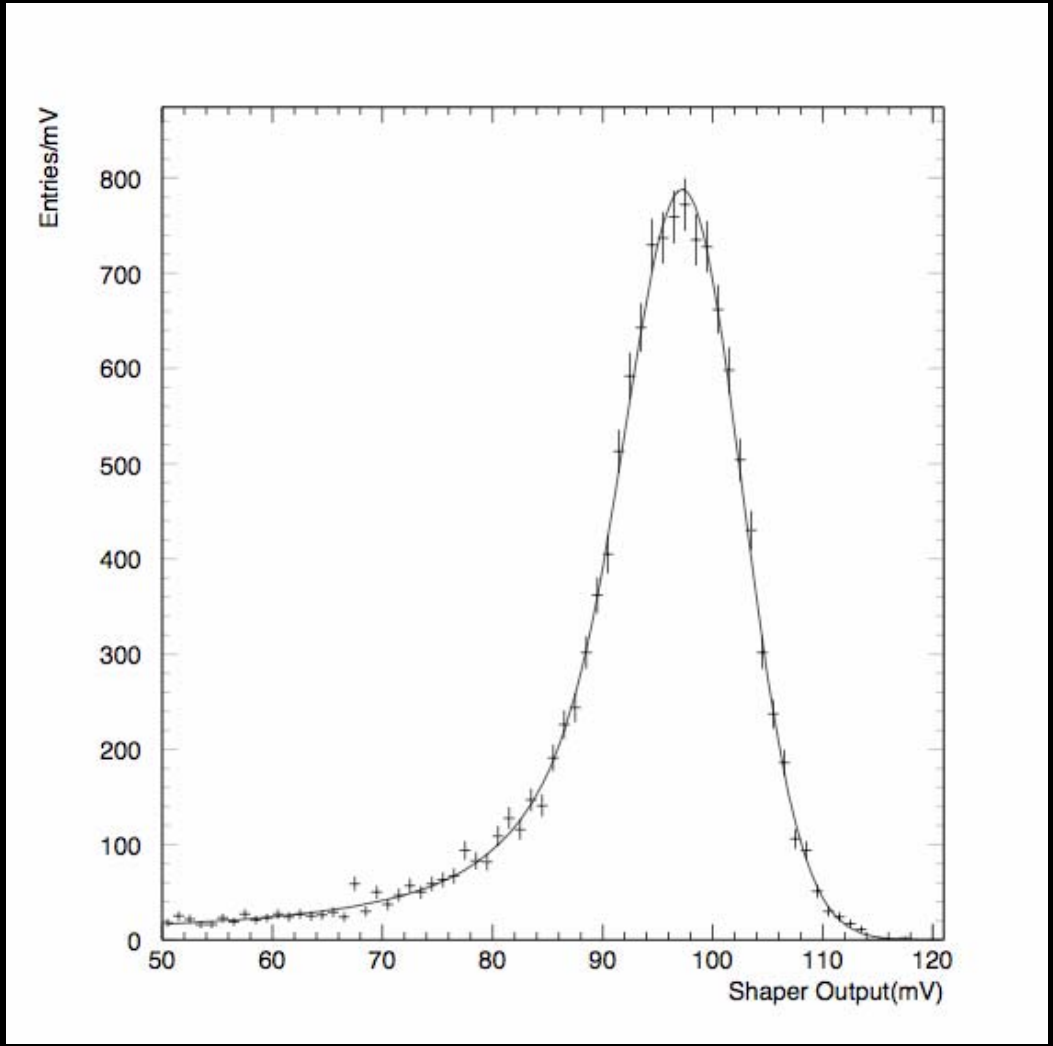




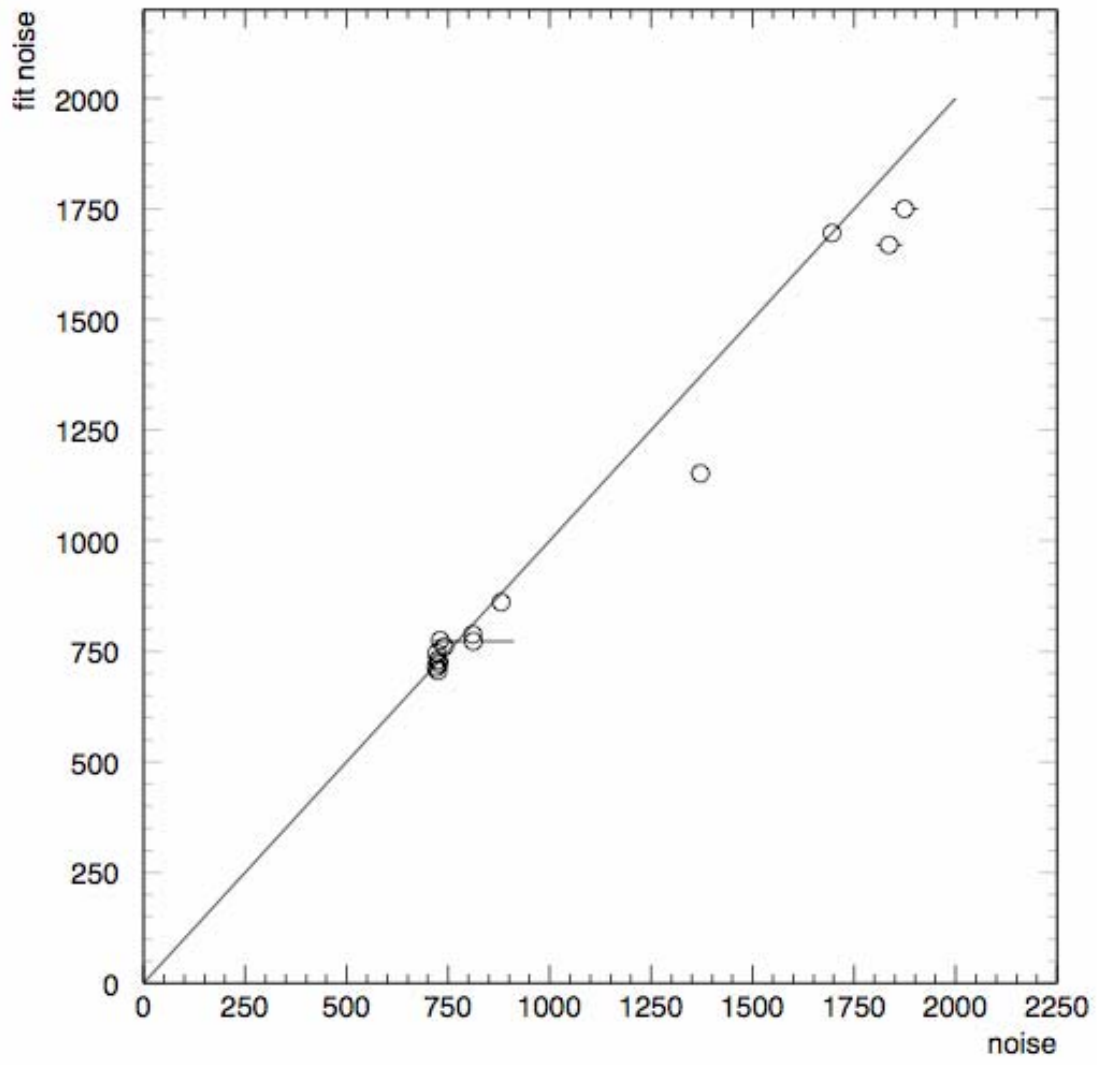


Errors do not include ~ 10% calibration uncertainty (no source calibration)

Response of Detectors to 60KeV Gamma's from Am^{241}



Possible ~1% wafer-wafer calibration?



Noise is consistent with expectation from capacitance and series resistance

Si/W ECal R&D Plan (Outline)

Overall goal: Develop full depth ECal module (≈one wafer wide) which has required functionality for a real ILC detector. Put in test beam(s).

1st round prototype Si detector design, dev., and testing	**complete**
Design, develop, and test fully functional readout chip (KPiX)	**64 channel prototypes in test**
Design and fabricate kapton readout cable	in design
Bump bonding trials and electromechanical development	2006
Design and order 2nd round detectors (≈40) for module	2006
Develop and procure KPiX-round 2, concentrator boards	2006
A first technical beam test (electrons)	Late 2006 ?
Order full 1024 channel KPiX	2007 ?
Fabricate ECal module; test in electron beam: determine EM response and resolution	**2007 ?**
ECal module + HCal module in hadron beam (presume FNAL) – Geant4 validation/calibration	**2008 ?**
Develop ECal mechanical design in parallel	ongoing

Summary

- A narrow gap silicon-tungsten detector is an attractive solution for a highly-segmented (transverse and longitudinal), compact ($r_{Moliere}$, X_0) detector for ILC physics requiring individual particle reconstruction.
- A highly integrated electronic readout can provide a practical realization of such an ECal.
- The development of such a readout chip is well underway. (Prototypes in hand.)
- First round of prototype silicon detectors perform as expected. Detectors can be produced with workable values of stray capacitance and series resistance.