Where do we go from there: SiLC and its main issues

SiLC Satellite Meeting, November 18th 2005

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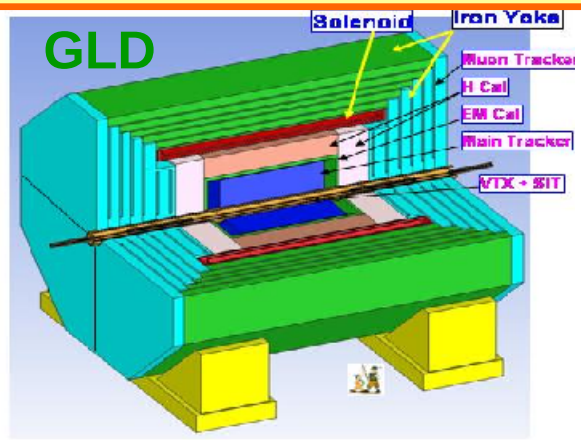
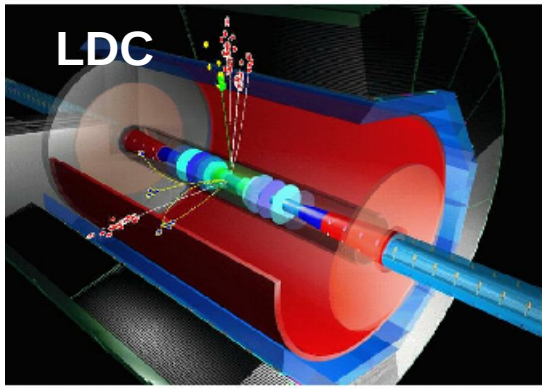
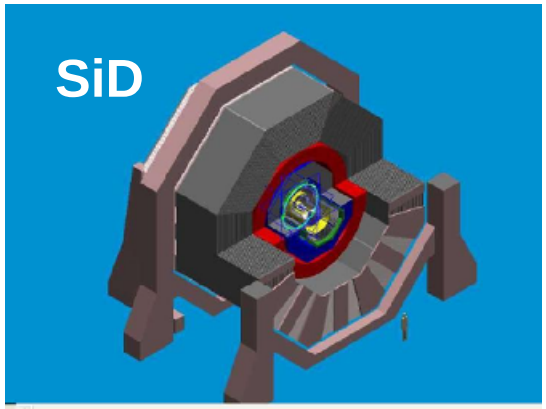
R&D Goals

SiLC is a generic R&D collaboration to develop the next generation of large area Silicon Detectors for the ILC; It applies to all the detector concepts and indeed gathers teams from all 3 detector concepts:







- **Very high precision on momentum and spatial measurements**
- **Low material budget**
- **Robustness**
- **Easy to build and to work with**
- **Low cost**

❖ ***SILC R&D offers a unique framework to compare tracking performances between the various detector concepts.***
❖ ***Main difference between the detector concepts = tracking system***

To achieve these goals:

- R&D on sensors
- R&D on Electronics
- R&D on Mechanics

together with developing the appropiate tools:

- Test benches
- Calibrations and Monitoring
- Simulations
- Test Beam

R&D on Sensors

- **Silicon strips are the baseline with:**
- **Larger size wafers, single and double sided**
- **Thinner/Thinning**
- **Smaller pitch**
- **High yield**
- **Eventually different shapes**
- **Possibility to use new technos in some regions:**
- **Pixelization: Pixels, DEPFET, MAPS/FAPS, SOI**

In order to achieve this R&D:

- **Lab test bench for full characterization of the sensors (most Labs in SiLC) *with a continuous upgrade*.**
- **Fabrication line for new ideas on sensors at various Institutes (Korean Institutes, Helsinki U., IMB-CNM/CSIC)**
- **Process Quality Control and sensor characterization (Vienna, Karlsruhe, Korea, Helsinki)**
- **Medium size fab line for small size production (looking at different such places, in Europe and Asia for the time being)**
- **Transfer to Industry for full production (presently Hamamatsu but could evolve).**

R&D on Electronics

The Si tracking system includes: a few $100m^2$, a few 10^6 strips
Events tagged every bunch (300ns) during the overall train (1 ms)
Data taking/pre-processing ~ 200 ms
Occupancy: < a few %

Requested features for FE chip:

- Low noise preamplifiers
- Shaping time (from 0.5 to 5 µs, depending the strip length)
- Analogue sampling
- Highly shared ADC
- Digitization @ sparsification
- Very low power dissipation
- Power cycling
- Compact and transparent
- Choice of DSµE & go to VDSM

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First LPNHE prototype fulfills most of these requirements

Other electronics issues:

- Time measurement
- Calibration/Monitoring of the electronic chain
- Connectics
- Cabling
- Integration into DAQ
- Data taking/pre-processing
  - ✓On detector
  - ✓Outside detector
  - ✓Bunch tagging

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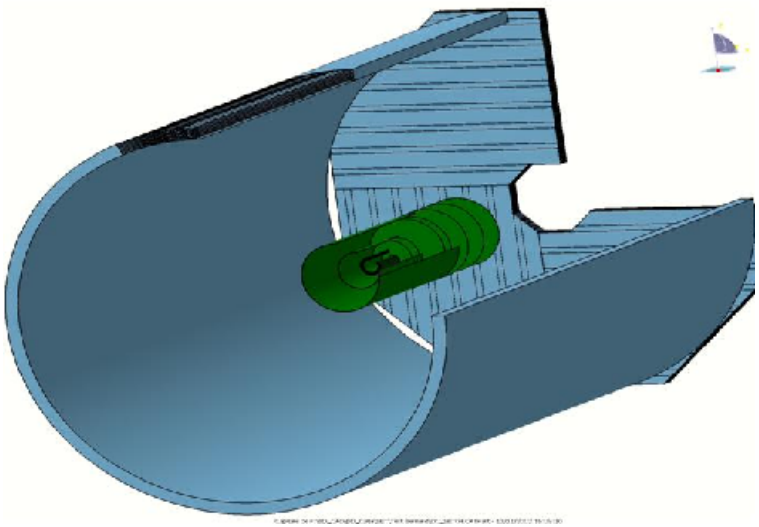
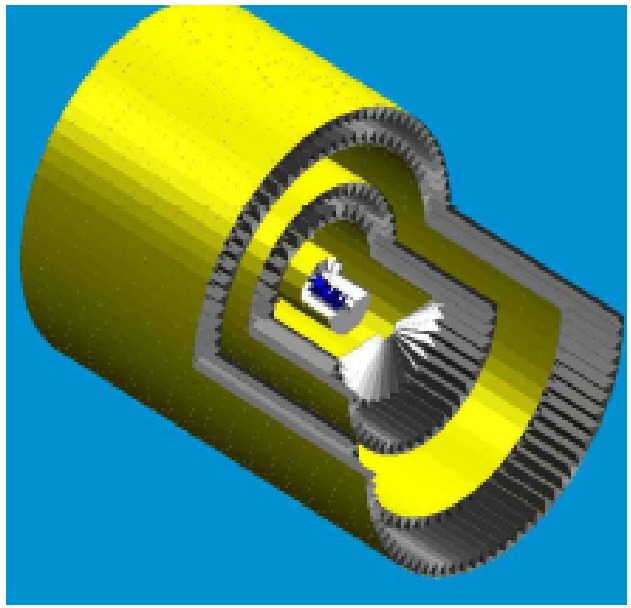
Will be discussed at the SiLC Meeting, Friday Nov. 18th



R&D on Mechanics concentrates on:

- CAD design of Si tracking components: essential for baseline design studies of detector concepts
- Elementary module design in close collaboration with FE electronics designers
- Large structure: robust, light, easy to build
- Materials
- Positioning & alignment
- Cooling
- Robotisation & Industry transfer
- Integration issues

For all these items new solutions must be found



The tools:

- **Lab test benches:**

  ***Dedicated test bench to be developed to test: VDSM chips, cooling studies, position monitoring and alignements, sensor characterization etc… Facilities already existing in some case have to be further developed/adapted to new developed techniques*.**

- **Position Monitoring and Alignment**

  (Michigan U. , IFCA-Santander)

  Presently two complementary systems: C. Rivero's presentation at SiLC Meeting on Friday.

- **Simulations *(see next & M. Berggren's talk)***
- **Test beams *(see next & Z. Dolezal's talk at SiLC meeting)***

The program prepared
for today by Thomas Bergauer,
Manfred Krammer and ASN
tries to cover all these topics.
Manfred Krammer had the idea to
organize this first collaboration
meeting as a satellite meeting to
this ECFA ILC Workshop.

9h -10h	***What are we learning from:***
25’	CMS experience: ***Gabriella Pasztor (CERN)***
25’	ATLAS experience: ***Salvador Marti (IFIC-Valencia)***
10’	***Where do we go from there: SiLC and its main issues***
10h- 11h	**R&D on sensors**
	▪ New strip sensors developments (larger wafer, thinning..) ***and***
20’	New pixel technologies for large surface: ***M. Merkin***
20’	***(Moscow.St.U.) and Steve Worm (Rutherford Lab)***
20’	▪ Quality control: ***Thomas Bergauer, HEPHY-Vienna***
11h-11h20	***Coffee/Tea break***
11h20-1h	**R&D on Electronics**
30’	▪ Very deep sub micron F.E. electronics: ***J. F. Genat, LPNHE***
20’	▪ Readout issues: ***Ledu (CEA Saclay)***
30’	▪ Pitch adapters, packaging, cabling: new techs ***M.Lozano, CNM***
20’	▪The UCSC Font End Chip: ***Bruce Schumm, UCSC***
1h – 2h	***Lunch break***

2h -3h30 15’ 20’ 20’ 15’ 30’	**Mechanics R&D** ▪ CAD design for the various Si tracking components: >> The Si Tracker in the SiD concept: ***Bill Cooper (FNAL)*** >> The Si Tracker in a Large Detector: ***H. Yamamoto*** ▪ Elementary modules: from tiles to ladders: ***B Cooper +F. Kapusta*** ▪ Thermo-mechanical studies: the cooling issues ***A. Savoy-Navarro*** ▪ Position Monitoring and Alignment systems: ***Celso Rivero IFCA & for K. Riles and Hai-Jun Yang (University of Michigan)***
3h40	***Coffee break***
4h00 – 20’ 20’	**Simulation studies: First performance studies of jet rejection using a pixel based detector: *Marco de Mattia (Padova U.)*** **General discussion on full simulation issues GEANT4 based**
4h40- 5h10	**Test benches/Test beams: *Zdenek Dolezal, Charles U. Prague***

Last but not least: let’s fix the next meeting!

Important coming issues: DOD in March and CDR of detector concepts end 2006; Plus forthcoming test beam(s)