Front-end electronics for the LPTPC

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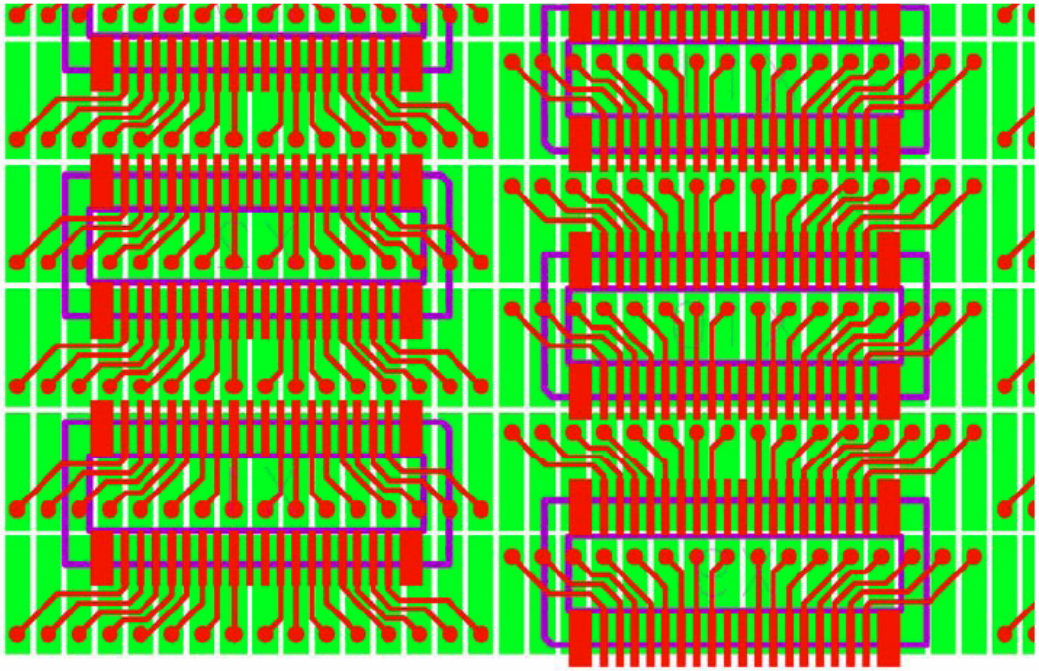
- Connectors
- Cables
- Alice readout electronics
- New developments
- New ideas
- Open questions

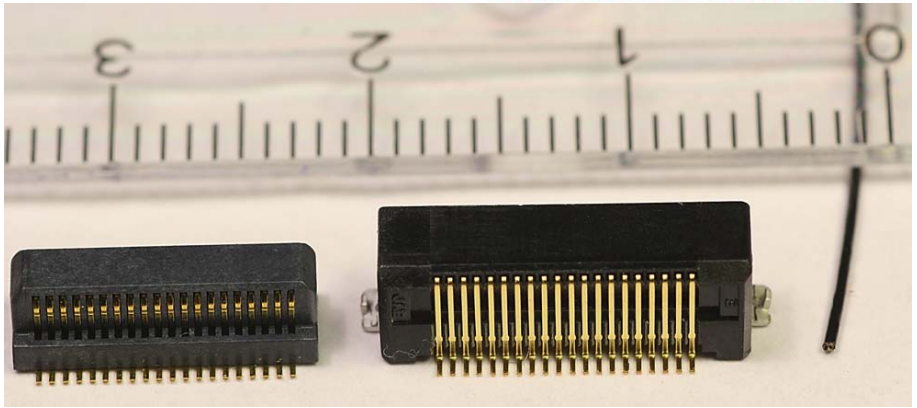
Starting point: min pad size 1 x 4 mm^2

Requirements: highest possible flexibility in terms of pad geometry and shape of pad panels
$\Rightarrow$ Small modules (i.e. small connectors)

Proposal: 32 channels modules, where each channel corresponds to an area of around 4 mm^2
- Japan Aviation Electronics offers a 40 pin connector with 0.5 mm pitch and the dimensions 13.9 x 4.7 mm^2. Thus, this connector allows additional 8 pins for grounding.

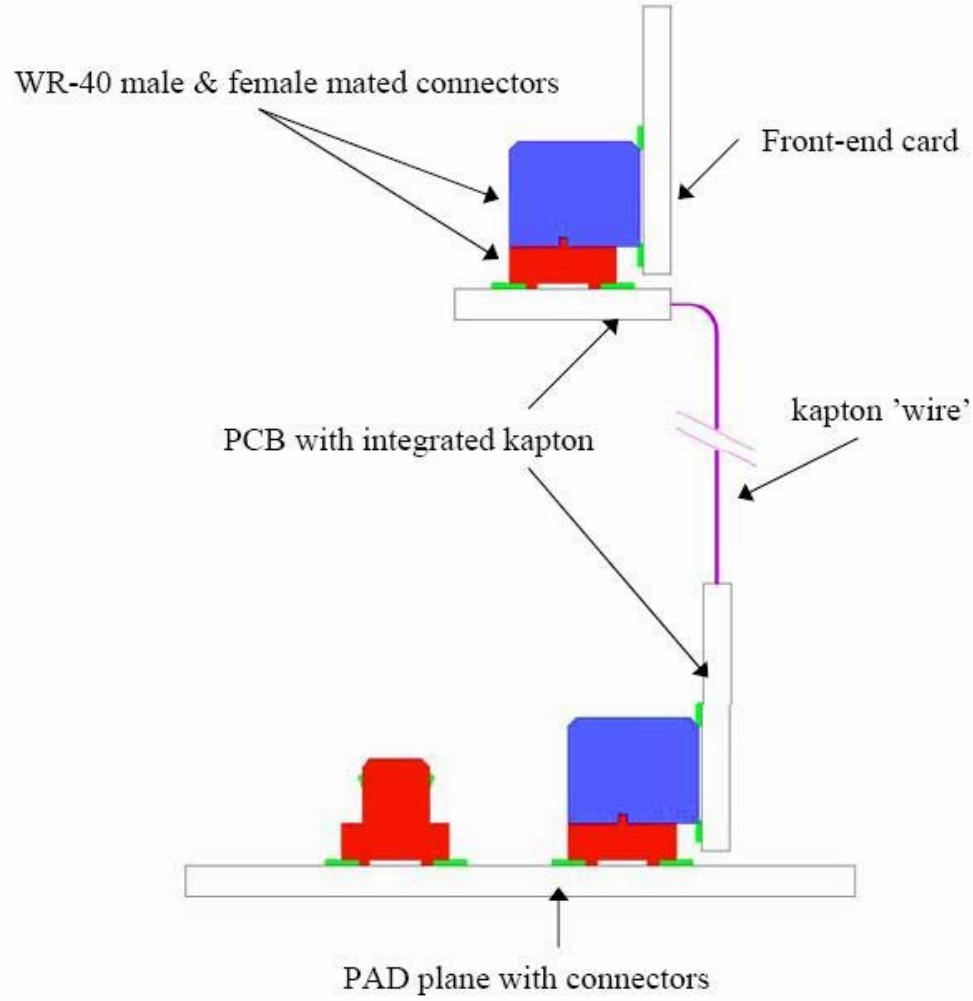
Example of signal routing from 1x4 mm² pads to the WR-40S connector





In case the front end card is connected via cables the arrangement may look the following way ⇒

However the front end card can also connected directly onto the pad plane



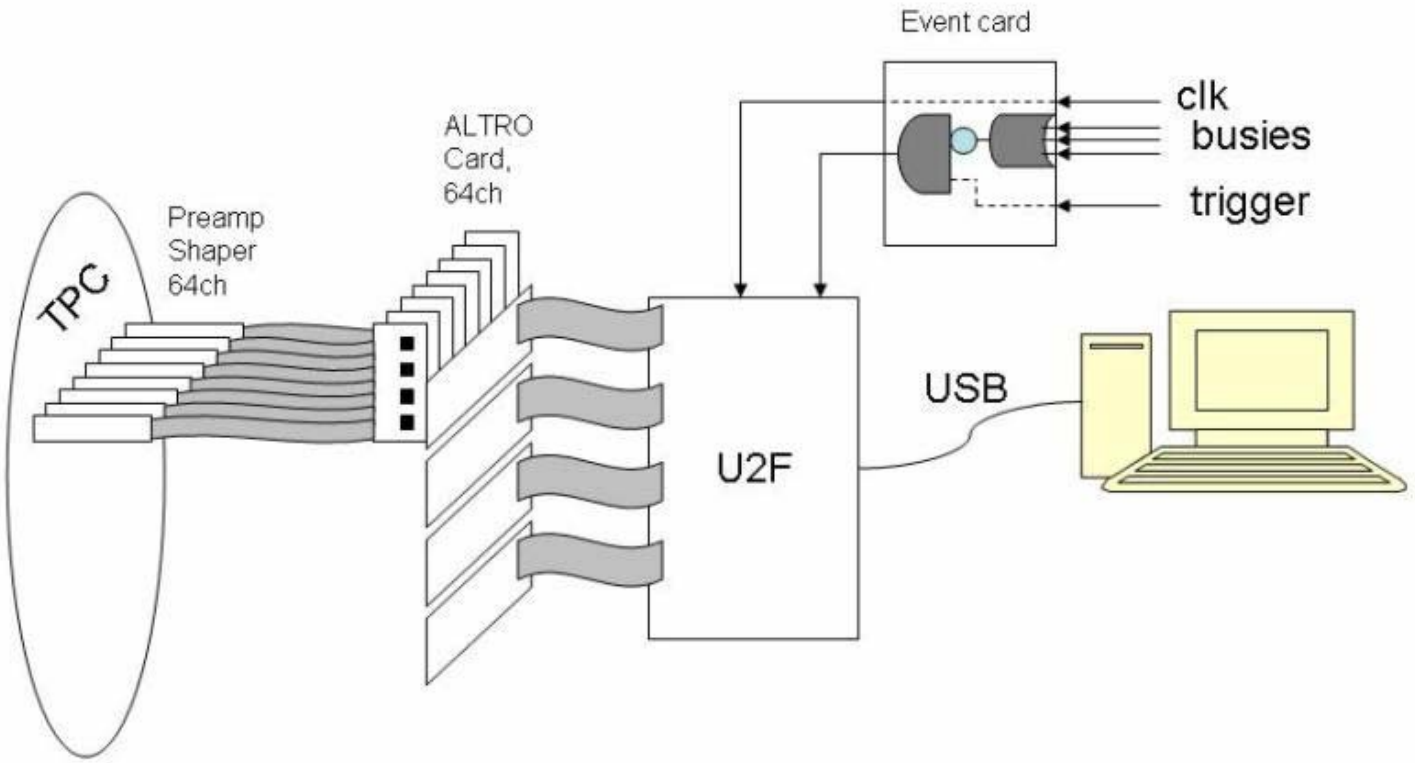
The general test concept (as presented at NIKHEF)

The intention is to build a modular electronic read-out system which offers a flexibility to test various types of avalanche read-out techniques and pad geometries.

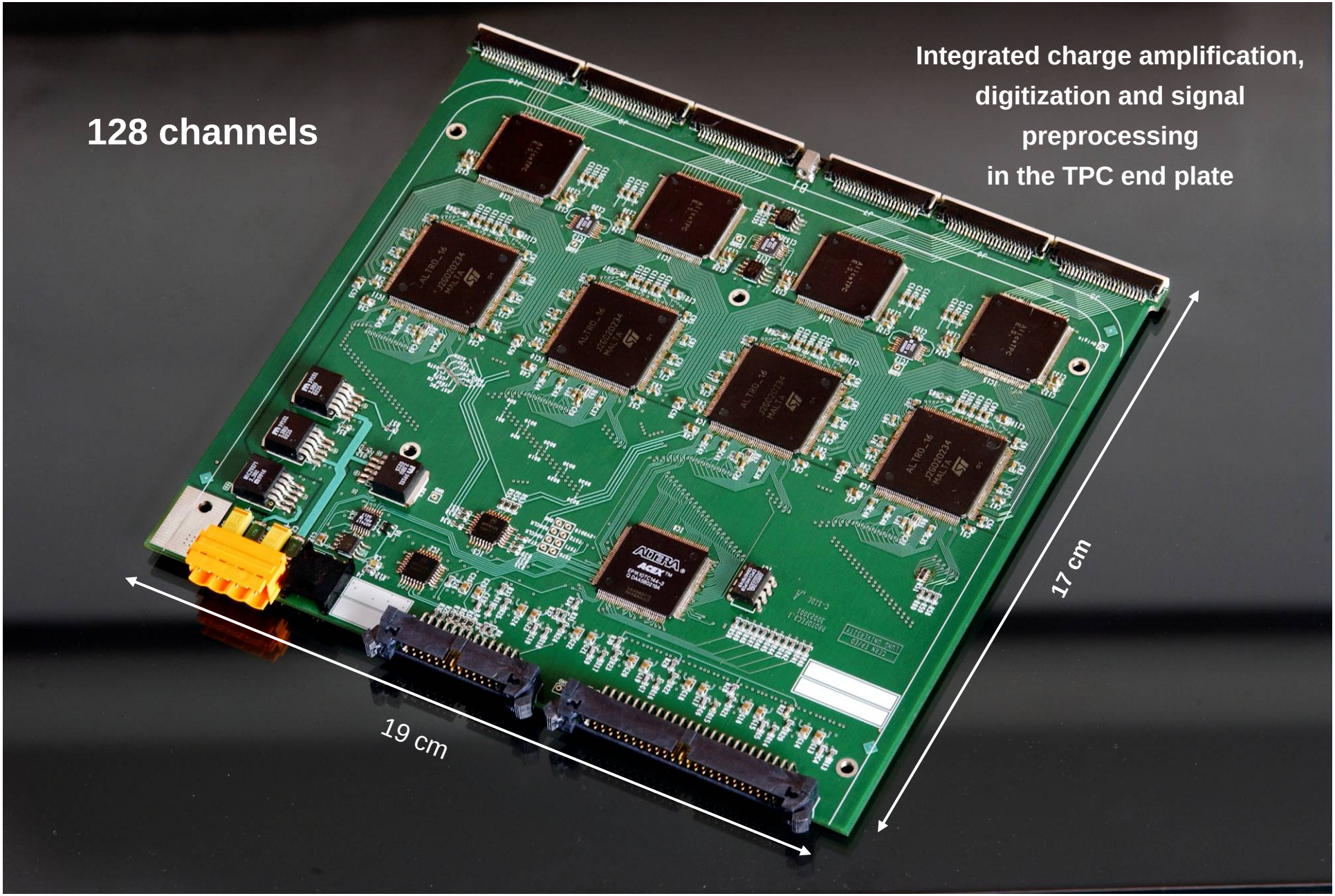
- The read-out electronics should be dismountable from the pad board such that it can be easily moved from one panel to the next
- The amplifier board should be directly attached to the pad board via a connector
- The analogue and digital electronics should be mounted on separate cards connected by short ribbon cables
- The DAQ system should be flexible, such that it can be duplicated and distributed to different users performing table-top experiment.

Is this still valid??? $\Rightarrow$ Option to test different types of amplifiers (shaping, non-shaping....)

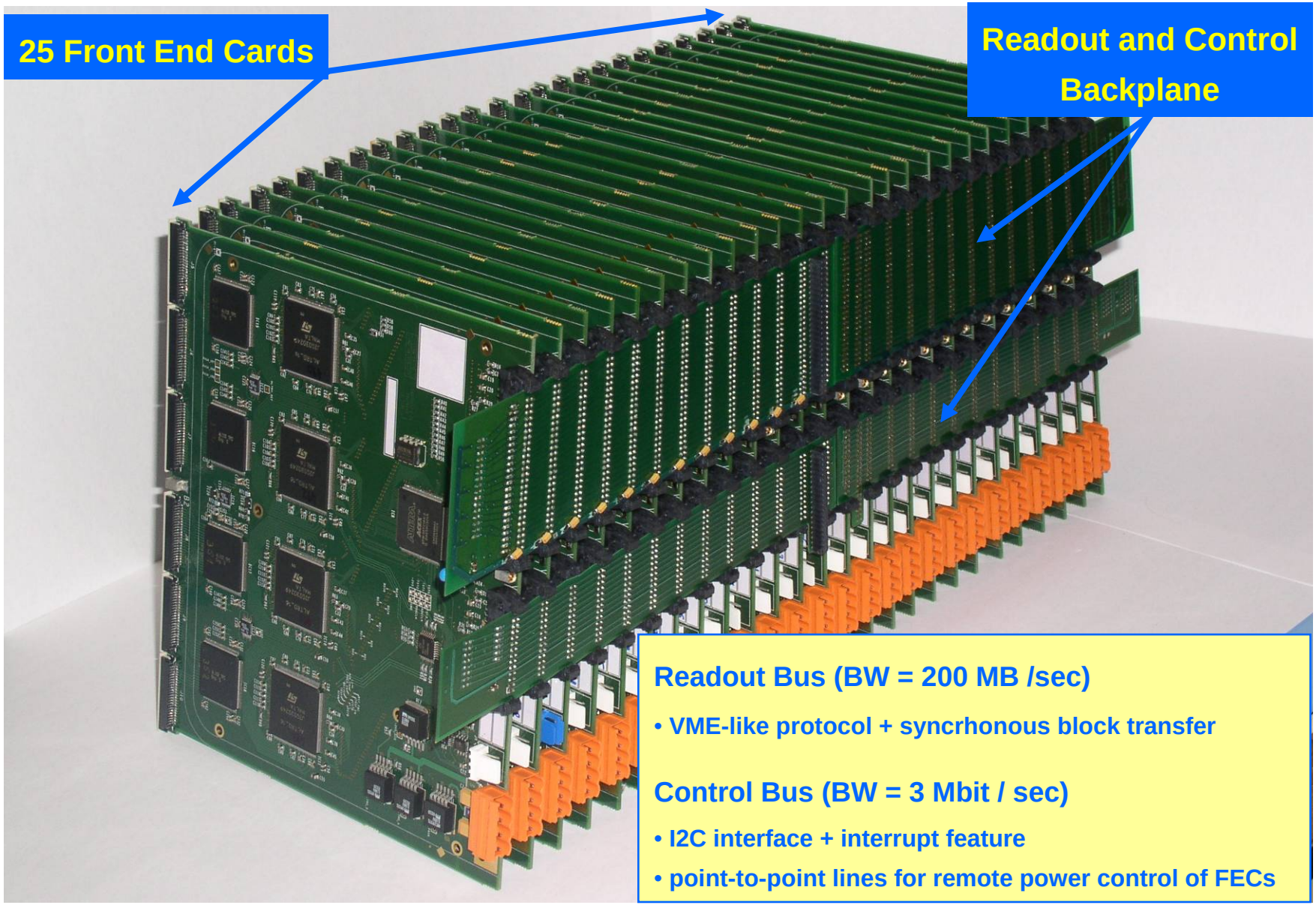
DAQ architechture



ALICE TPC Front End Card



Readout & Control Backplane



Readout Bus (BW = 200 MB /sec)

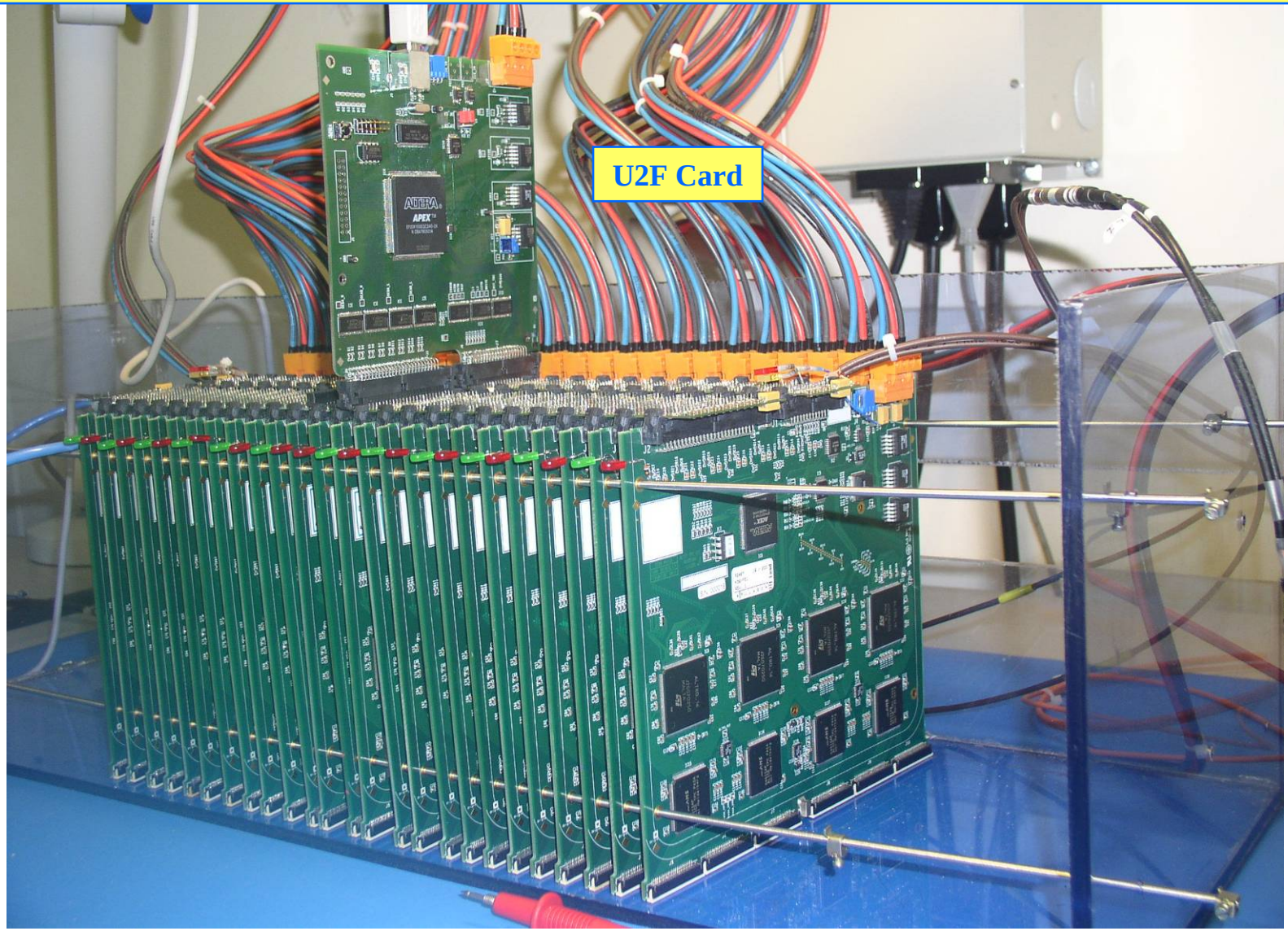
- VME-like protocol + syncrhonous block transfer

Control Bus (BW = 3 Mbit / sec)

- I2C interface + interrupt feature
- point-to-point lines for remote power control of FECs

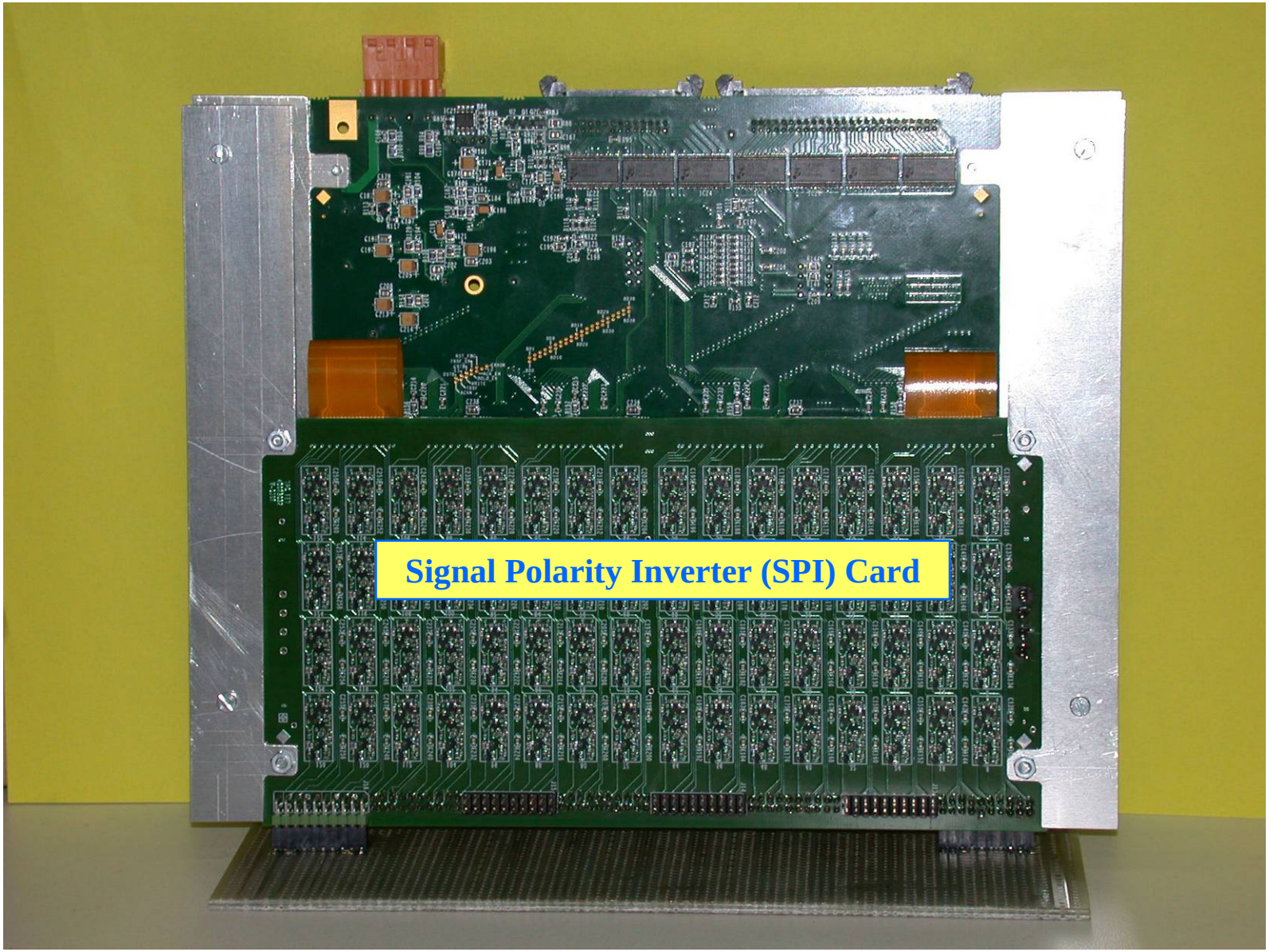
USB to FEC Interface Card (U2F)

The U2F Card can read up to 16 FECs (2048 channels)



SPI Card + ALICE TPC FEC

Temporary during the development phase of the new preamplifier



Readout electronics for the Large Prototype TPC (LPTPC)

- modular with well defined interface for
  - ✓ various amplifcation technologies (GEM & μMegas)
  - ✓ different module geometries
- easy to use and with a modern DAQ system
- Two strategies pursued in EUDET
  - new TDC (Rostock)
  - FADC-based (Lund, CERN)

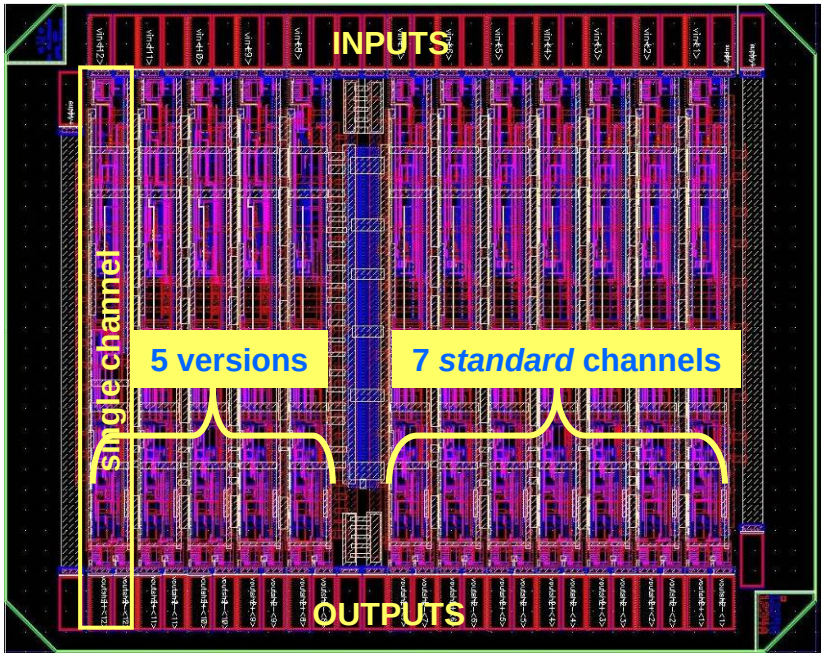
Status of the ALICE FEC

- 40-MHz ALTRO chip: about 125 chips have to be unsoldered from existing FECs (obsolete ALICE prototypes). This work is planned for Q1 2007.

- U2F and SPI cards: 2 additional boards of each type have been produced and tested

- New shaping amplifier chip: well advanced
  - number of channels: 32 or 64
  - programmable charge amplifier:
    sensitive to a charge in the range: ~10^2 - ~10^7 electrons
    input capacitance: 0.1pF to 10pF

Programmable Charge Amplifier

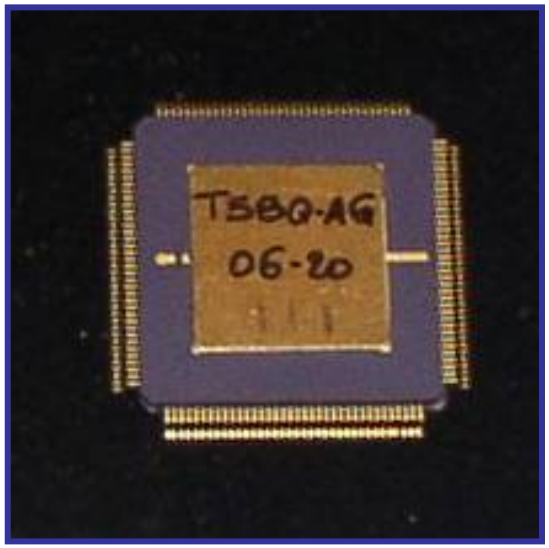


Production Engineering Data

- 12- channel 4th order CSA
- various architectures (classical folded cascode, novel rail-to-rail amplifier)
- process: IBM CMOS 0.13 μm
- area: 3 mm²
- 1.5 V single supply
- Package: CQFP 144
- MPR samples (40): Apr '06

Parameter	Requirement	Simulation	MPR Samples
Noise	< 500e	300e (10pF)	270e (10pF)
Conversion gain	10mV / fC	10mV / fC	9.5mV / fC
Peaking time (*standard*)	100ns	100ns	100ns
Non linearity	< 1%	< 0.35%	0.4%
Crosstalk	<0.3%	0.4%	< 0.3%
Dynamic range	> 2000	3300	4600
Power consumption	< 20mW	10mW / ch	10mW / ch (30pF cl)

Programmable Charge Amplifier



- **The CQFP 144 package has the same pin-count and similar pin-out as the ALICE TPC PASA**
- **In the near future the new chip will be tested on a ALICE TPC FEC**

Next Step

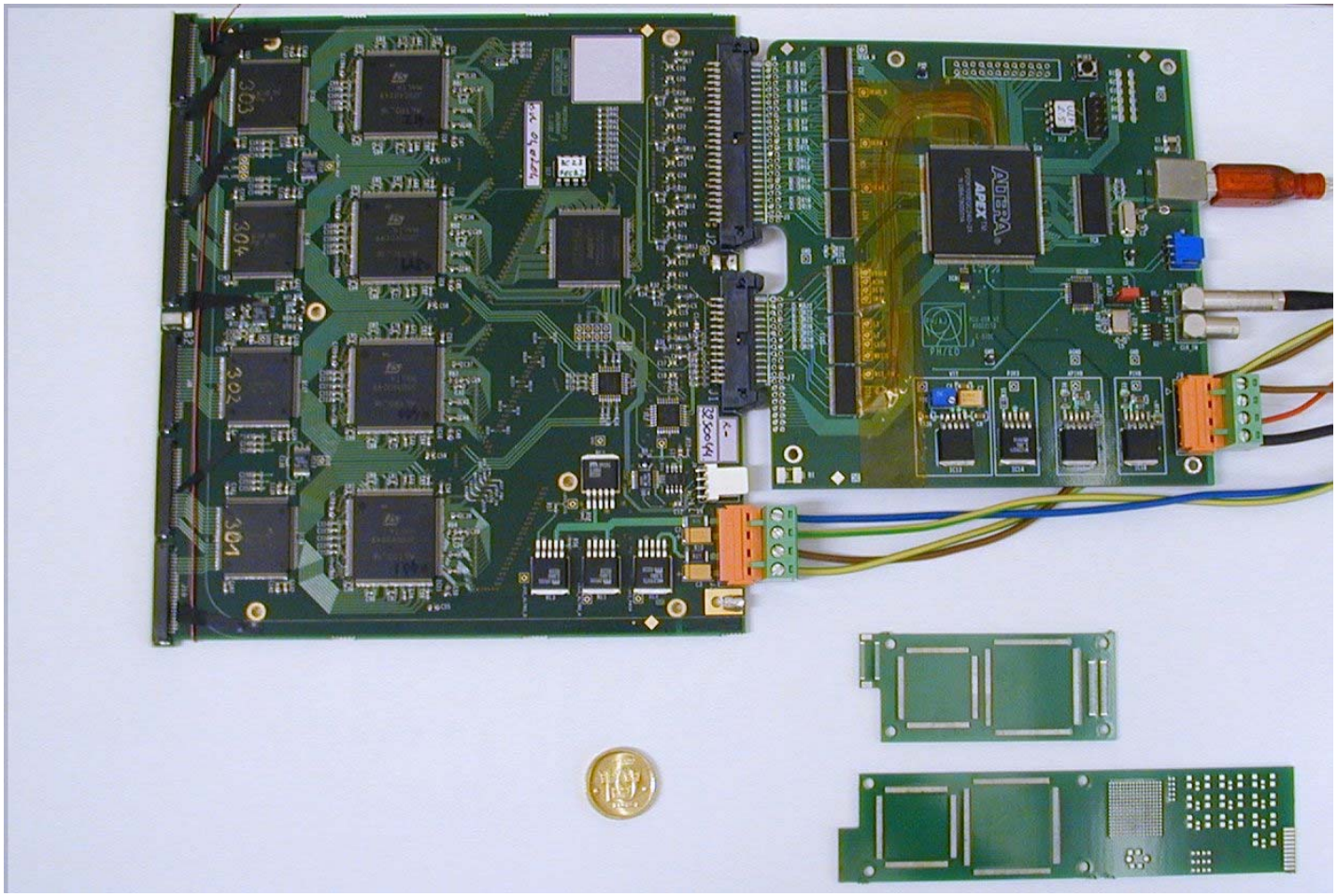
- Programmable Charge Amplifier (prototype)
  - 16 channel charge amplifier + anti-aliasing filter
  - Programmable peaking time (20ns – 140ns) and gain

System components and responsibilities

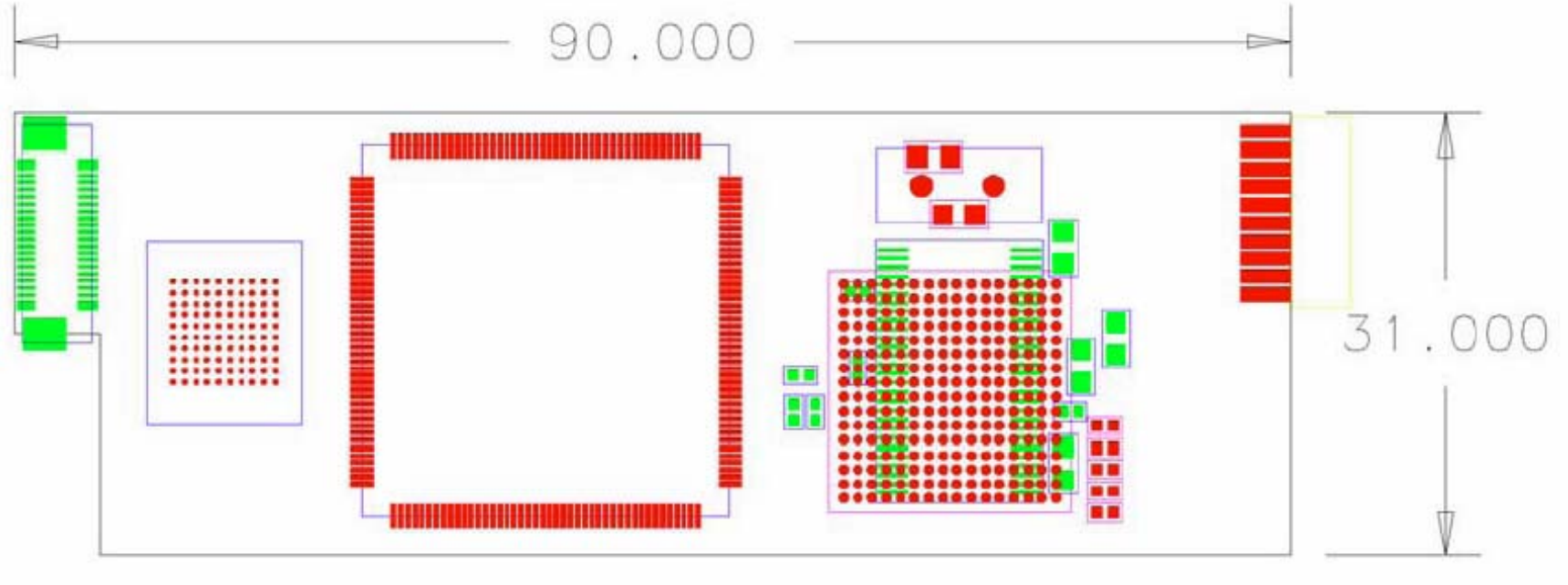
- ✓ interface between TPC readout plane and FEE (Lund)
- ✓ new shaping amplifer chip (CERN)
- ✓ 40-MHz ALTRO (CERN)
- ✓ Front End Card (PASA + ALTRO):
  - new design (Lund)
  - production and test (Lund)
- ✓ U2F card (CERN)
- ✓ System integration and test (Lund)
- ✓ DAQ (Lund)

The mini-FEC new design

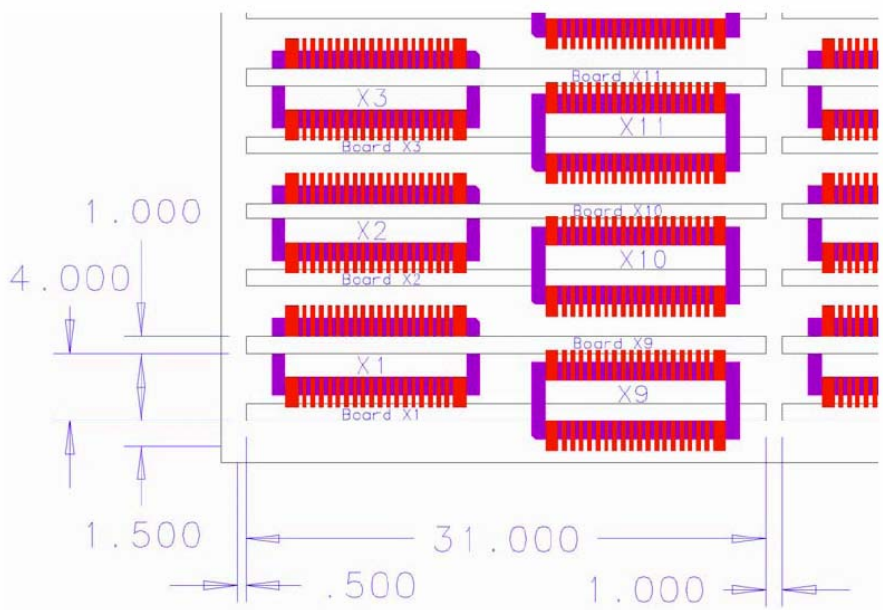
Motivation: should be compatible with the available area such that it can be mounted directly onto the connectors at the plane
$\Rightarrow$ the number of equipped pads can be increased without getting space problems.

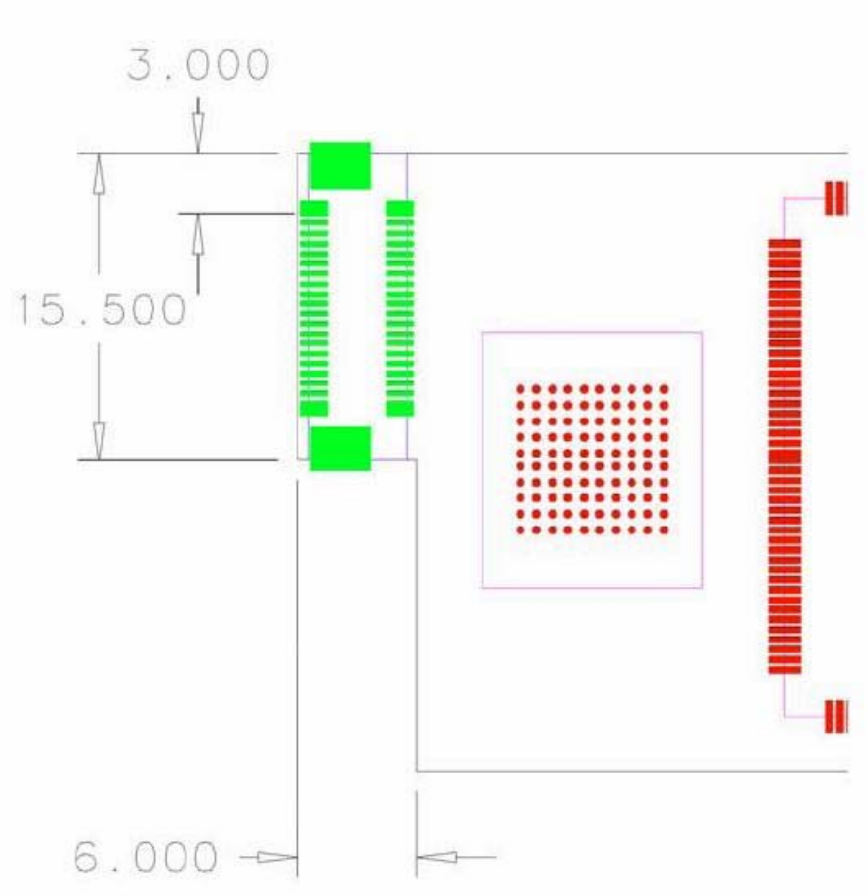


The mini-FEC new design
(based on the ALTRO chip)

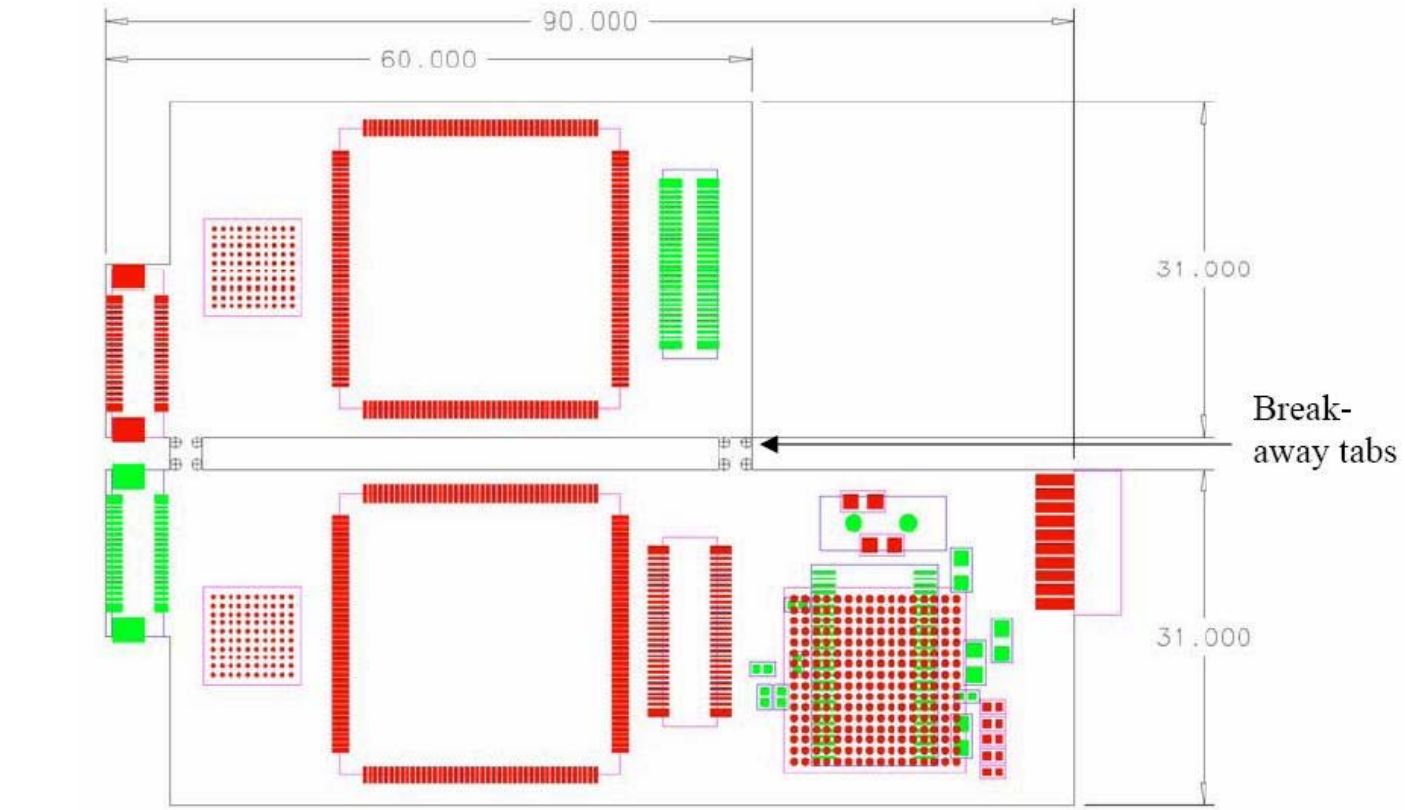


Connector arrangement



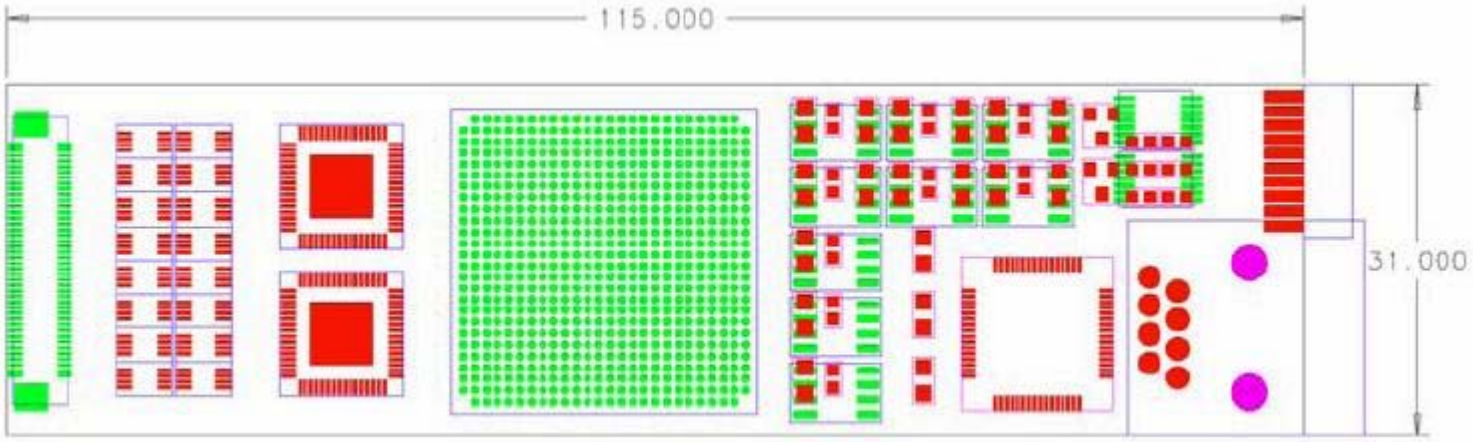


Dual mini-FEC
(based on the ALTRO chip)



Mini-FEC based on commercial components

- In telecommunication a completely new approach of handling signals has been developed (digitizing baseband + digital signal processing, DSP).
- Recent development in density and complexity of FPGA's (field programmable gate array) and lower prices.
- Completely reprogrammable DSP in contrary to ASIC.
- A new generation of multi-channel, high-speed and high resolution FADC's with low noise and serial digital output has been developed, offered to a reasonable cost.

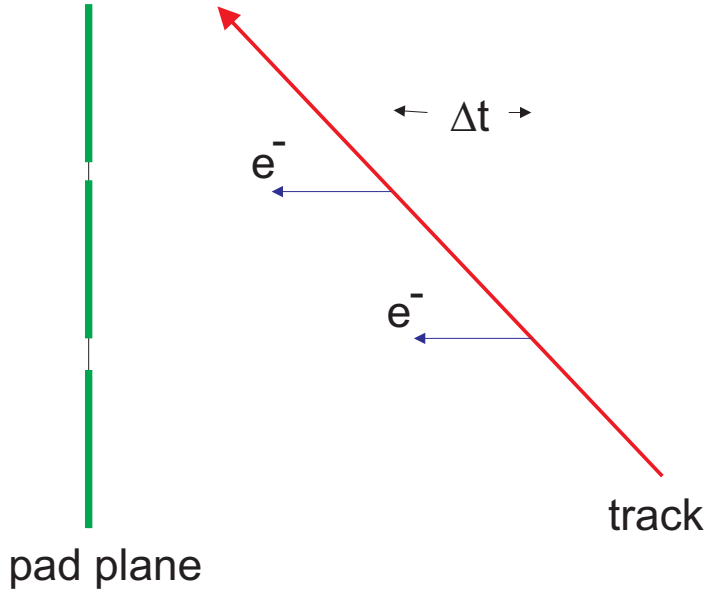


Pulse characteristics

- For tracks traversing the chamber parallel to the pad plane i.e perpendicular to the beam axis, the pulse length is determined by the longitudinal diffusion.

- For inclined tracks the pulse length is given by the difference in arrival time of the electrons emitted at the ends of the track segment covered by the length of a pad.

⇒ Pulses will be of different length



Options:

- Charge preamp, τ_{rise} ~40 ns, τ_{decay} ~2 μs and shaper integrator 200-500 ns 10 MHz sampling
- Charge preamp, τ_{rise} ~40 ns, τ_{decay} 2 ~μs, no shaping, 25 MHz sampling

Available: Charge preamp, τ_{rise} 20-140 ns, shaping, 40 MHz sampling

Dispute: The characteristics of the intrinsic GEM-pulse

Project Milestones

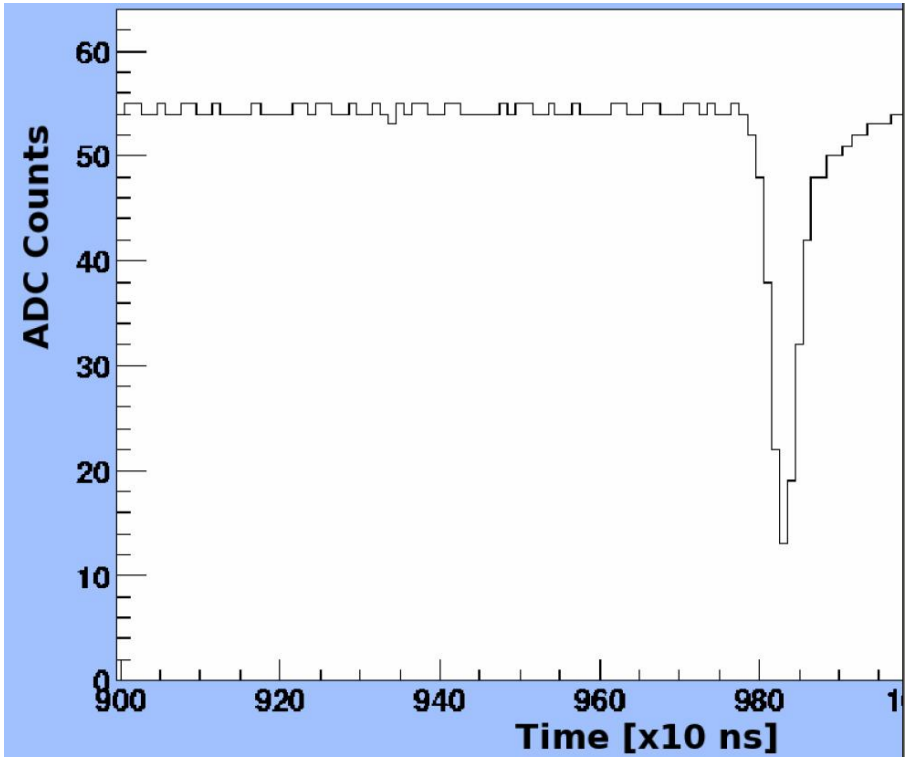
- Milestone I (Q1 2007)
  - Programmable Charge Amplifier (prototype); 16 channel charge amplifier + anti-aliasing filter
- Milestone II (Q2 2007)
  - 10-bit multi-rate ADC (prototype); 4-channel 10-bit 40-MHz ADC. The circuit can be operated as a 4-channel 40-MHz ADC or single-channel 160-MHz ADC.
  - Modified circuit board (design).
- Milestone III (Q3 2007)
  - Operating DAQ-system
  - Production and bench-top tests of modified FEC.
- Milestone IV (Q2 2008)
  - Charge Readout Chip (prototype); This circuit incorporates 32 (or 64) channels.
  -Mini FEC (design)
- Milestone V (Q4 2008)
  - Mini FEC (prototype) production and bench-top tests.
- Milestone VI (Q2 2009) ⇒ Charge Readout Chip (final version)
  - Production and final tests

Open questions

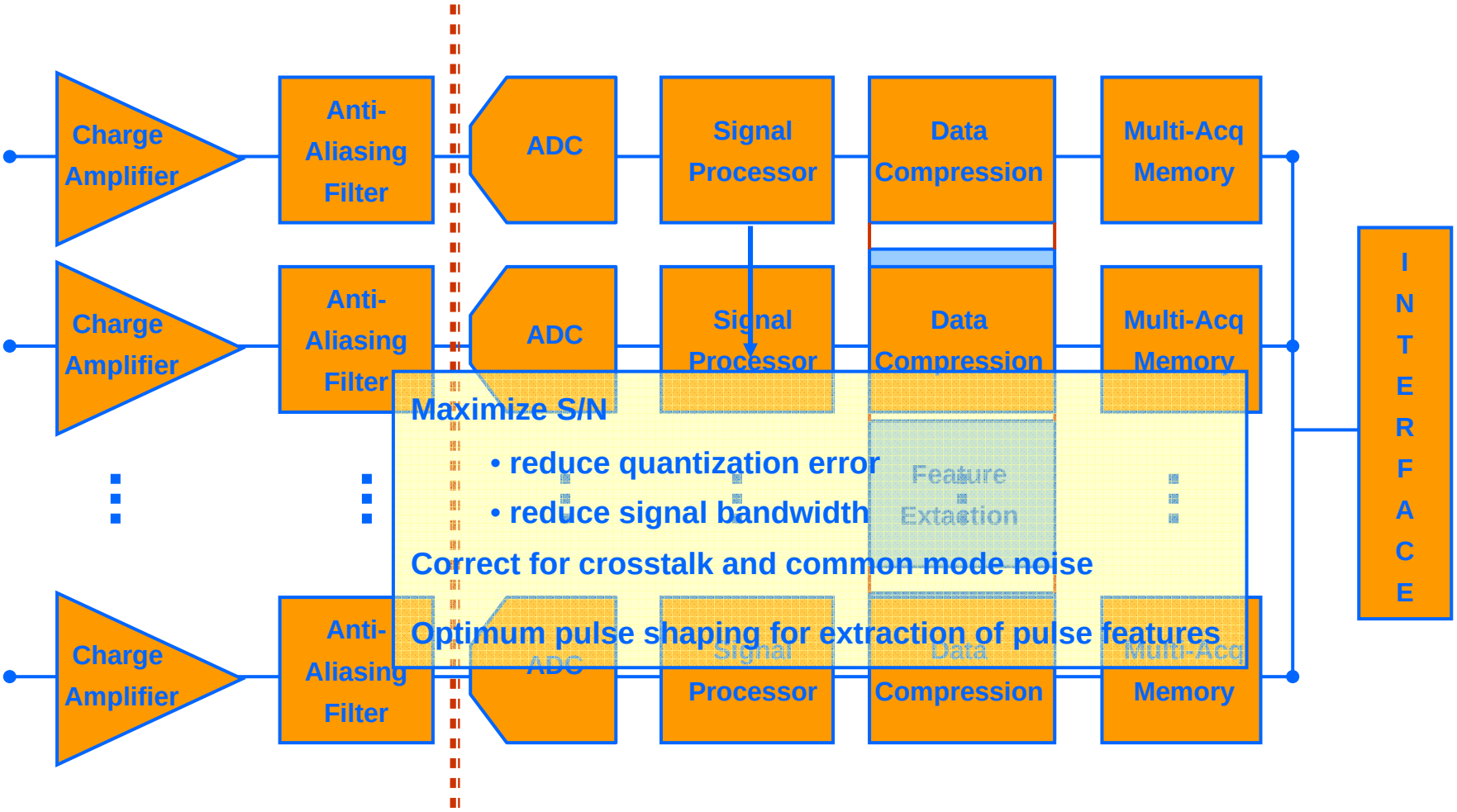
What is the rise time of a typical GEM pulse?
Mahdu Dixit claims around 100 ns or more
Aachen measures around 40 ns with a 3 gap GEM structure and Ar/CH_4 = 95/5 %

Shaping?
+ the pulse shape is well-known
⇒ low sampling frequency enough
- the integration time has to include the longest possible pulse
⇒ loss in two-track resolution for shorter pulses

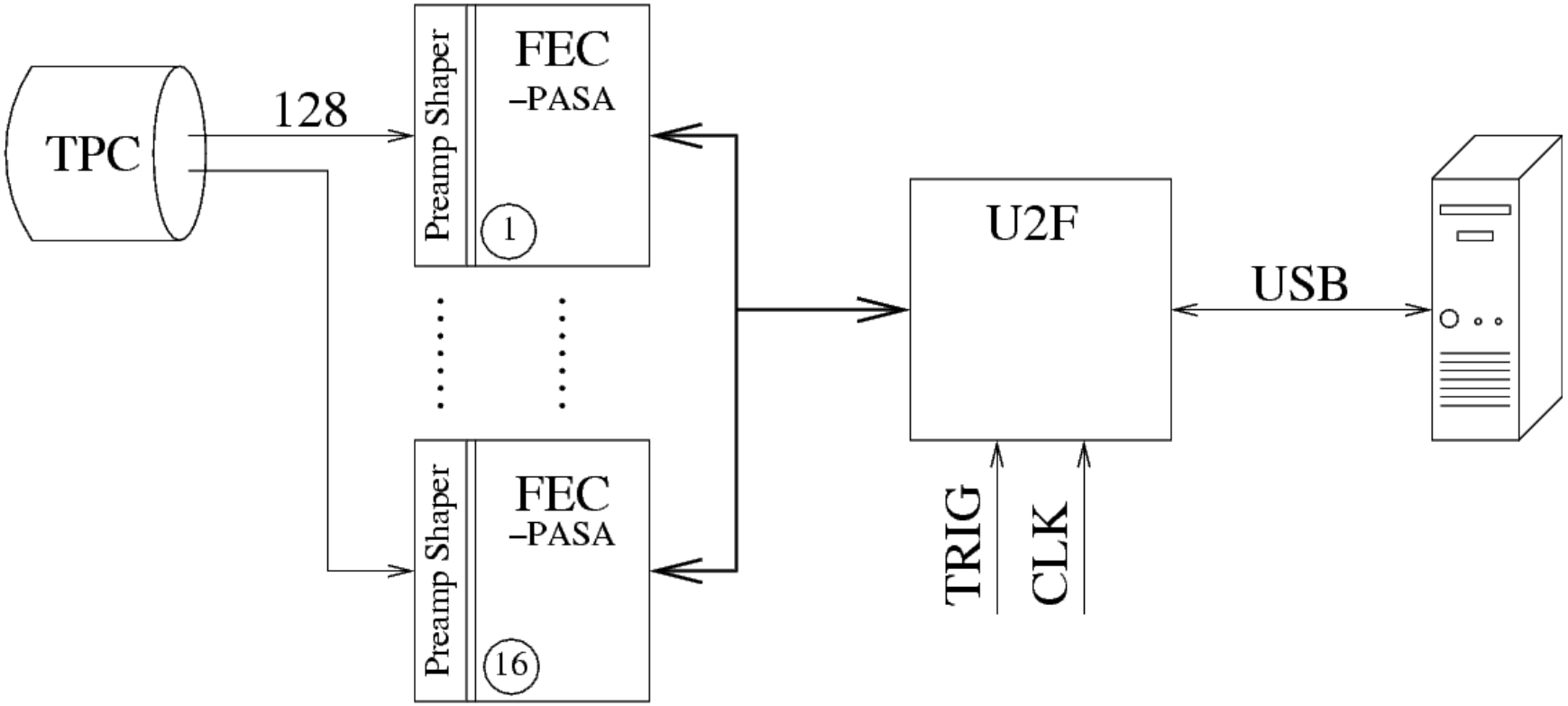
No shaping?
+ the sampling can be stopped at the end of the pulse
⇒ best possible two-track resolution
- the pulse shape is unknown or has to be assumed to be known
⇒ needs higher sampling frequency?



32 / 64 Channel



The layout


TPC
128
Preamp Shaper
FEC
–PASA
1
Preamp Shaper
FEC
–PASA
16
U2F
USB
TRIG
CLK