



Front-End electronics for Future Linear Collider calorimeters



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On behalf of the **CALICE** collaboration

<http://www.lal.in2p3.fr/technique/se/flc>

Slides from JC Brient, S. Blin, C. Jauffret, J. Fleury, G. Martin-Chassard, N. Seguin-Moreau, L. Raux, F. Sefkov

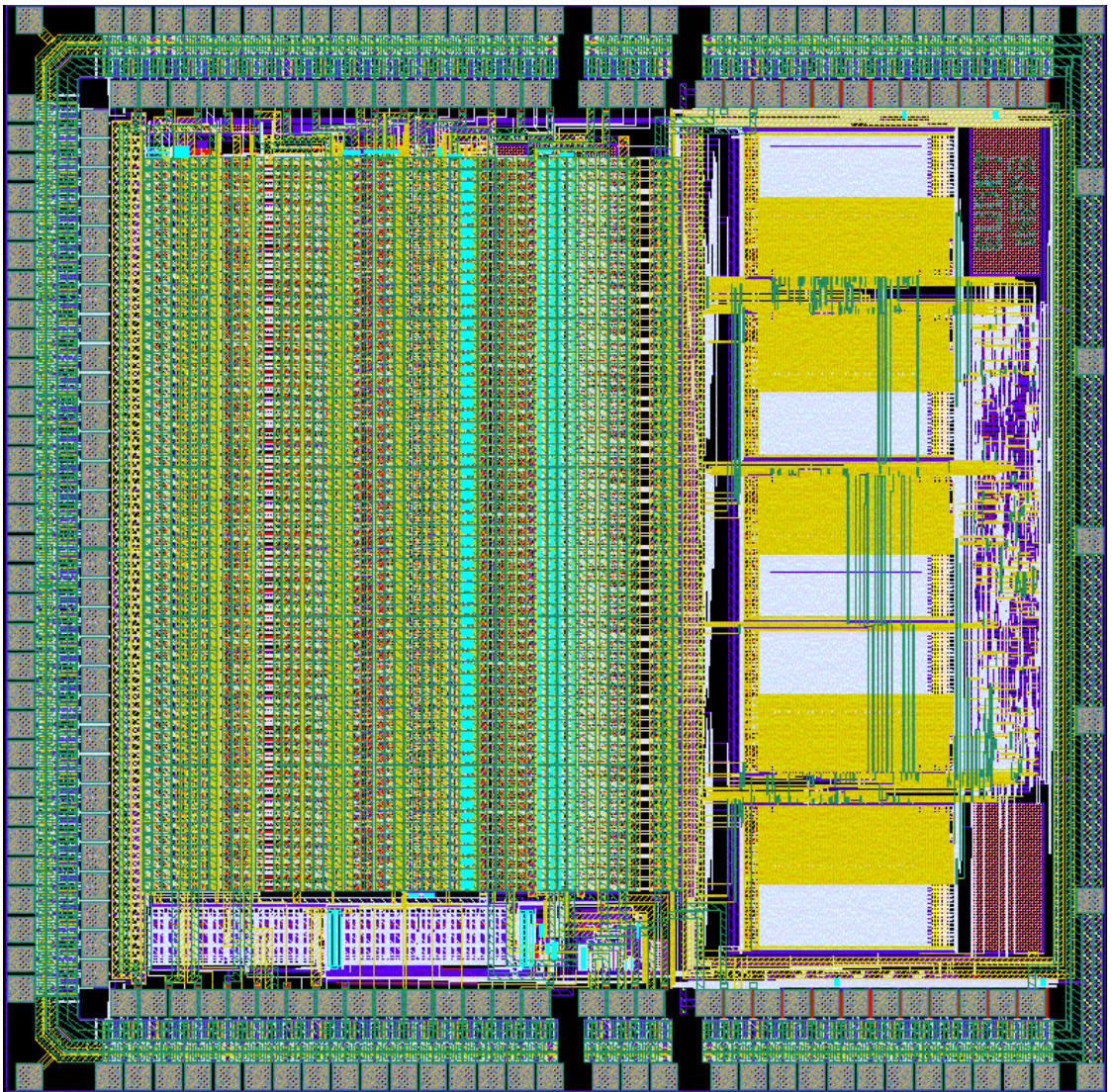
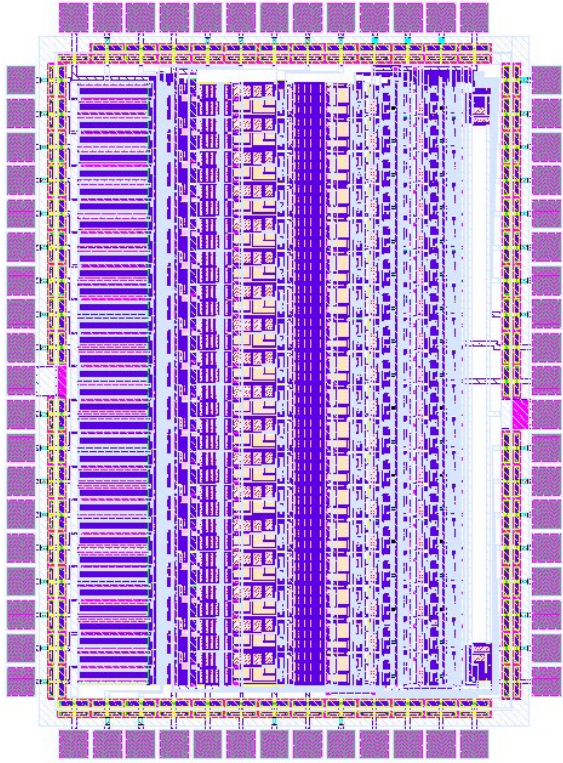
CALICE Testbeam at CERN SPS



Next steps

HaRD_ROC (2006)

FLC_PHY3 (2003)



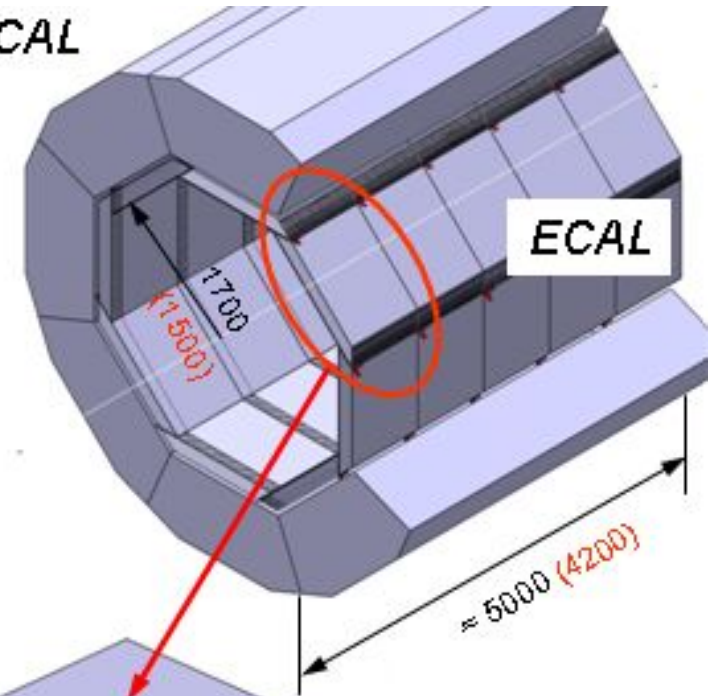


Technological prototype : "EUDET module"



- **Front-end ASICs embedded in detector**
 - Very high level of integration
 - Ultra-low power with **pulsed mode**
 - **FLC_TECH1 ASIC prototype in 0.35 μm SiGe**
- **All communications via edge**
 - 4,000 ch/slab, minimal room, access, power
 - small data volume (\sim few 100 kbyte/s/slab)
- **« Stitchable motherboards »**

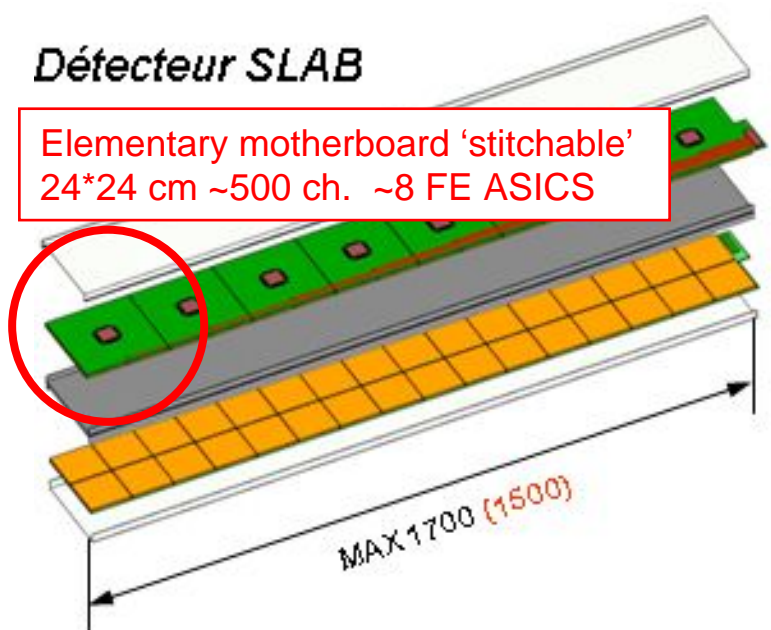
HCAL



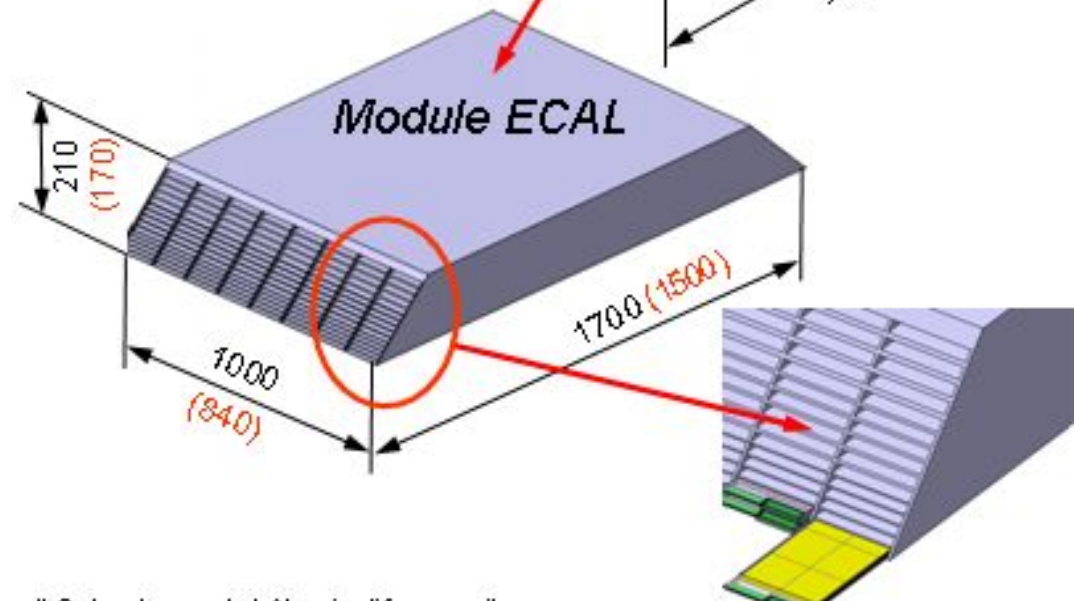
ECAL

Détecteur SLAB

Elementary motherboard 'stitchable'
24*24 cm ~500 ch. ~8 FE ASICS



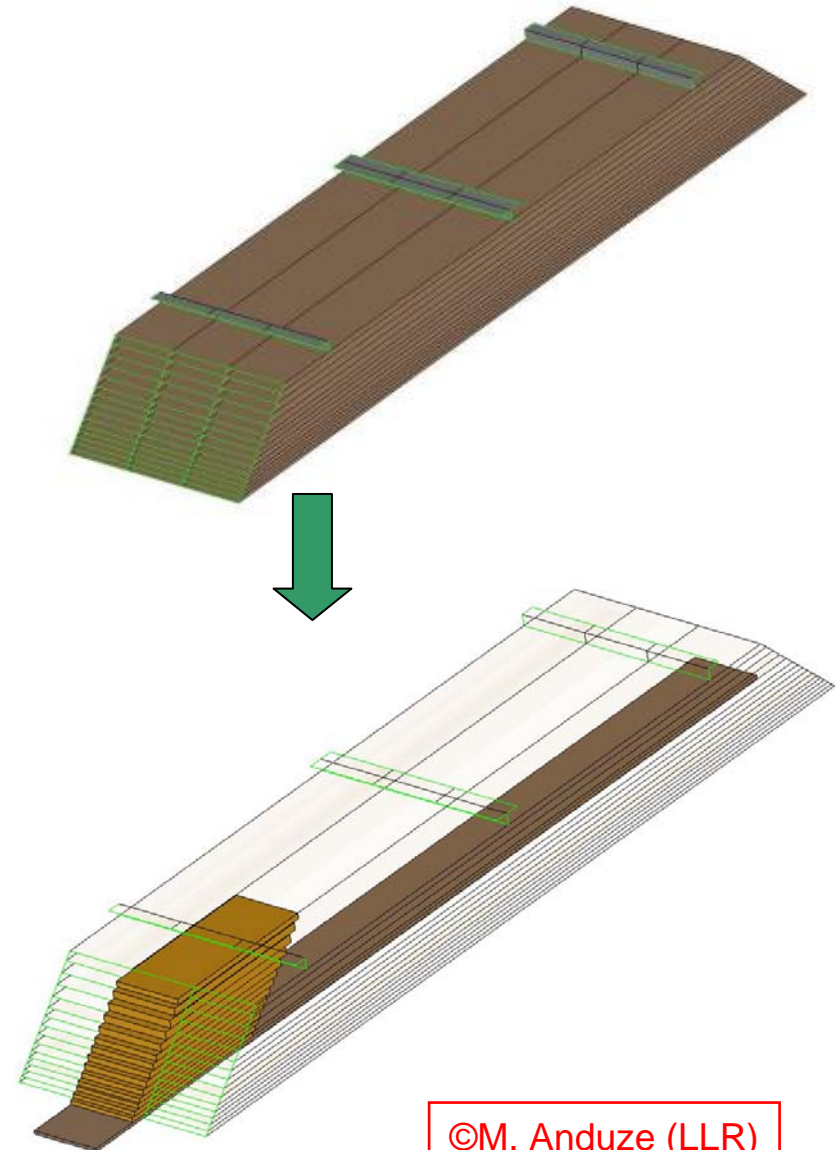
Module ECAL





EUDET : ECAL emodule

- **Electromagnetic calorimeter**
 - Prototype of a ($\sim 1/6$) module 0 : **one line & one column**
 - 150 cm long, 12 cm wide 30 layers
 - 1800 + 10800 channels
 - Test full scale mechanics + PCB
 - Can go in test beam
 - Test full integration + edge communications
- **Similar in #channels as physics prototype**

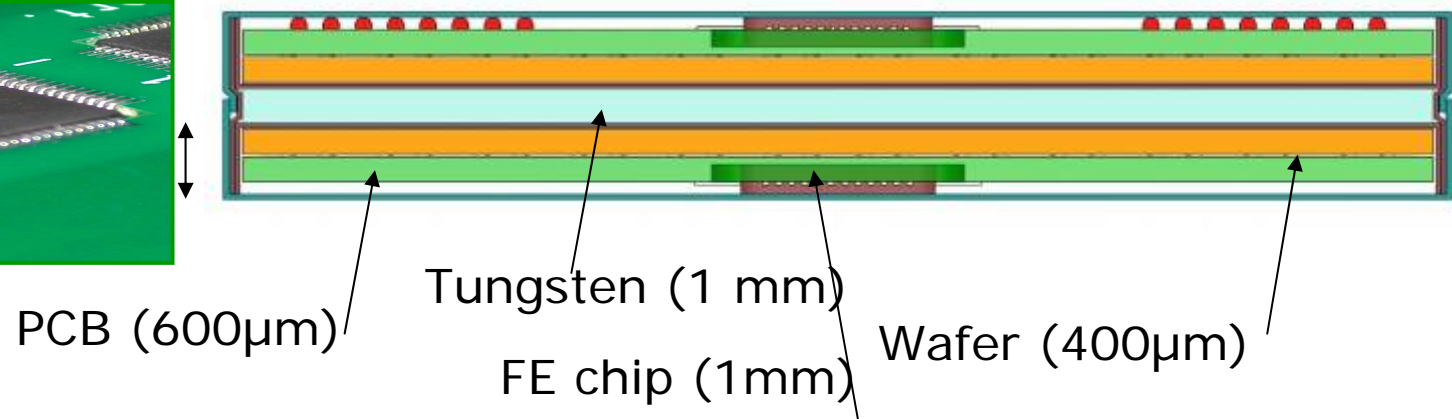
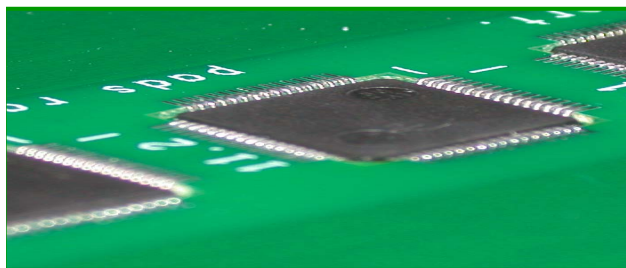


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EUDET module FEE : main issues

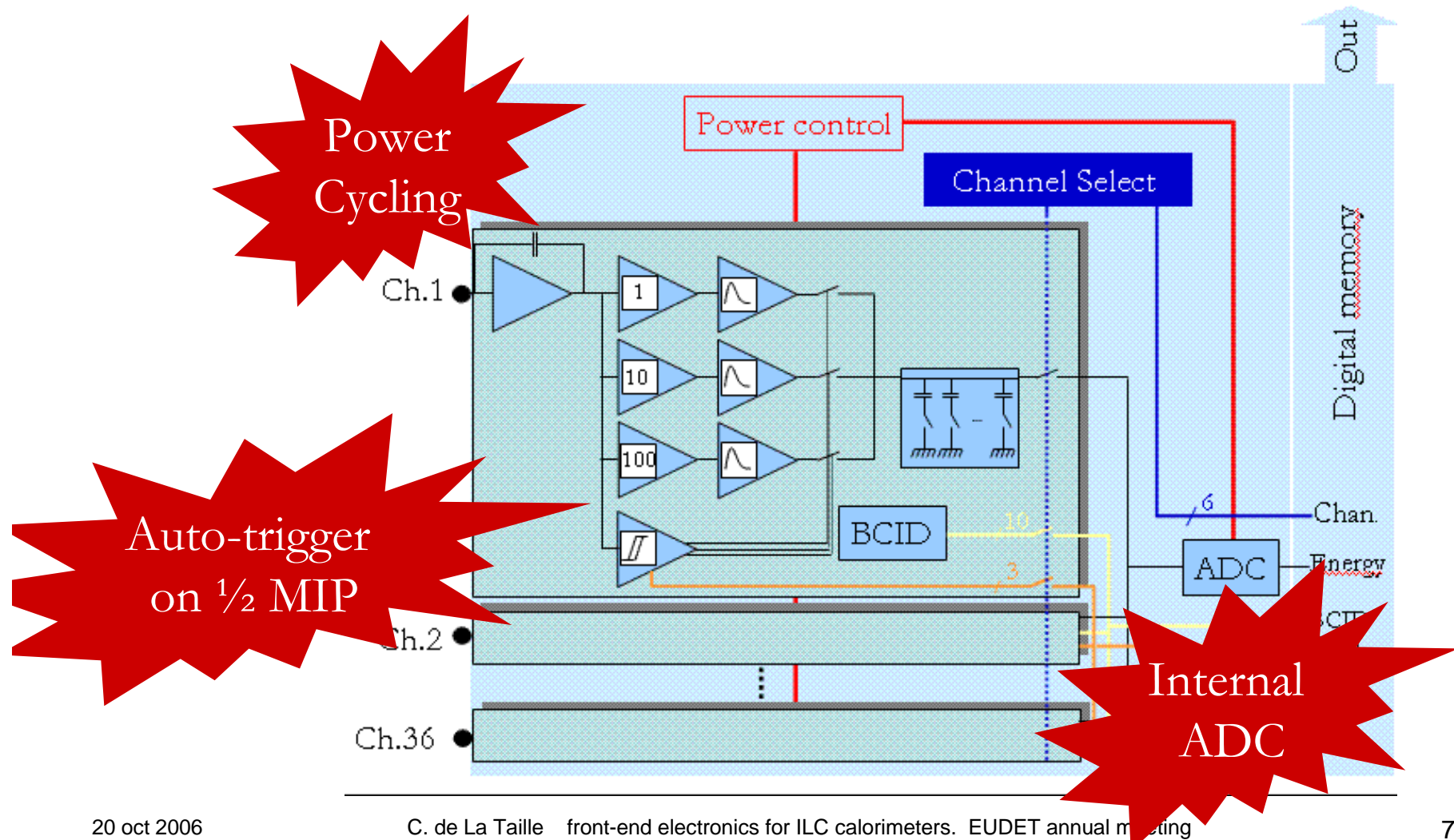
- **Mixed signal issues**
 - Digital activity with sensitive analog front-end
- **Pulsed power issues**
 - Electronics stability
 - Thermal effects
 - To be tested in beam a.s.a.p.
- **No external components**
 - Reduce PCB thickness to $< 800\mu\text{m}$
 - Internal supplies decoupling





ECAL Front-End ASIC

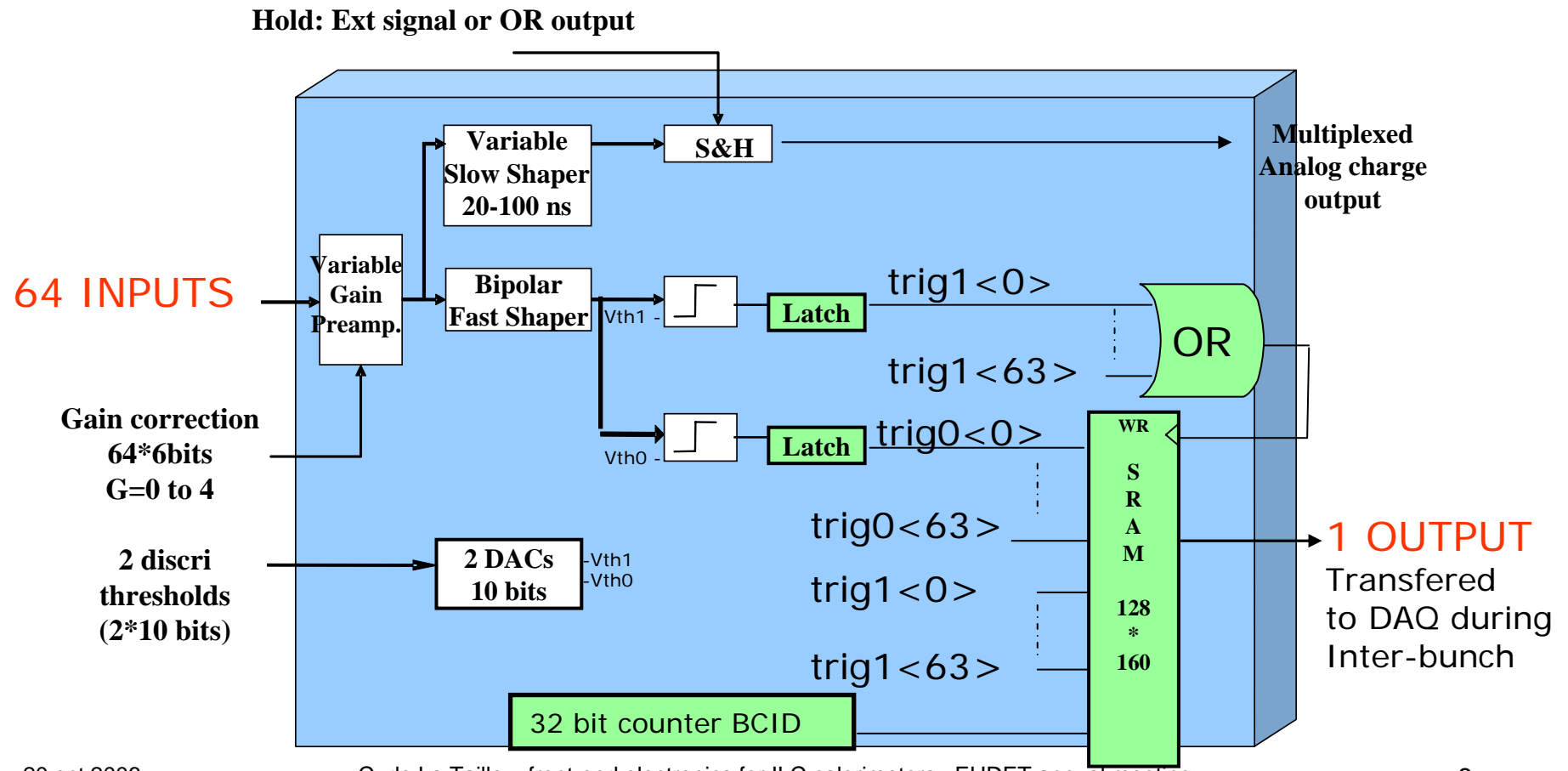
- Readout integration is the key element of compact detector
 - Keep small Moliere radius for good shower separation
 - Many features have never been used before e.g. power cycling (ON 2ms OFF 200 ms)





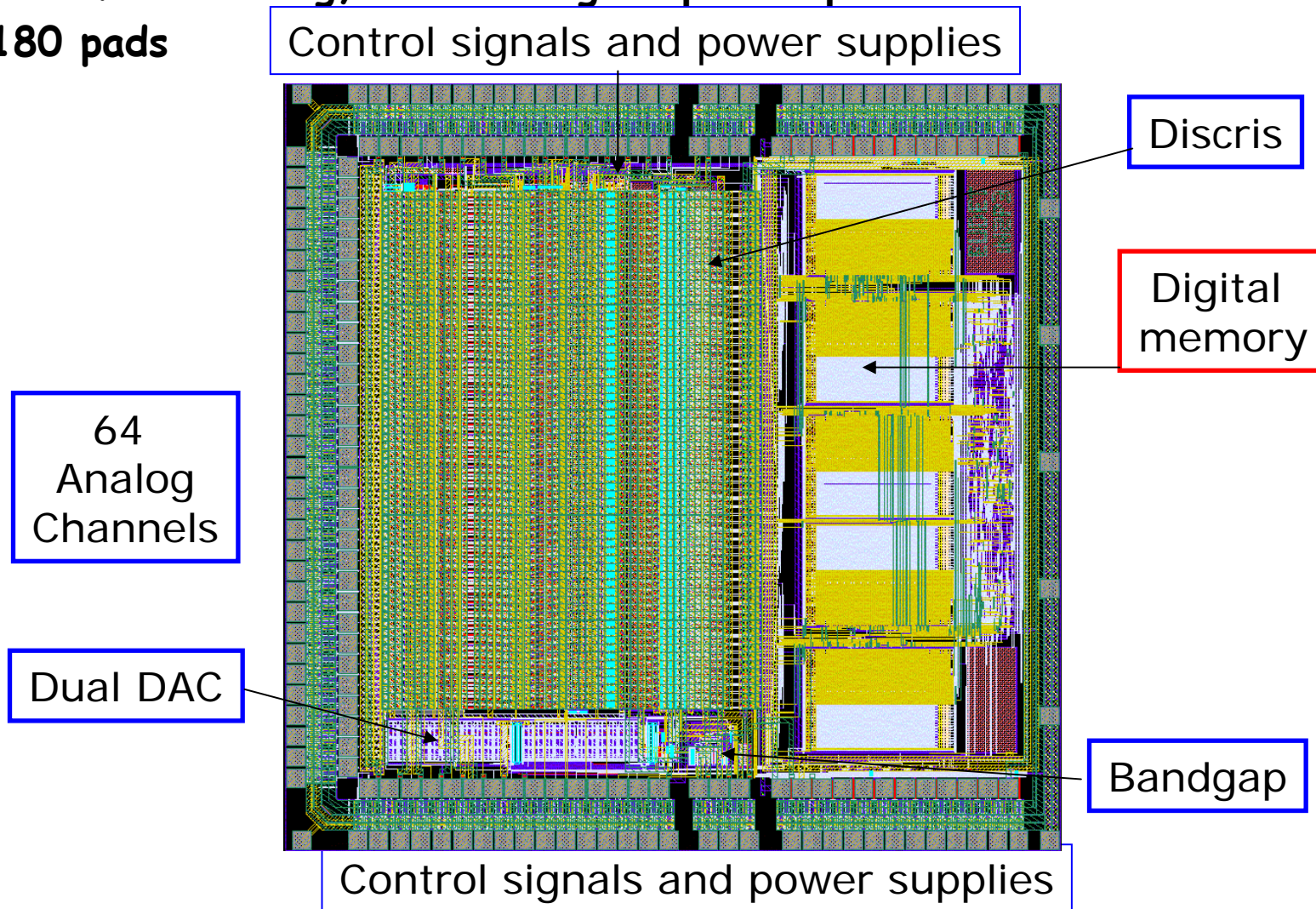
HaRDROC architecture

- Full power pulsing
- Digital memory: Data saved during bunch train. **Only one serial output**
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : $128(\text{depth}) * [2\text{bit} * 64\text{ch} + 32\text{bit}(\text{bcid}) + 8\text{bit}(\text{Header})] = 20\text{kbits}$
- Sequential readout @ 100 MHz : $20\text{k} * 10 \text{ ns} = 200 \mu\text{s}$ (read up to 1000 chips/inter bunch)

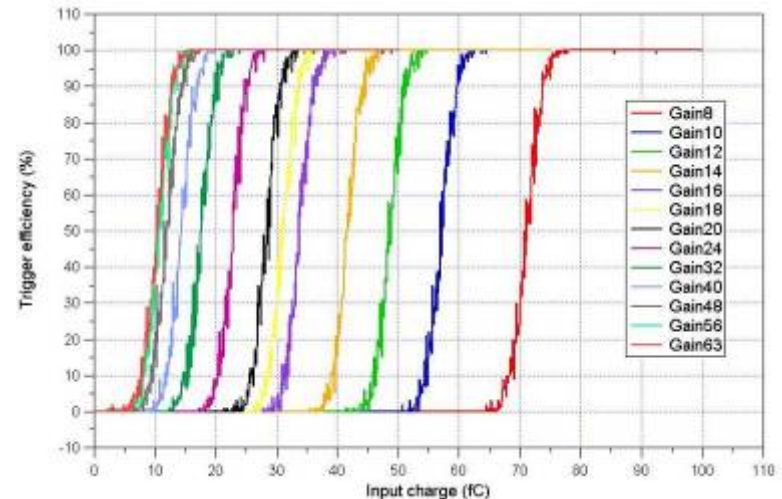
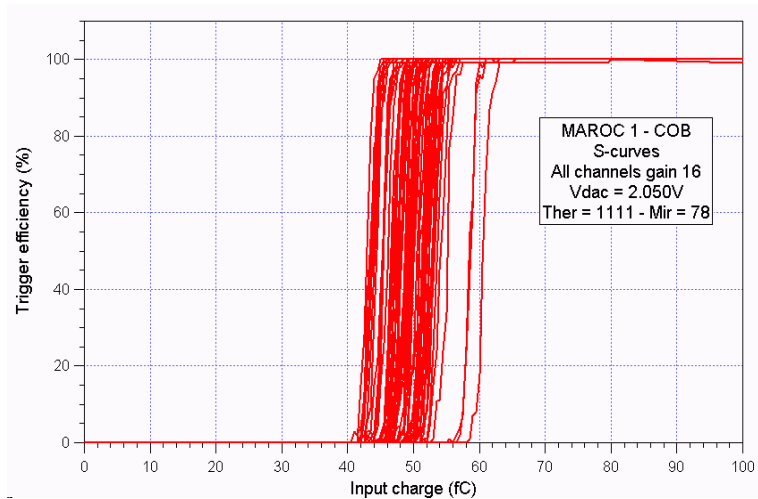


HaRDROC layout

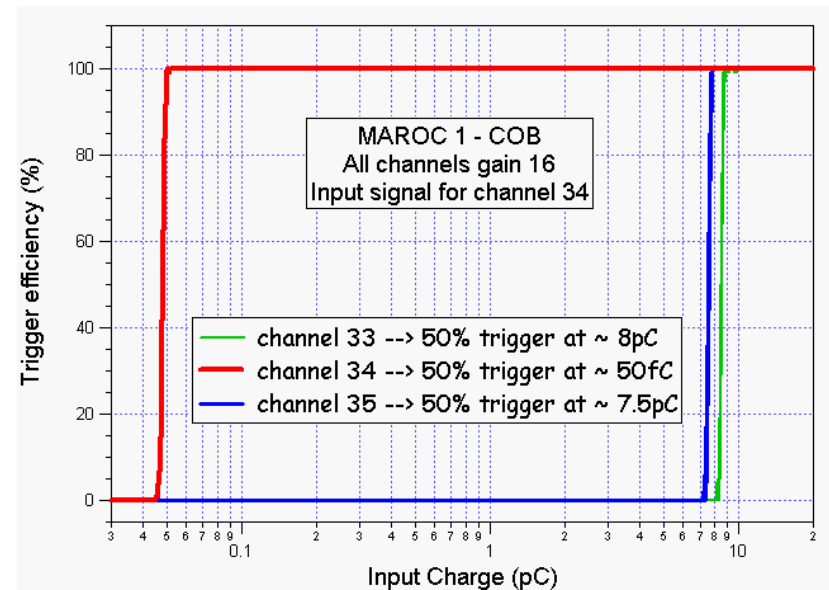
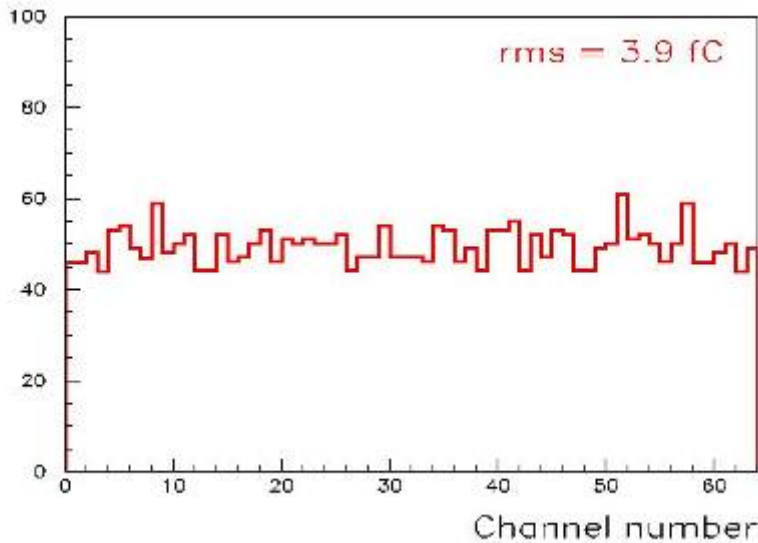
- 64 inputs, 1 data output
- Vss of the analog, mix and digital part separated
- 180 pads



MAROC Efficiency curves

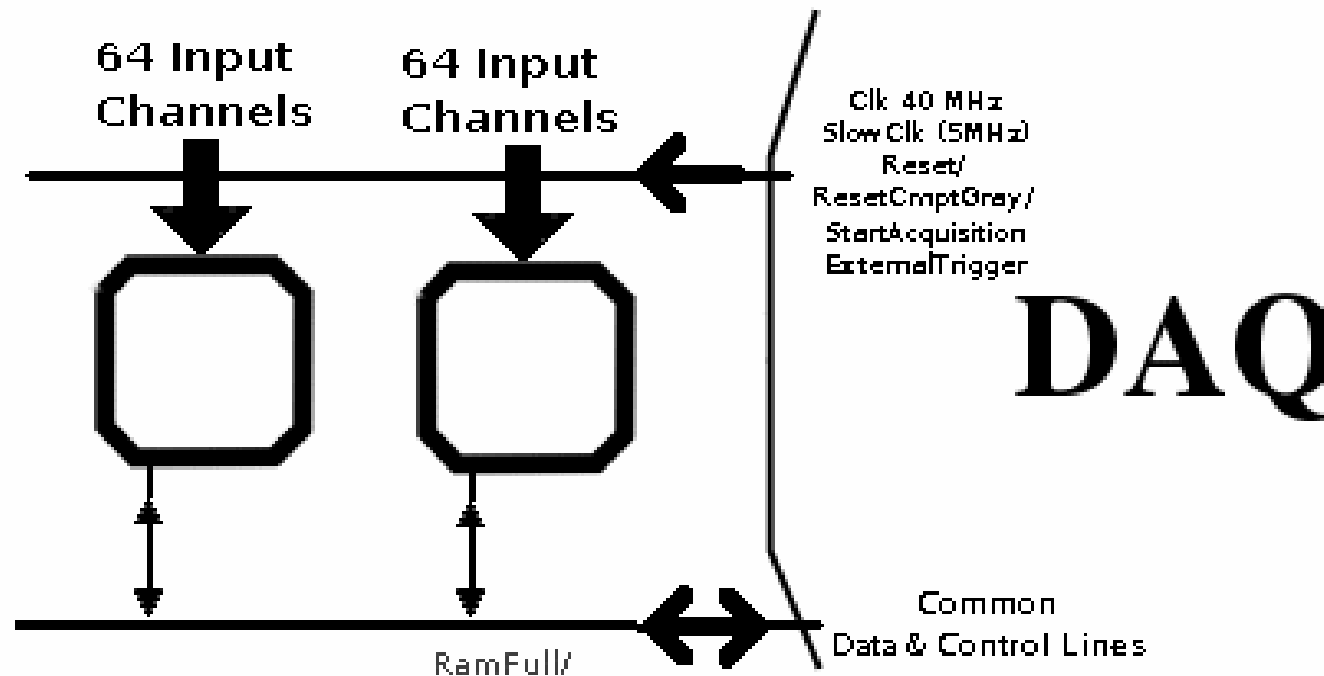


trigger @ 50



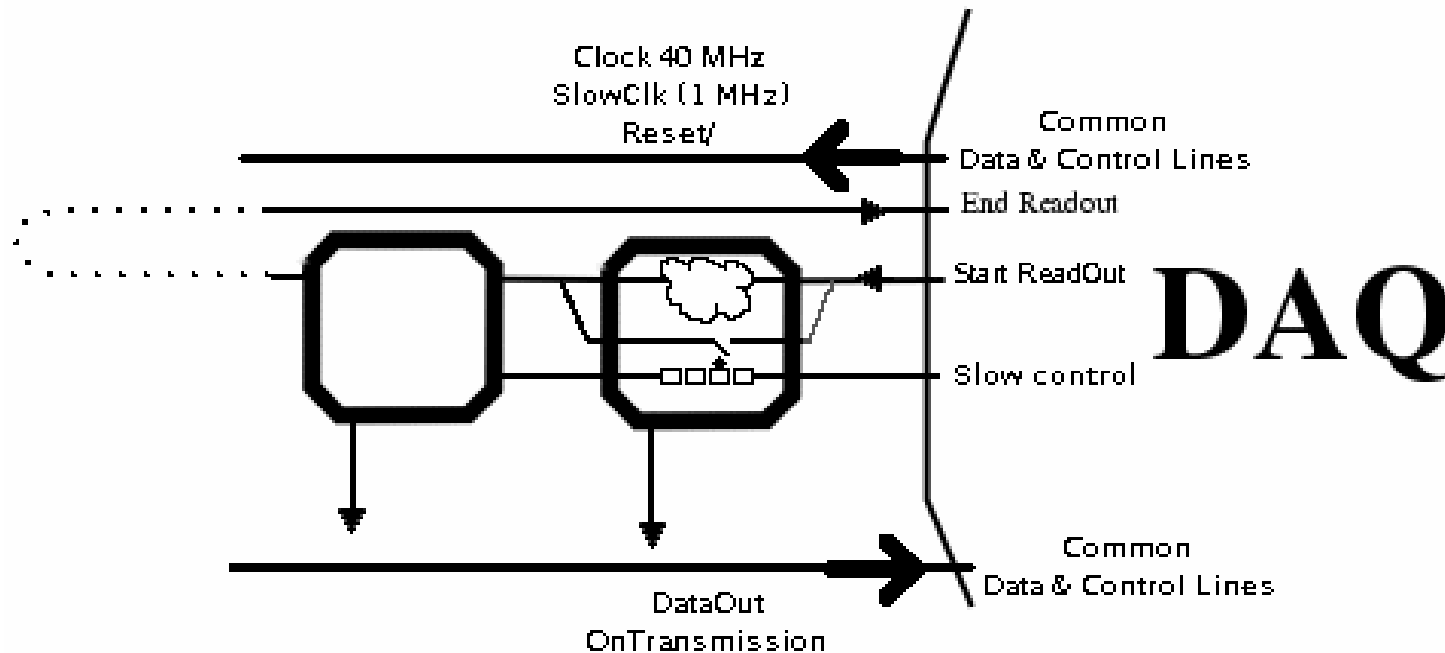
Acquisition mode

- Store upto 128 events in RAM
- Stop acquisition when ram_full signal asserted
 - Common collector bus for ram_full signal



Readout mode

- **Token ring mechanism initiated by DAQ**
 - Possibility to bypass a chip by slow control
- **One data line activated by each chip sequentially**
 - Readout rate few MHz to minimize power dissipation
 - With 500 pF bus capacitance, power dissipation is $\sim 10\mu\text{W}/\text{chip}$
 - $i=CdV/dt = 1\text{ mA} \Rightarrow 1\text{ mW}$ for up to 100 chips on bus
 - Readout time max (ram full) $10\text{ kbit} * 1\ \mu\text{s} = 10\text{ ms}/\text{chip}$





EUDET ECAL ASIC



- **72 channels**
 - Scales with the 4 factor reduction in pad size and is compatible with physics prototype

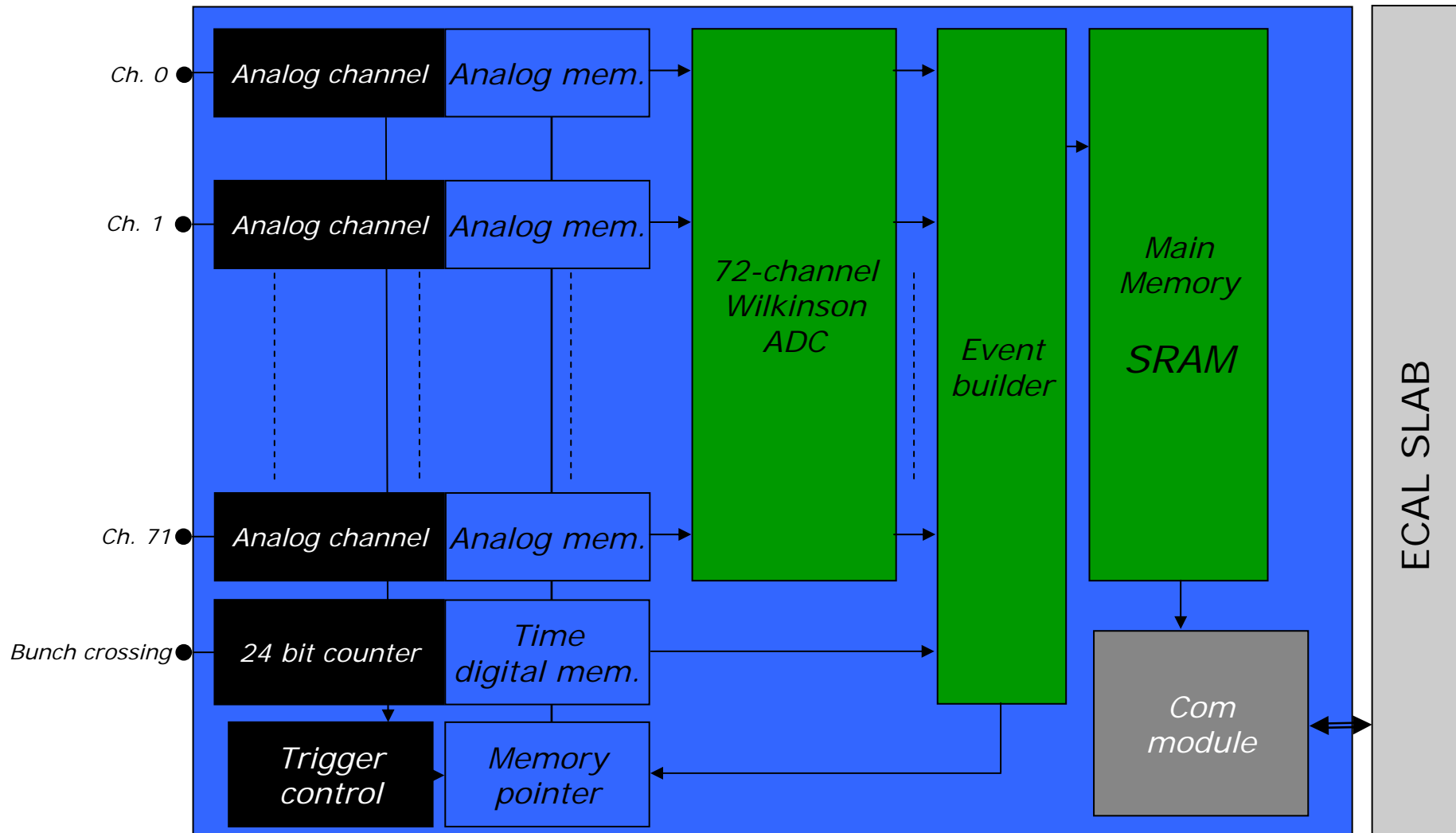
- **Detector DC coupling**
 - Prepares the case the on-detector MMIC HV capacitance is not affordable
 - Provides leakage current monitoring, up to 1 $\mu\text{A}/\text{Ch}$

- **Auto-trigger**
 - If one channel is hit during a bunch crossing, then the whole chip is recorded with a time tag (BCID)
 - The auto trigger activates the T&H

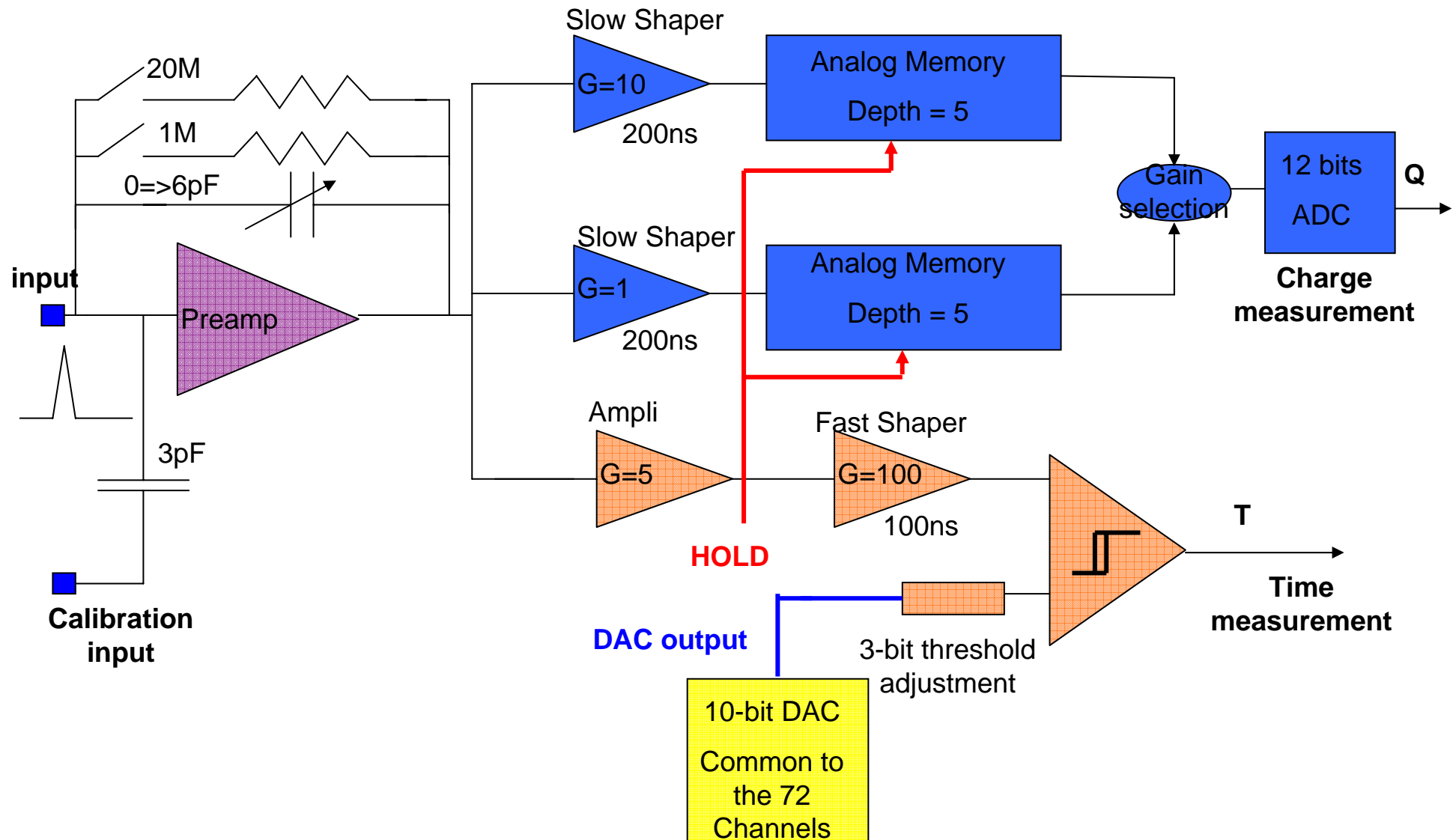
- **Analogue pipeline, ADC & digital registers**
 - 8-depth analog pipeline to store « in bunch » events
 - Wilkinson 12 bit 100MHz ADC
 - On chip storage, inter-bunch data outputting

- **Digital data output**
 - Daisy chained with redundancy : one output for 40 ASICs
 - Common architecture for ECAL and HCAL

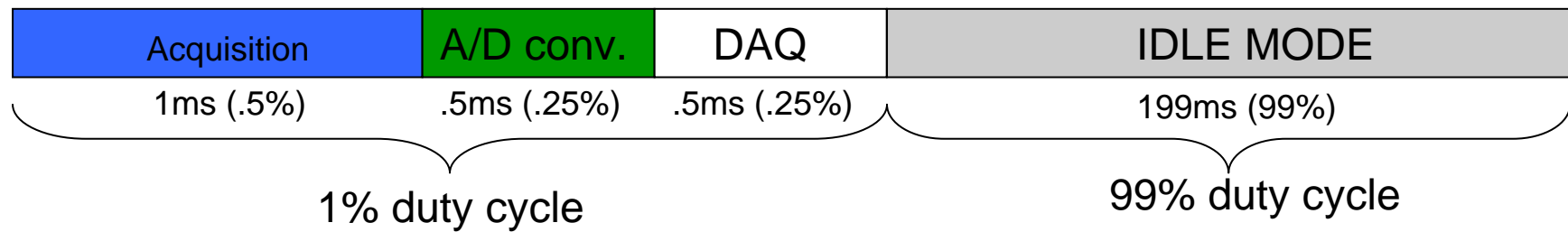
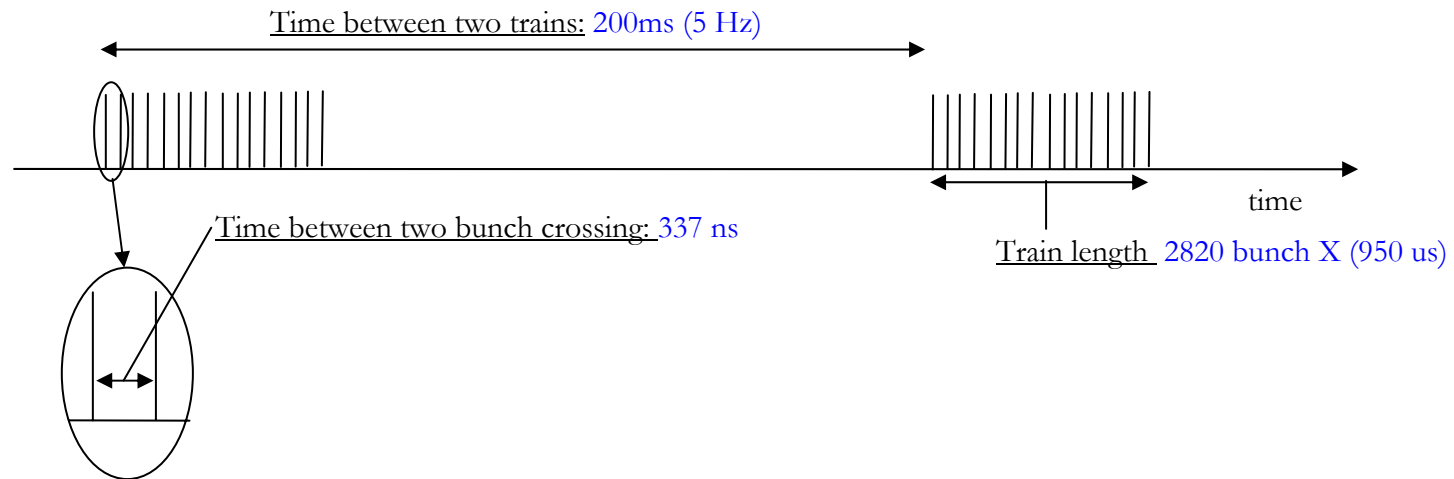
General block scheme

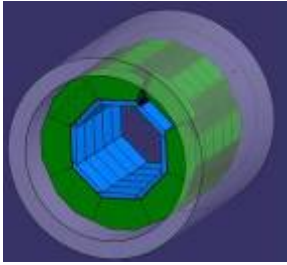


One channel

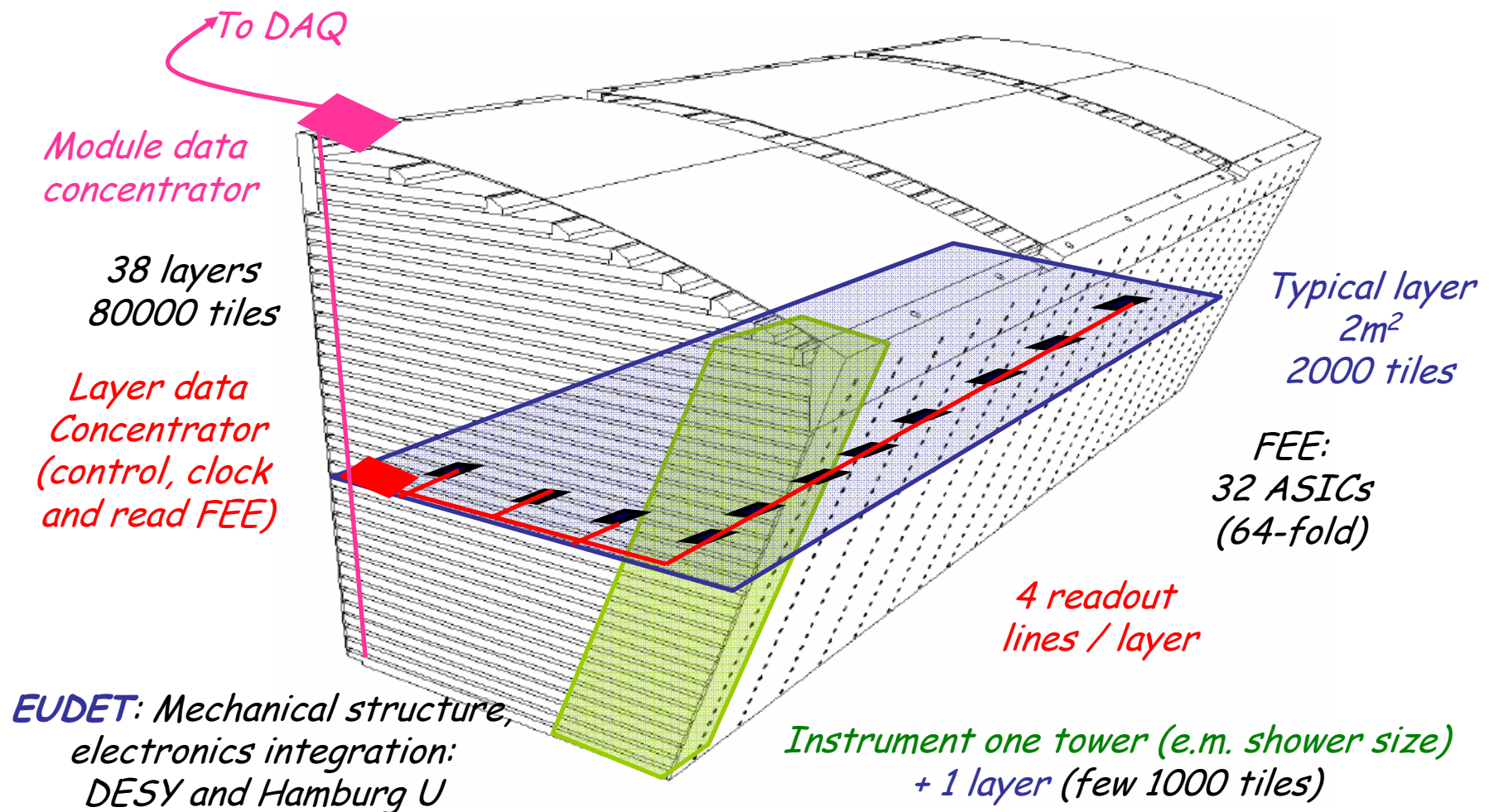


Time considerations





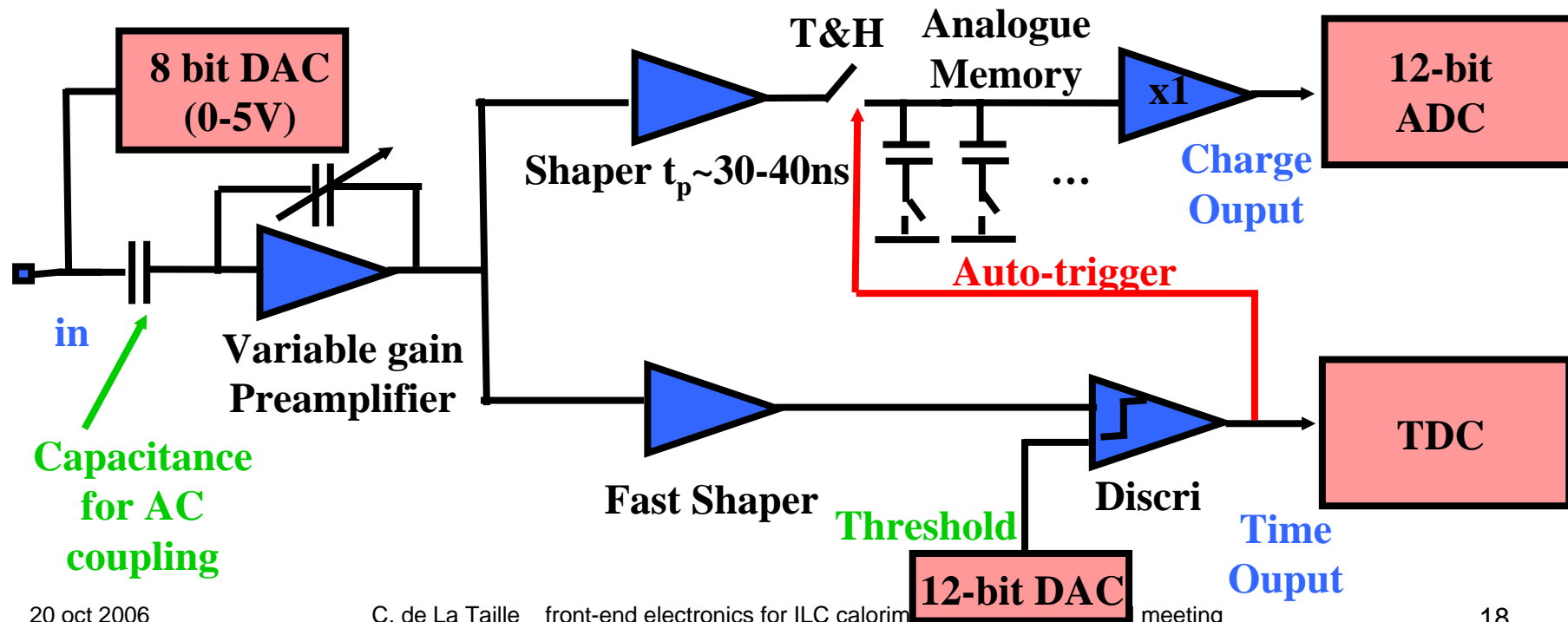
HCAL architecture



Prospective for A-HCAL SiPM Chip

■ Similar developments for AHCAL

- Chip fully dedicated to SiPMs developed after ECAL chip
- Internal DAC for SiPM gain adjustment (5V range)
- Auto-trigger (fast shaper + Discriminator)
- Internal TDC, 1 ns step
- Internal 12 bit ADC
- Power pulsing





Conclusion

- **Second generation calorimeter ASICS being designed**
 - Power pulsing, Zero-suppress, Auto-trigger...
 - HARPROC for DHCAL Readout submitted sept 06
 - First EUDET milestone passed
 - ECAL chip to be submitted in nov 06
 - AHCAL SiPM ASIC to be submitted in mar 07

- **System aspects to progress in parallel**
 - "Stitchable" PCBs for large module
 - Second generation DAQ
 - **Low power low cost essential target**

