

Study of Readout Electronics for LumiCal detector

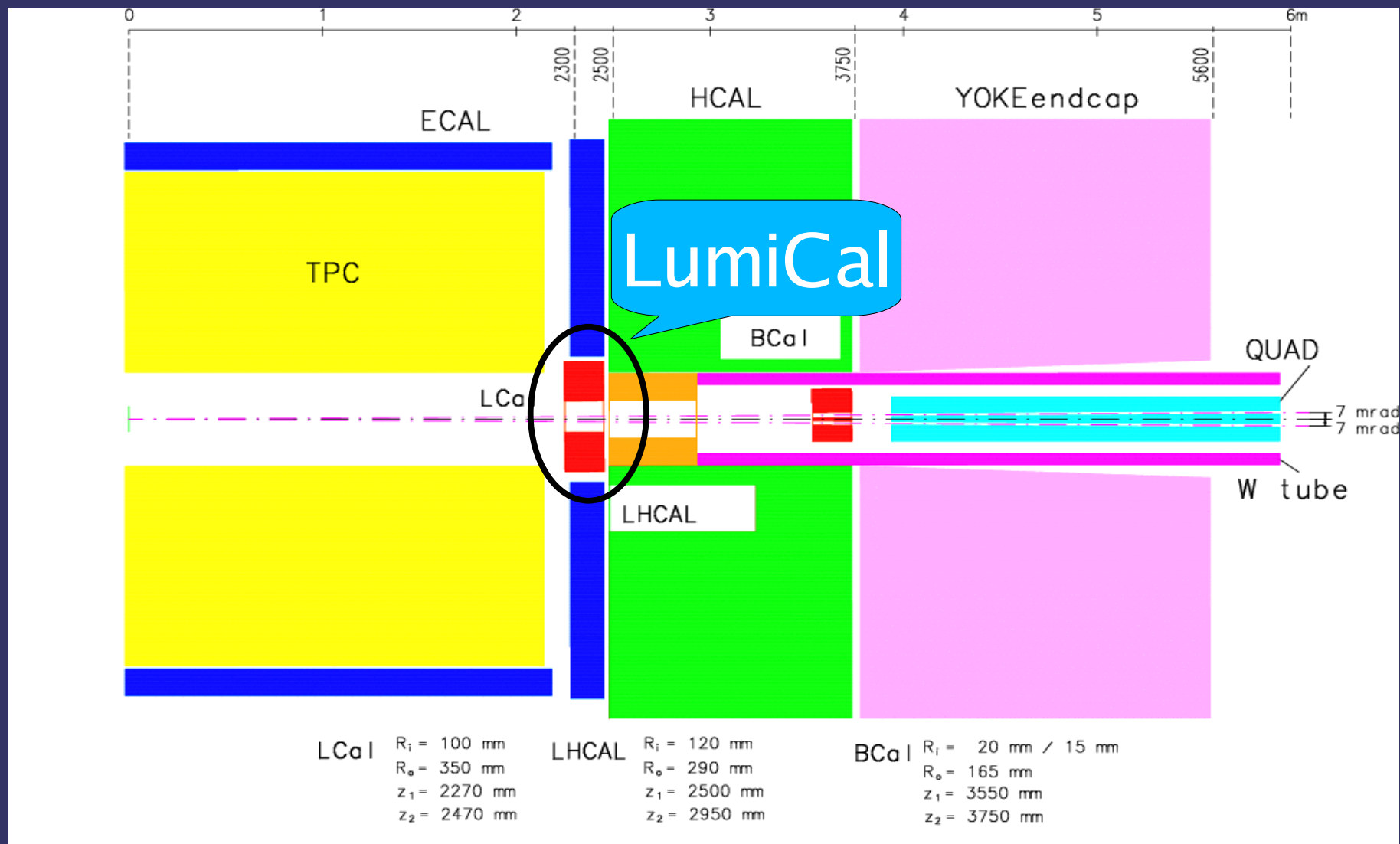
M. Idzik

on behalf of FCAL Collaboration

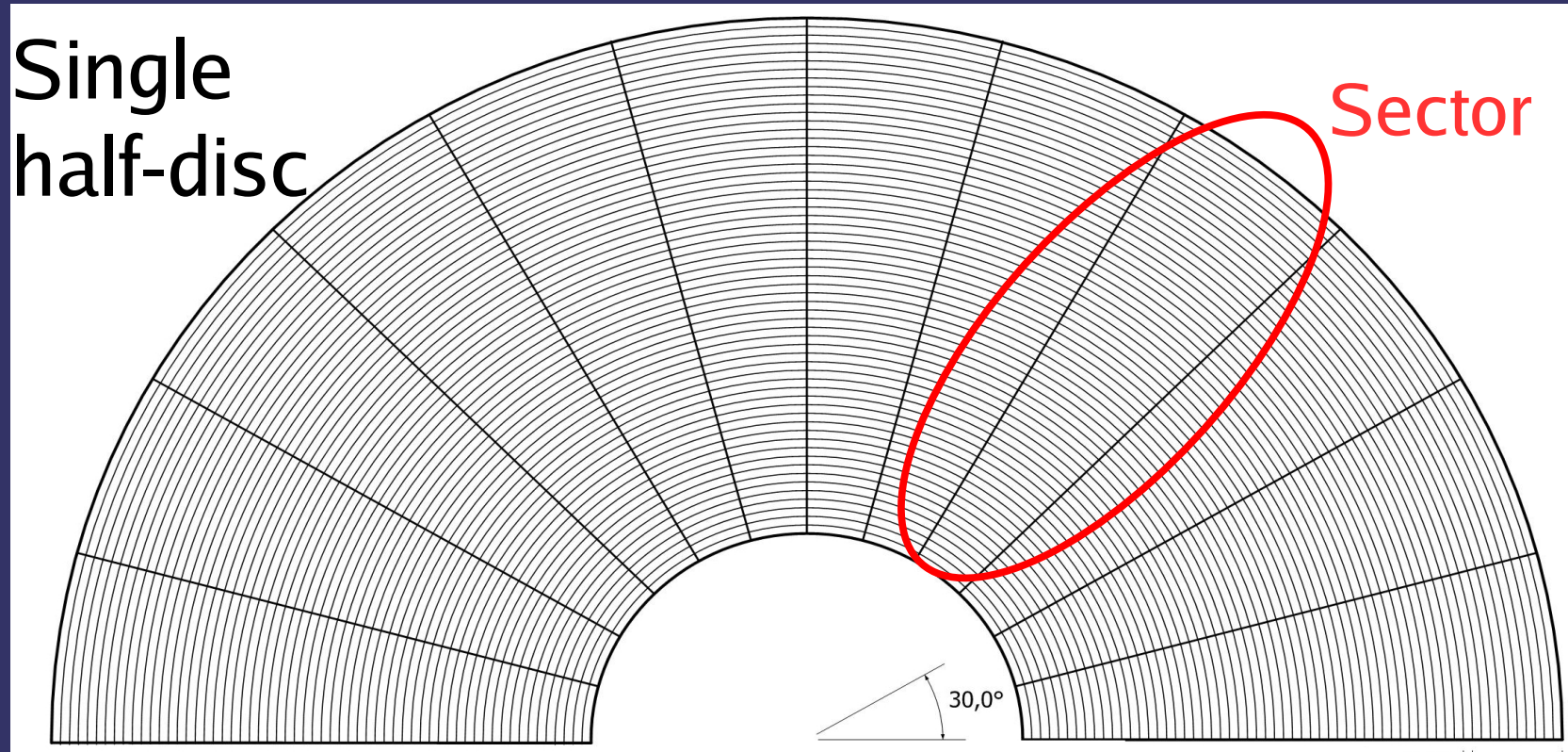
Outline

- ➔ LumiCal detector overview
- ➔ Specifications & implications for front-end
- ➔ Noise considerations - theory
- ➔ Front-end design & preliminary simulations
- ➔ Overall readout architecture
- ➔ Summary & Schedule

General detector architecture



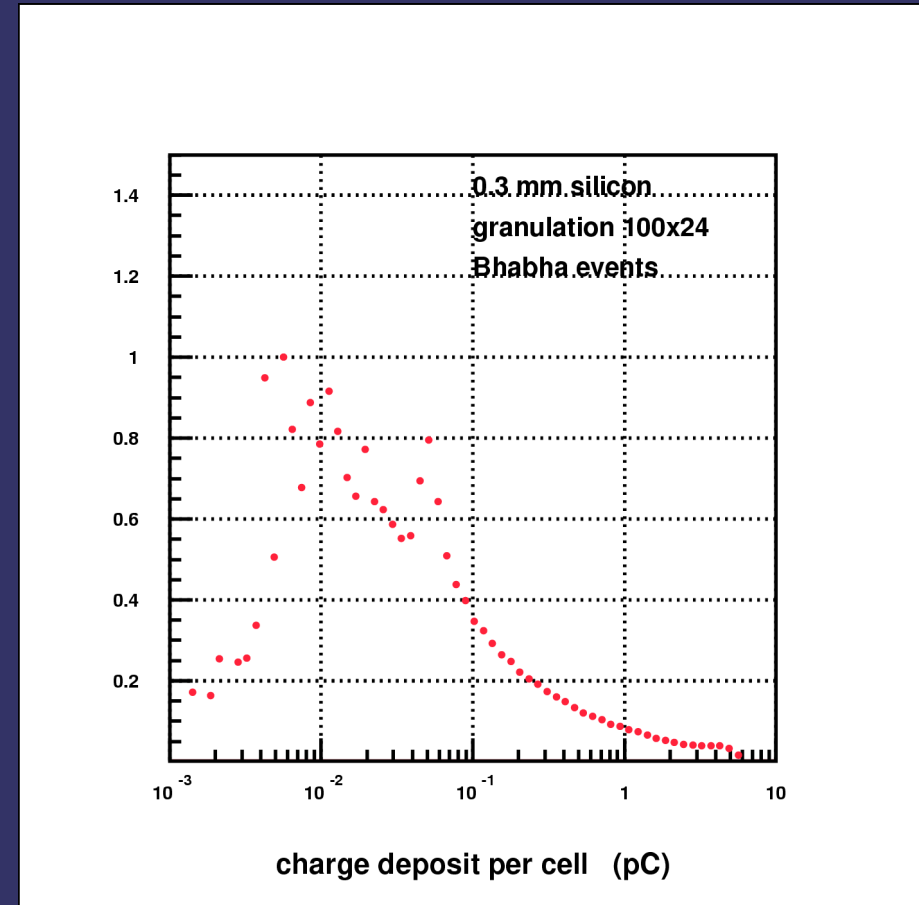
LumiCal architecture



- ➔ LumiCal \Leftrightarrow of 30 discs of silicon detectors ($300 \mu\text{m}$)
 - Disc \Leftrightarrow 24 azimuthal (15 degree) sectors
 - Sector \Leftrightarrow ($R_{\text{in}}=6\text{cm}$, $R_{\text{out}}=35\text{cm}$) built of ~ 100 radial pads

Specifications for front-end

- ➔ Signal: from 4fC (muons in test mode) up to $\sim 6\text{pC}$ (physics mode)
- ➔ Occupancy: up to $\sim 20\%$ (beam-strahlung), below 1% (bhabha)
- ➔ Detectors:
 - DC-coupled $300\ \mu\text{m}$ Si pads
 - C_{det} range: 20pF-120pF plus fanout ($\sim 1\text{pF/cm}$?)
 - Leakage current ?
- ➔ Inter bunch time: 330ns
- ➔ Power limitations ?



Front-end implications

Large C_{det} range



Charge sensitive configuration

$Q_{max} \sim 6$ pC



$C_f \sim 6-10$ pF

Test & Physics mode



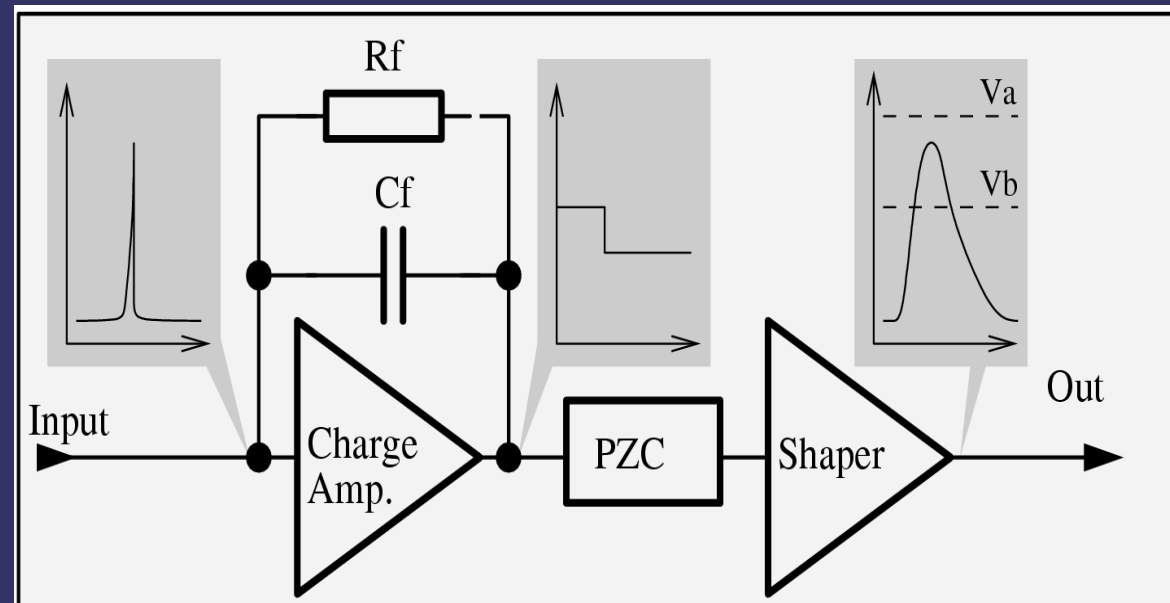
Variable gain

$\Delta t = 330$ ns, pileup



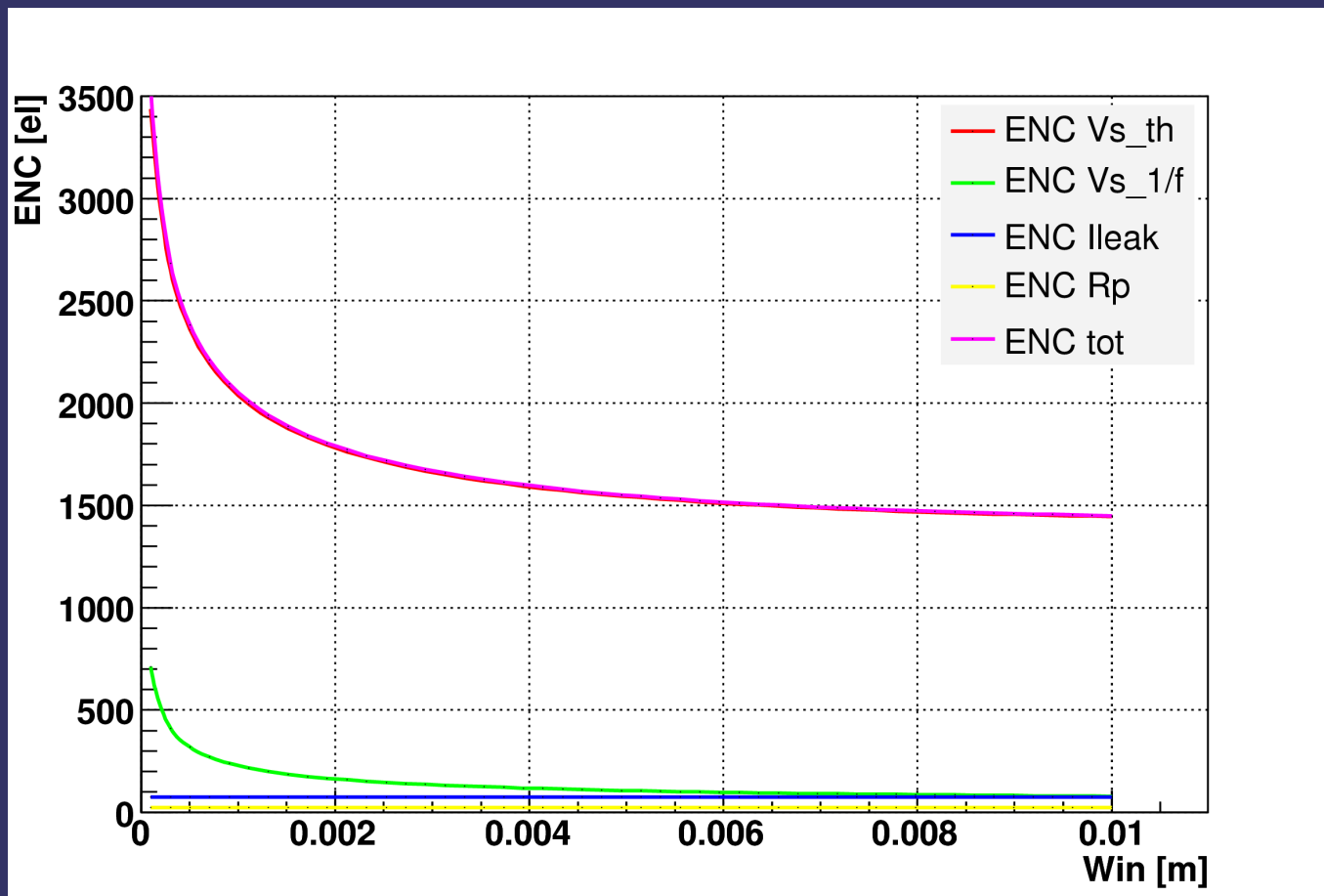
$T_{peak} \sim 50-70$ ns

Preamp+PZC+Shaper



Noise considerations - theory

- ➔ Input stage noise (ENC) simulations with EKV model
- ➔ Assumptions: AMS 0.35 μm , $C_{\text{det}} = 100 \text{ pF}$, $I = 2.5 \text{ mA}$, 1st order shaping, $T_{\text{peak}} = 50 \text{ ns}$, $R_f = 500 \text{ k}\Omega$, $I_{\text{leak}} = 10 \text{ nA}$



- ➔ Thermal noise dominant
- ➔ S/N=10 possible for MIP (24000e-)
 - $W_{\text{in}} > 2000 \mu\text{m}$
 - $I > 2 \text{ mA}$

Front-end design

⇒ Folded cascode amplifier

- $I \sim 2.5\text{mA}$
- PMOS input, $\sim 5000/0.4\mu\text{m}$
- $R_f \sim 500\text{k}$

⇒ Physics mode:

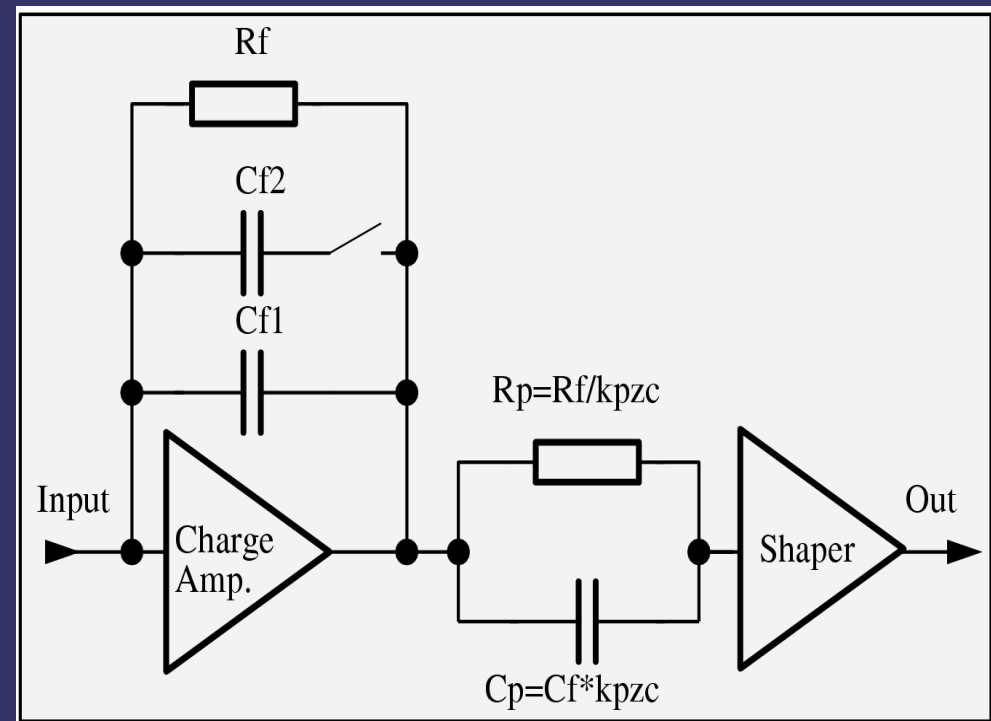
- $C_f = 6\text{-}10\text{pF}$, $k_{\text{PZC}} = 1$

⇒ Test mode:

- $C_f \sim 0.5\text{pF}$, $k_{\text{PZC}} = 10\text{-}20$

⇒ Shaper:

- $I_{\text{sh}} \sim 0.6\text{mA}$
- 1st order, $T_{\text{peak}} = 50\text{ns}$
- variable gain

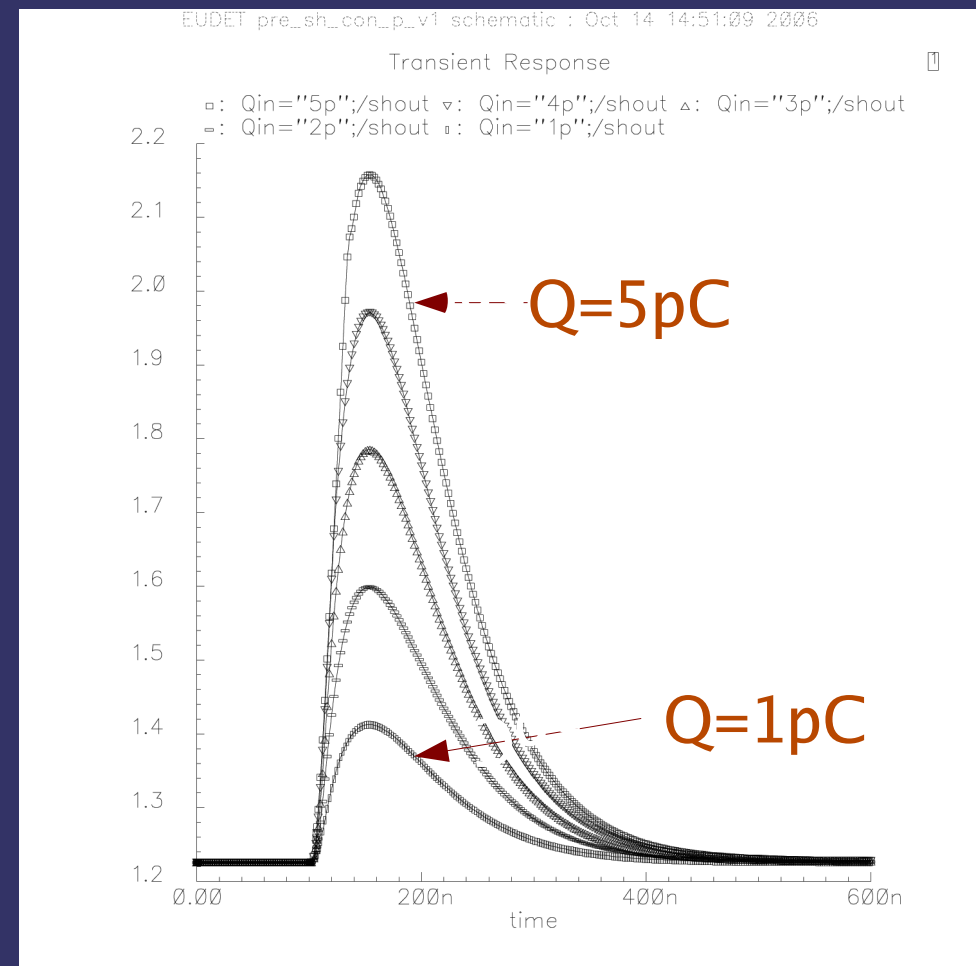


Preliminary simulations

Noise performance

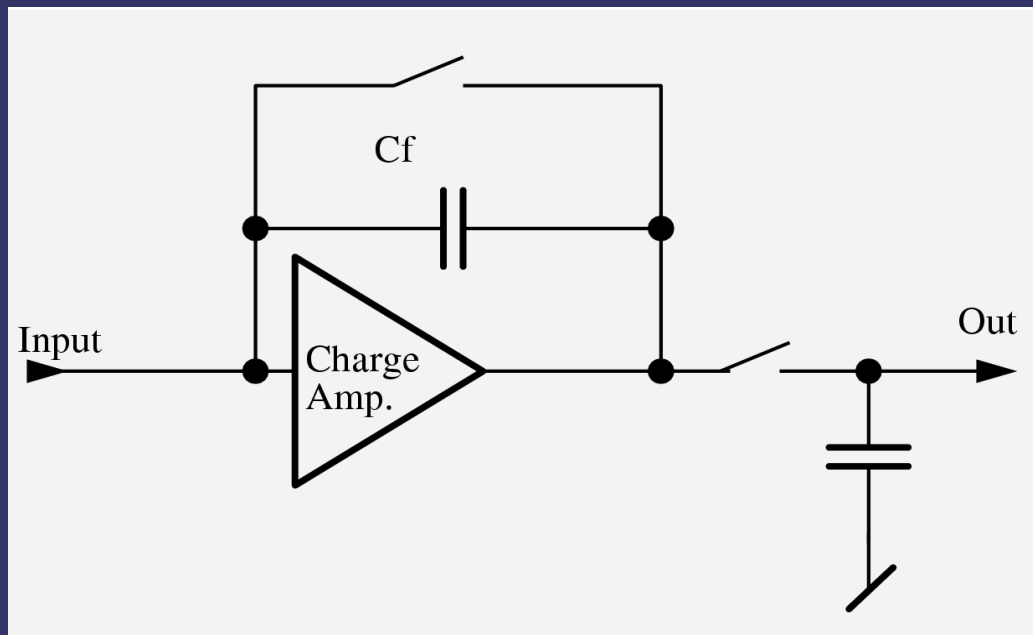
- ⇒ Test mode:
 - $S/N \sim 10$ ($ENC \sim 0.4$ fC)
- ⇒ Physics mode:
 - dynamic range > 11 bit

Linearity



Alternative front-end

Switched integrator configuration



⇒ Simulations in progress...

Readout solutions to consider



- ⇒ Is there an advantage from having a derandomizing buffer in each channel ?
- ⇒ ADC inside the chip or external ?
- ⇒ Data stored in local memory during the train or sent immediately ?
- ⇒ Which data protocol ?

Derandomization buffer

⇒ Advantages:

- Low frequency ADC/channel can be used OR high frequency ADC multiplexed to number of channels
- Lower averaged power per channel

⇒ Disadvantages:

- More complicated design
- More man power
- Possible buffer overflow

Analog to digital converter

	External (commercial)	Internal (custom)
Need to be design	No	Yes
Space on PCB	a lot	No
Control	complicated	easier
Price & power	comparable	

Texas Ins.
ADS 5277 10bit, 0.9W
65MSPS, 8 chan.
\$32 = 25.5 €
Tot. \approx 20 k €

10bit, 55mW
40MSPS, 1 chan.
2.6 mm²
Tot.(P&P) \approx 25 k €

I.Mehr and L.Singer ISSC vol. 35, pp.318, 2000

Memory and data transmission

	Test mode	Bhabha
Occupancy	<0.2%	5.5%
Direct transmission*	7.88 Gb/s	5.22 Gb/s
InterTrain transmission*	23.6 Mb/s	15.62 Mb/s
Data per Train*	7.1 Mb	4.7 Mb

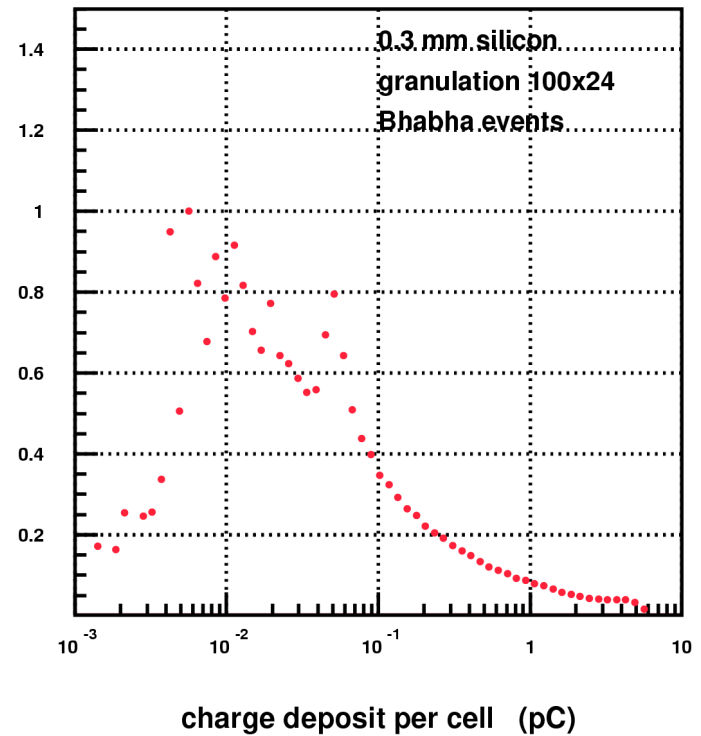
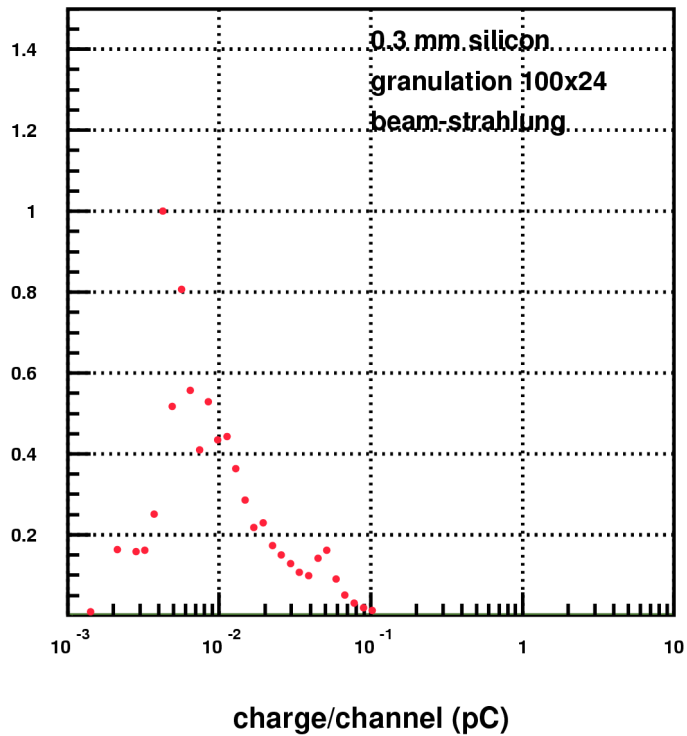
*Calculations done for half-disc unit

Both solutions: Direct and InterTrain transmission seem feasible
We should watch commercial solutions!

Summary & Schedule

- ➔ The work on LumiCal Readout Electronics has just started (~1 month)
- ➔ First prototypes of Front-end (and maybe something else) will be submitted in ~2-3 months
- ➔ More detailed study on Readout architecture needed (compatibility with mechanical and cooling design!)

Charge deposition



Front-end electronics

