

ECAL EUDET MODULE

Summary talk

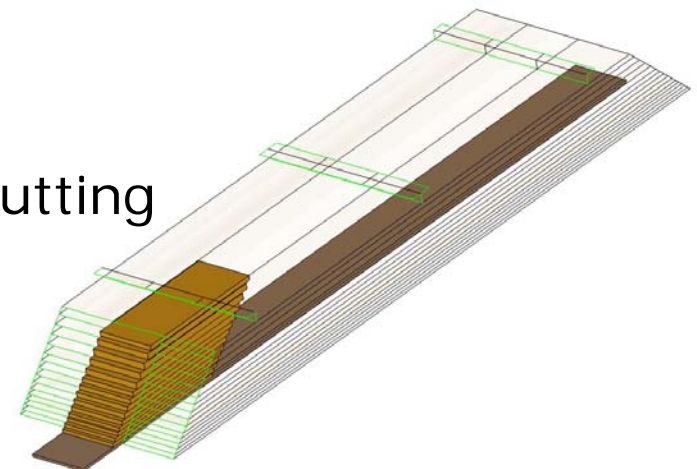


EUDET annual meeting, oct, 20, Munich



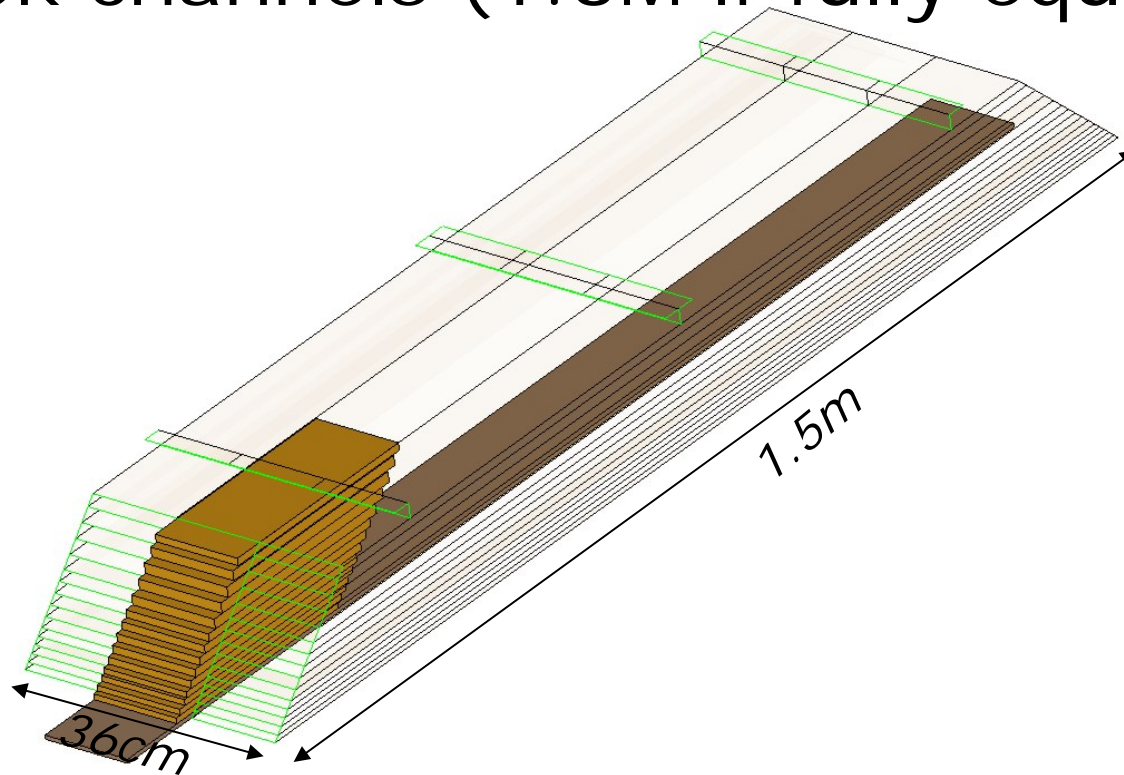
Goal of the program

- Mechanic
 - Validate a full length structure
 - Validate fastening
 - Validate thermal calculation
- Silicon sensor
 - Validate physical behaviour
 - Validate costing and production feasibility
- Electronic
 - Validate front-end ASIC
 - Ultra low consumption
 - System on chip
 - Daisy chaining and data outputting



EUDET module overview

- Full length structure
- 500kg radiator
- 40k channels (1.3M if fully equipped)

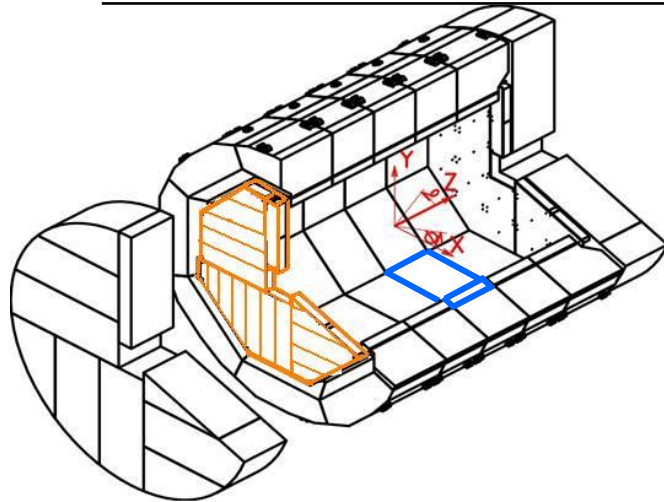




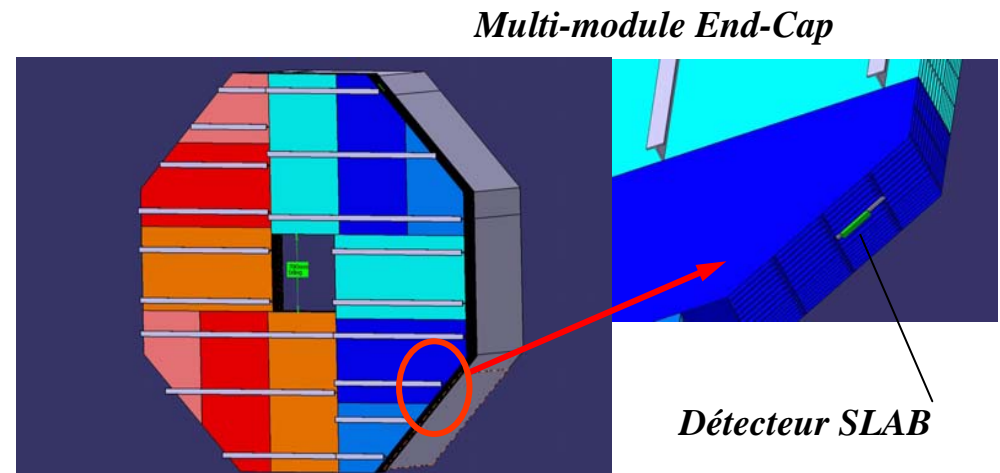
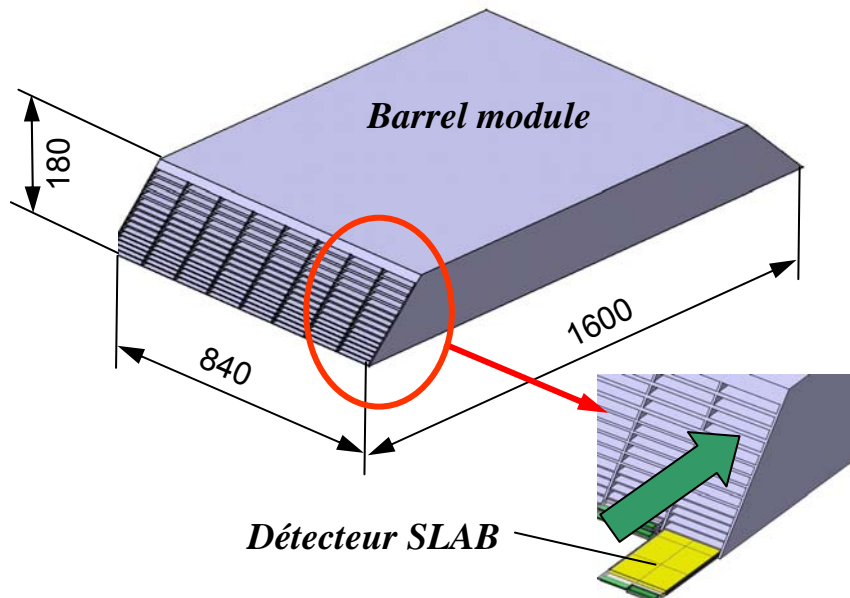
Mechanical R&D

On behalf of Marc Anduze & Denis Grondin
LLR/LPSC

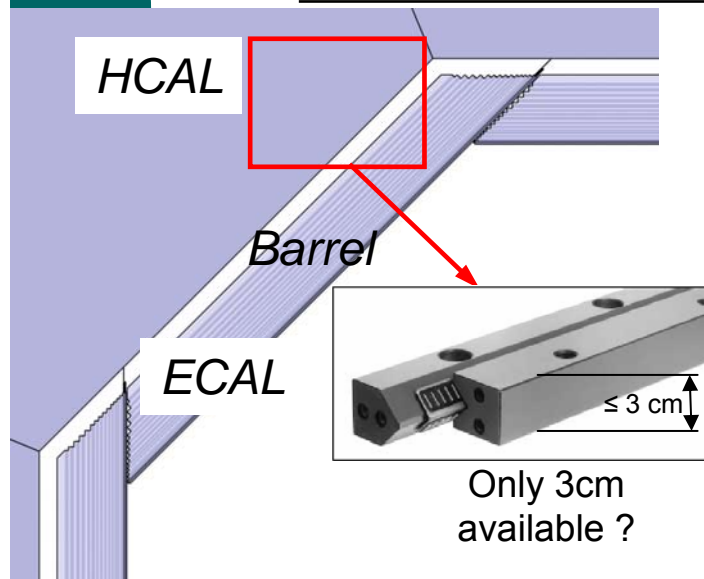
ECAL for LDC- Global presentation



- W/Si calorimeter (24 X_0 with 29 W layers)
Weight full ECAL: ~ 112 T (80 barrel+32 End-Cap)
- Barrel : 40 identical trapezoidal modules
- End-Cap : constituted of 12 modules (3 types)
- ECAL module : alveolar structure - carbone fibers compound including half of W plates (fixed on HCAL End-Cap with rails)
⇒ Minimization of dead zones
- Detection elements (detector slab) in each alveolar case (Si+W), FE chips integrated, pad size : 5×5 mm²

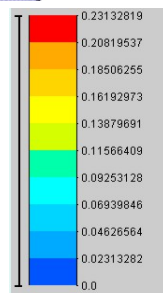


ECAL/HCAL - Interface

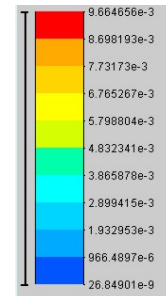
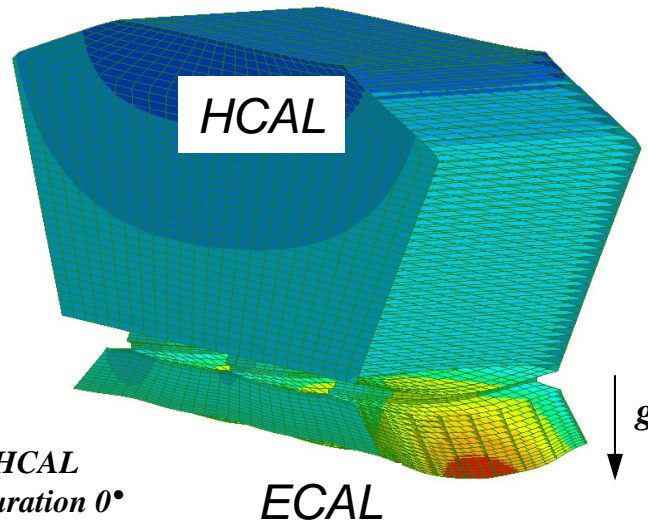


Fastening system ECAL/HCAL is **fundamental** for mechanical and thermal calculations (barrel and End-Caps):

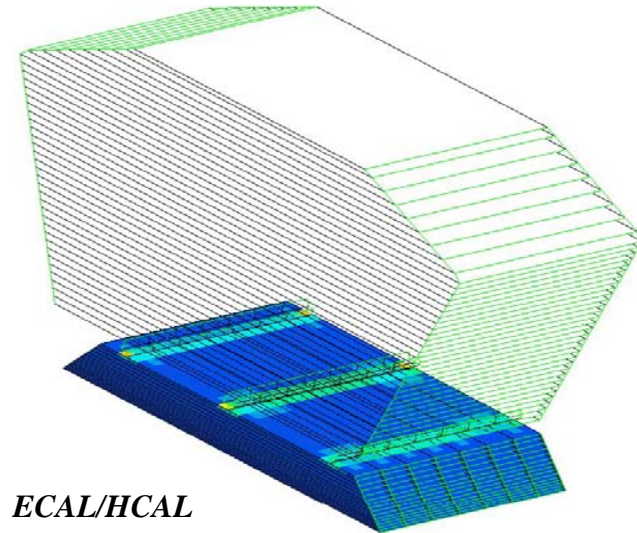
- choice of **fasteners** : rails directly inside composite or metal inserts ?
- **Connections** set path in gap between ECAL and HCAL (via a panel for cabling interface ?)
- Rails are 1 way for **positioning system** (gravity support) but a second complementary system may be added for fast interchange of modules... recommendation ?
- Whole End-Cap (ECAL+HCAL) **assembly behavior**



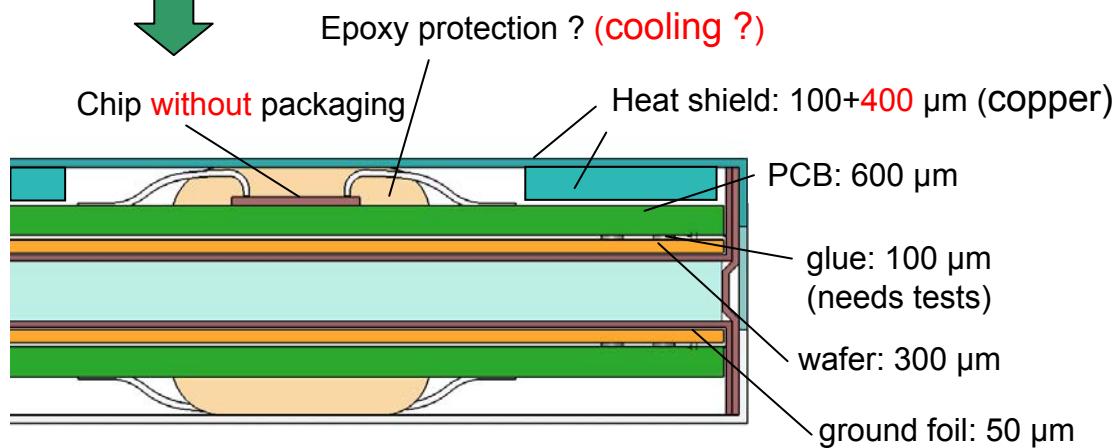
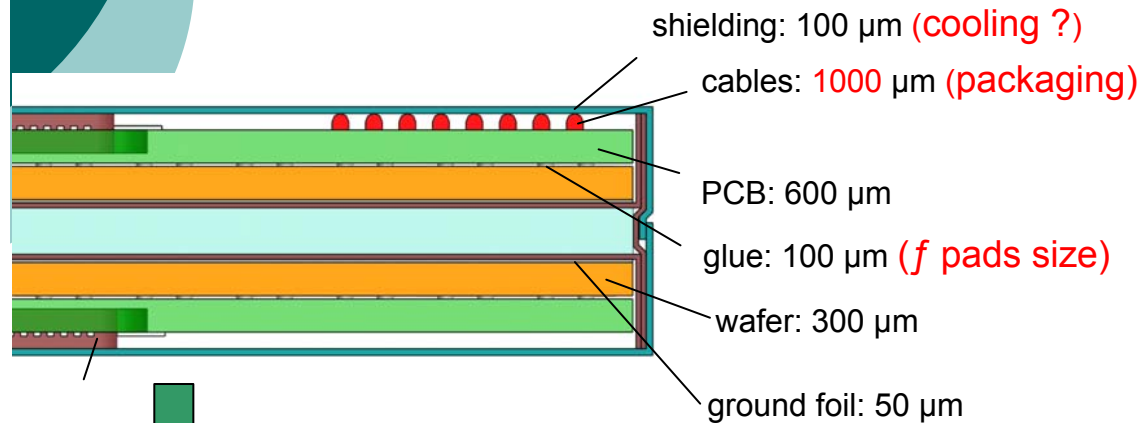
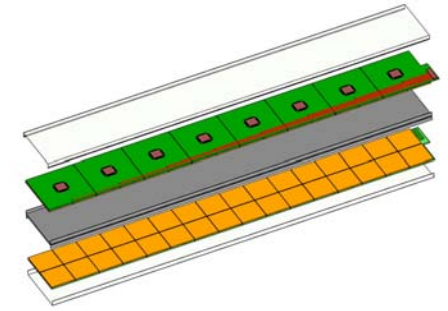
ECAL/HCAL
Configuration 0°



TSAI-HILL ECAL/HCAL
Configuration 0°



ECAL - Detector slab



Main ISSUES :

Front End chips **inside** :

- ⇒ Thermal dissipation (cooling ?)
- ⇒ Chip behaviour in an electron shower
(tests with a thin PCB in October 2006)
- Long structure :
 - ⇒ Design and fabrication problems
(composite with segmentation of W plates, mechanical behaviour ...)
 - ⇒ Segmentation of PCB (design of an interconnection)
- Diminution of the pads size
 - ⇒ Increases of the number of channels
(thermal cooling ?)
 - ⇒ Size of glue dots

ECAL - Thermal analysis

Thermal sources:

Pad size	Chan/ wafers	Ch/chip	Chip/wafer	Chip size mm ²	Chan/barrel	Chan/ End-cap
5*5 mm ²	144	72	2	15x15	60.4 M	21.8 M

→ CALICE ECAL: ~ 82.2 M of channels

Assuming that the chip power is 25 μW/channel

total power to dissipate will be : 2055 W

⇒ external cooling OK

inside each slab :

necessity of cooling system but active or passive ?

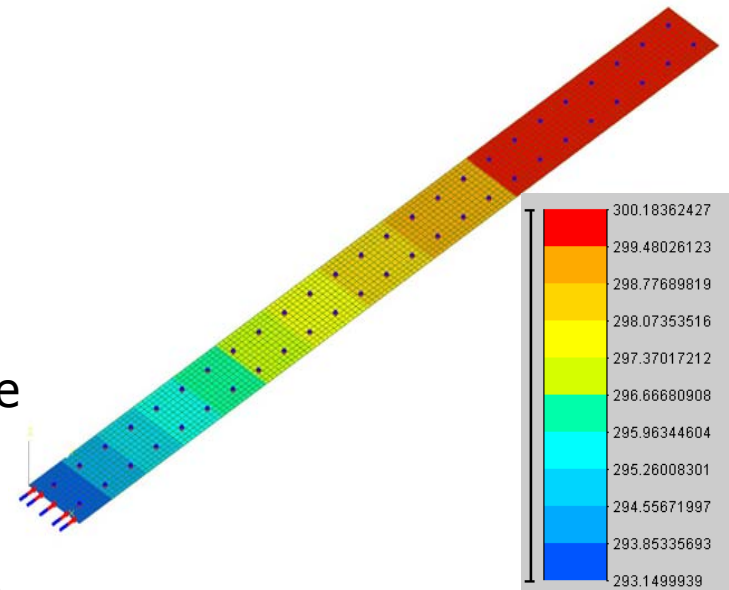
Ex: Pessimist simulation of heat conduction just by the

heat shield : $\lambda = 400 \text{ W/m/K}$ (copper) ; $S = 124 * 0,4 \text{ mm}^2$

$L = 1,55 \text{ m}$; $\Phi = 50 * \Phi_{\text{chip}} = 0,18 \text{ W}$

We can estimate the temperature difference along the slab layer around 7°C and without contribution of all material from slab (PCB, tungsten, carbon fibers...)

⇒ passive cooling OK ?



Conclusion

R&D – EUDET module (2006-2007)

○ Long Type H structures :

- Design and fabrication of the **long mould** – (end of 2006)
- **Fabrication** of validation model (1-3 samples)

○ module EUDET :

- **1.5 m** long ; **≈ 500 Kg**
- real radiator sampling : **20** layers with **2.1** mm thick
9 layers with **4.2** mm thick

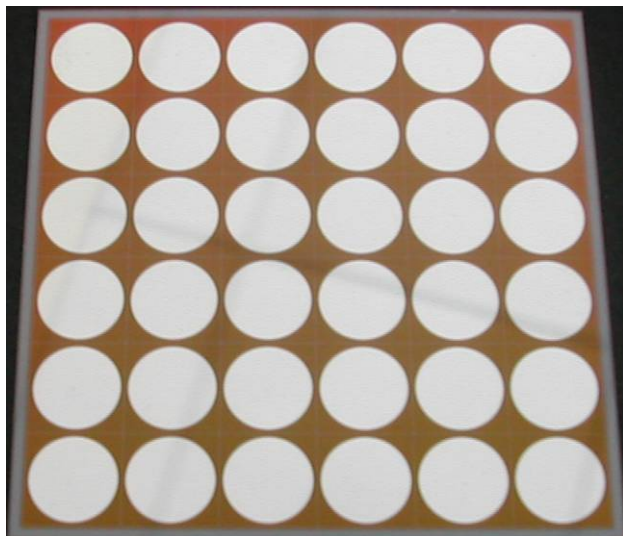
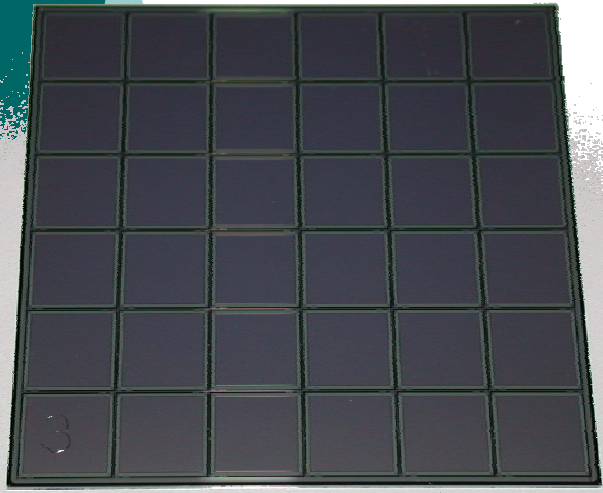
- **Design** (mechanical and **thermal** simulations) of the module
- **Optimization of composite sheets** : studies of main parameters (thickness, shape ...)
- **Fastening system** on HCAL : design and destructive tests too
- Design and fabrication of **the mould** with an **industrial expertise** (DDL consultants)
- Transport **tools**
- **Fabrication of the structure** (end 2007)
- **Mechanical support** for beam test in 2008



Silicon detector R&D

On behalf of Jean-Charles Vanel
LLR

Starting point : the physic prototype



- Several producer
 - To manage production risks
 - Russia
 - Czech Republic
 - Korea
 - Brazil
 - India
 - Contact with Hamamatsu

*Final detector :
Cost driven*

Conclusion - Parameters change



*300 wafers needed
for EUEDET module*

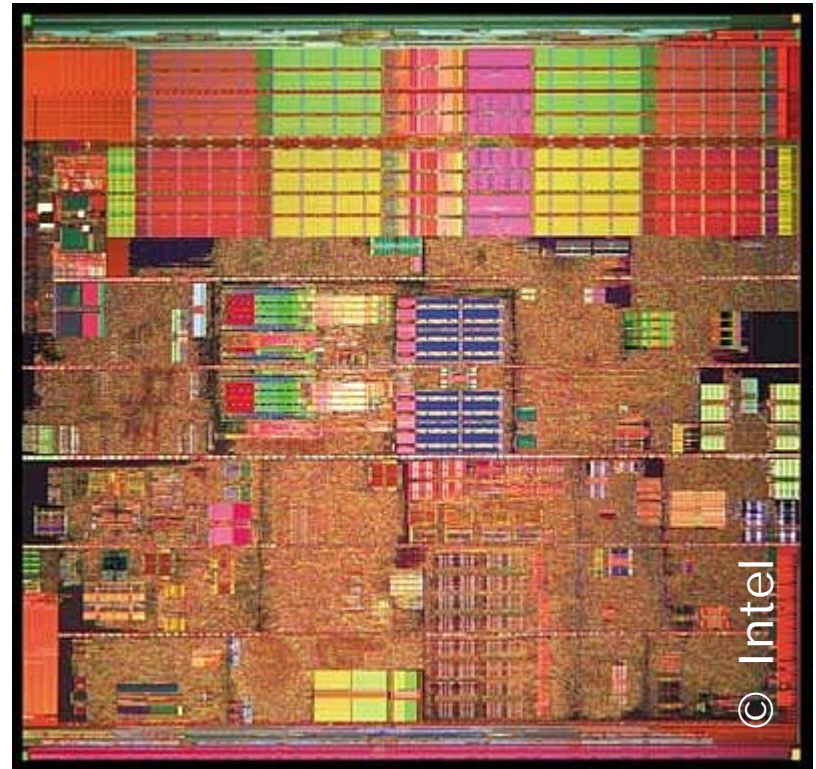
- Still under development
- Many parameters to be analyzed
- EUEDET is crucial for good detector optimization

*CRUCIAL for slab design : is it possible to embed the DC block capacitance ?
→ VERY QUICK INVEST NEEDED !*

Electronic R&D

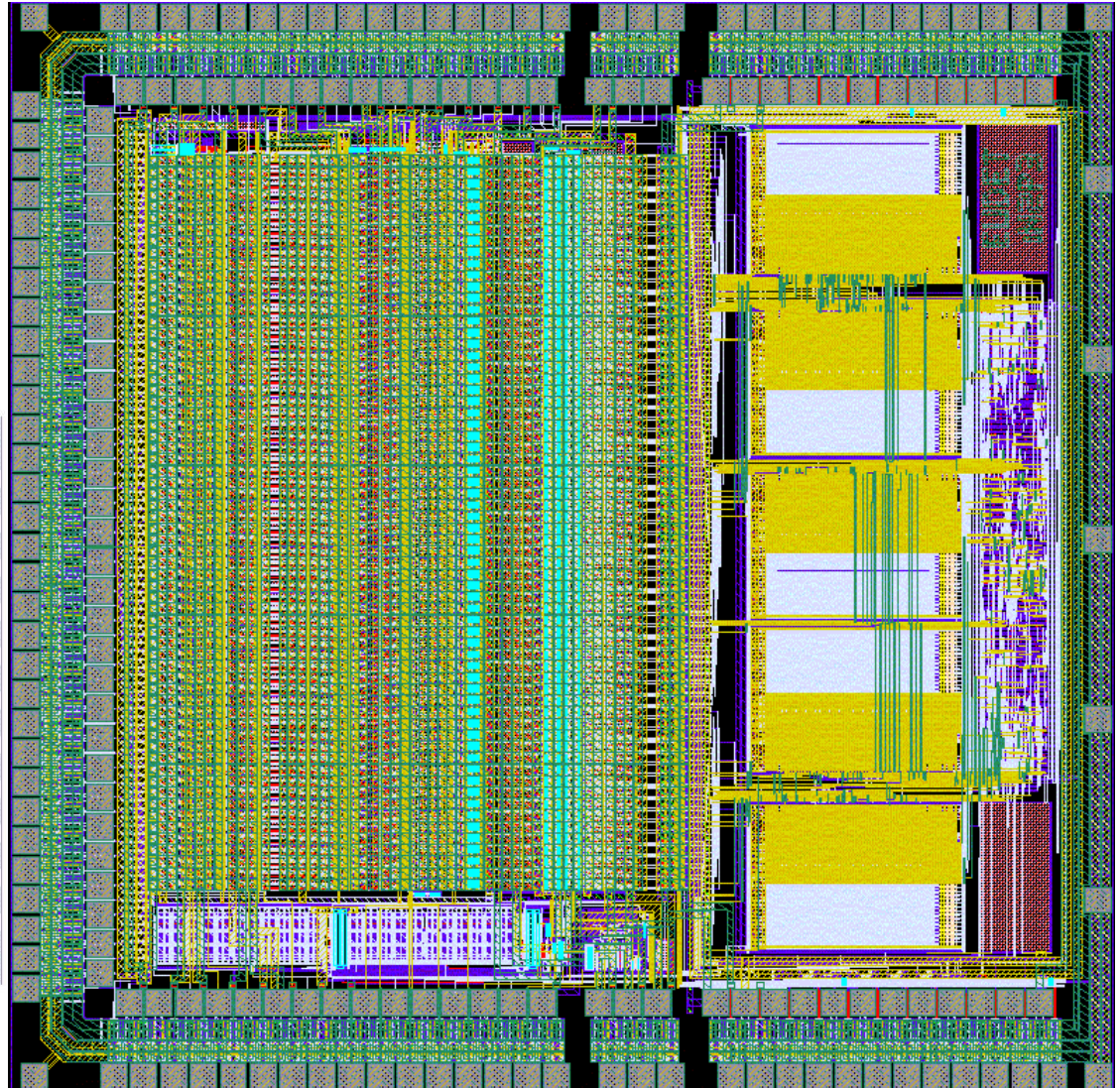
ILC_PHY5

In behalf of :
LPC/LAL/LLR/UCL

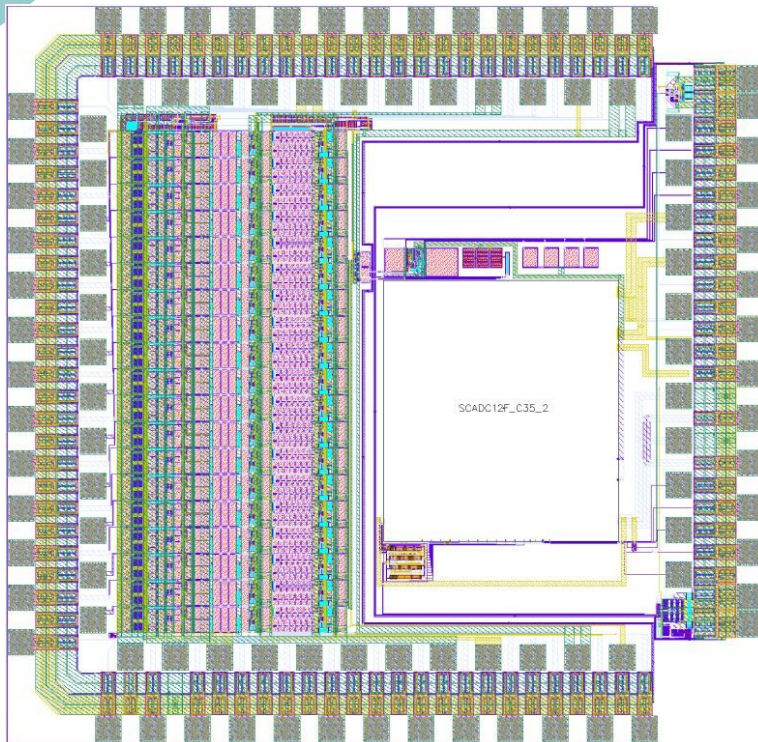


System on Chip design

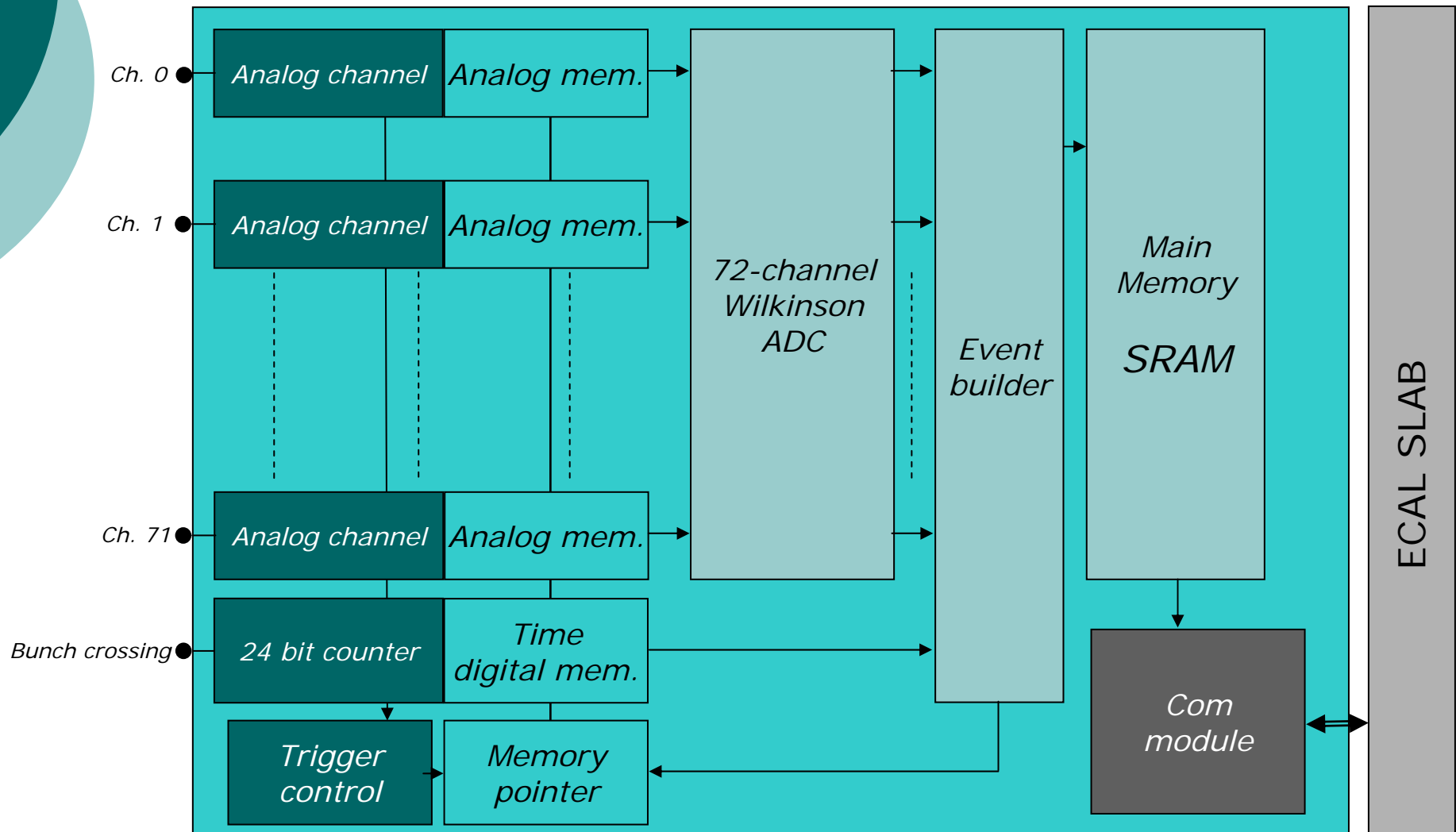
HaRD_ROC (2006)



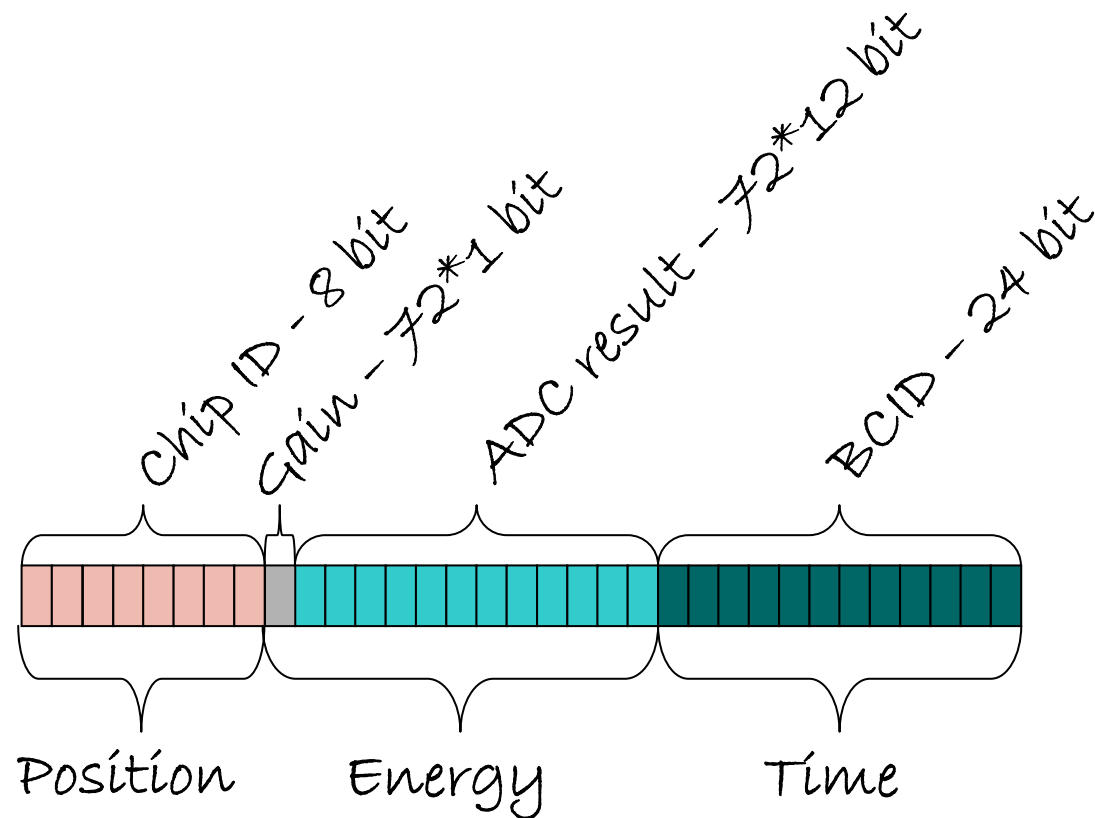
ILC_PHY4 (2005)



General block scheme of VFEE



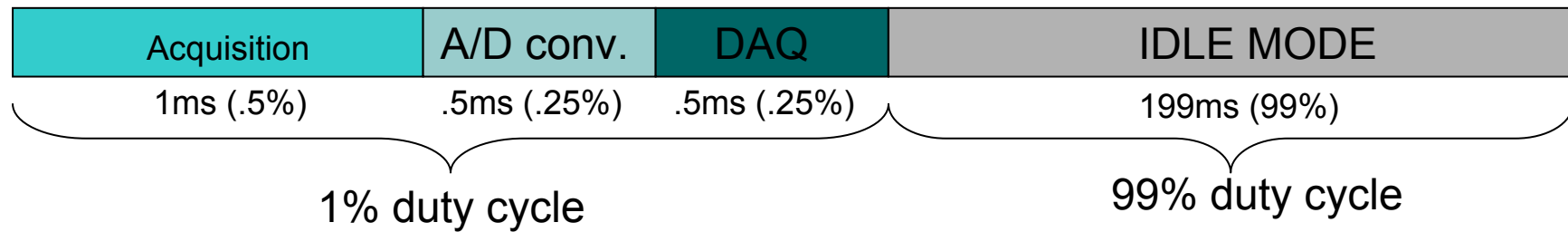
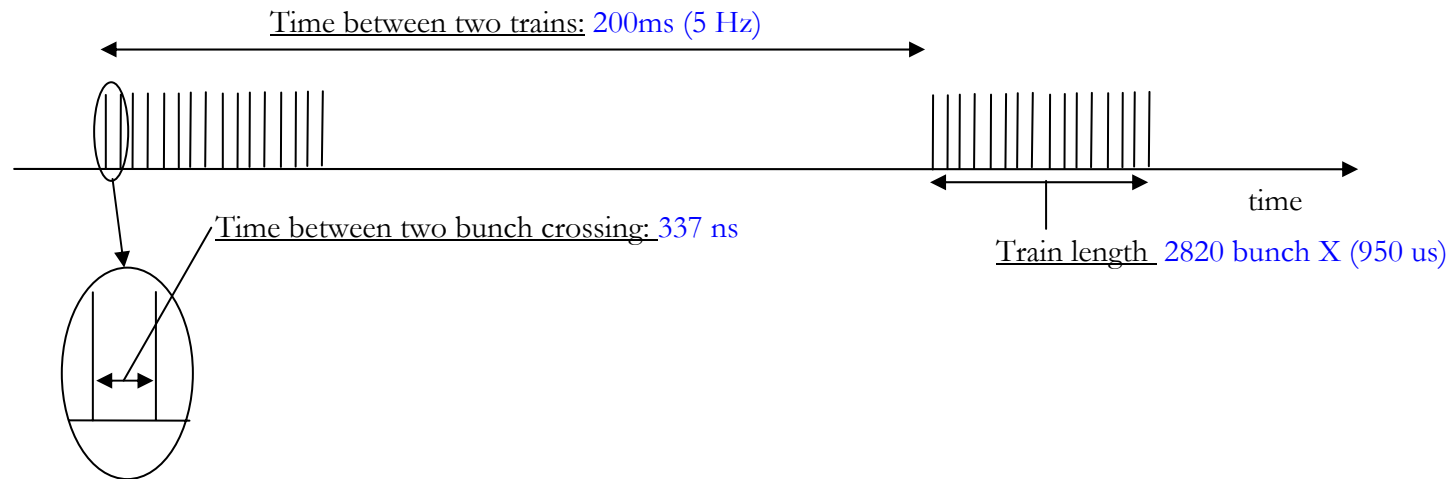
One ILC_PHY5 event



→ 968 bits / chip event

- Depth is 5 because of room on silicon

Time considerations





Consumption

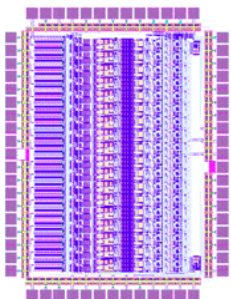
- The goal is $25\mu\text{W}/\text{ch}$. (with Power Pulsing)
 - The analogue part consumption :
 - is $2.3\text{mW}/\text{Ch}$. Without Power Pulsing
 - ie $11.5\mu\text{W}$ with 99.5% Power Pulsing
 - The ADC part consumption :
 - is $3.7\text{mW}/\text{Ch}$. Without Power Pulsing
 - ie $9.25\mu\text{W}/\text{Ch}$. With 99.75% Power Pulsing
 - Need to estimate digital part consumption
- So far, on track

Conclusion on electronic R&D

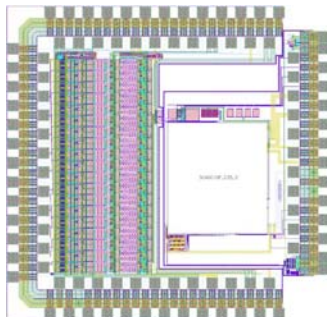
- Work is going on
 - For ASIC R&D, with a crucial interaction with DAQ
 - For PCBs R&D to equip long slab
- Complexity of ASIC increases quickly
 - To simplify PCBs and achieve thickness requirement
 - Mixed design issues, system aspect of the ASIC
- Collaboration is very efficient and fruitful. It shall achieve the outstanding expectations within the very tight schedule

ILC_PHY5 (2006)

FLC_PHY3 (2003)



ILC_PHY4 (2005)



HaRD_ROC (2006)

