EUDET JRA3
DAQ Status

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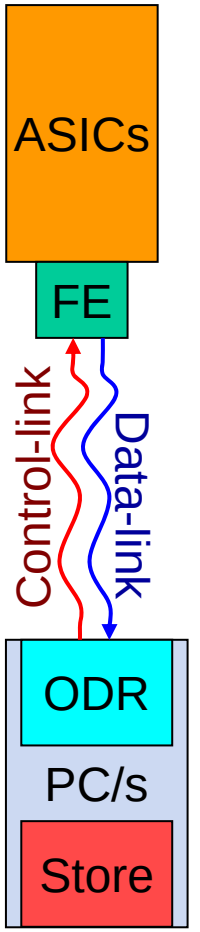
20 October 2006

Overview

- General DAQ goals
- Details of current design and status:
  1. Front-End interface to sub-detector (FE)
  2. Data-link (FE to Off-Detector Receiver)
  3. Off-Detector Receiver (ODR)
  4. Control data-link (Clock, Control to FE)
  5. Data Store
  6. Software
- Summary

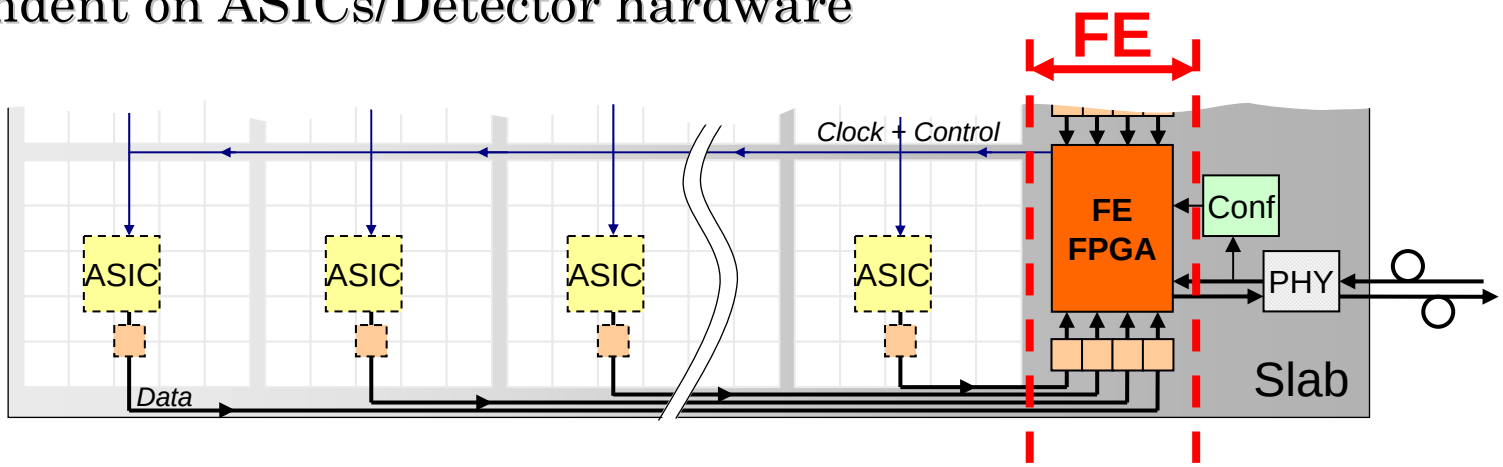


DAQ Goals

- Use commercial components where possible:
  - -Readout links use standard connectors and protocols
  - -PCs with PCI (-Express) cards
- Modular
  - -Generic readout board for all users
  - -Detector specific interfaces as plug-in modules
  - -Other 'bespoke' functionality in firmware
- Front end control attempts commercial hardware too
  - -Extract 'fast' signals from commercial signalling
- DAQ software generic
- Failure protection (fail-over)
  - -PCs not reliable – reroute signals on-the-fly

Front End Interface (FE)

- Interfaces directly with sub-detector ASICs
  - Collects data (and buffers) for transmission
  - Provides clock+control signals
- Formats data for specific data link protocol (S-Link, Ethernet, raw etc.)
- FPGA based
- Assume plug-in module at edge of detector
- Dependent on ASICs/Detector hardware

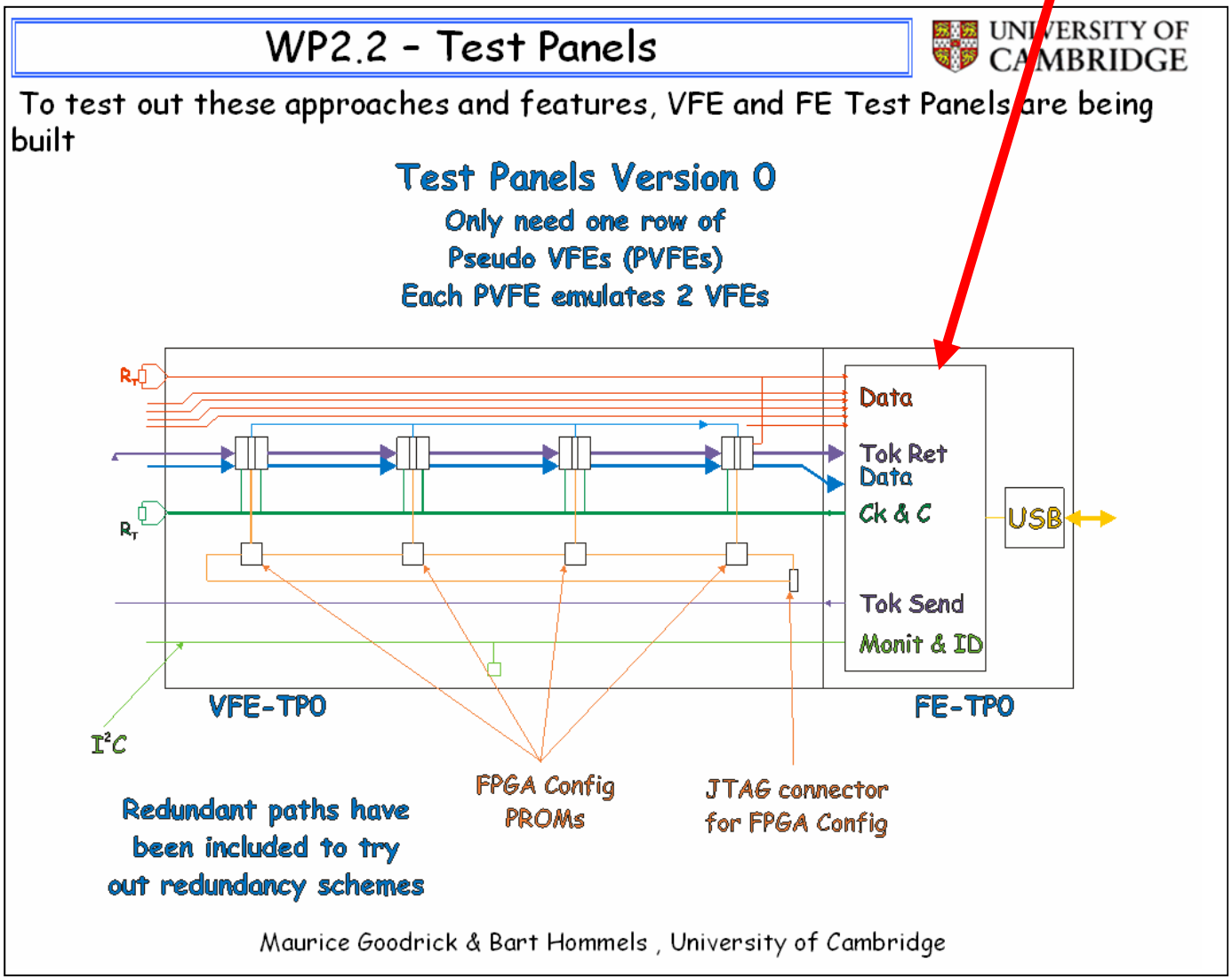


- BUT is the FE part of DAQ?
  - For ECAL, UK groups are active: e.g. Cambridge has test FE ...

FE with ECAL 'Test-Panel'

FPGAs emulate ASIC using same digital part (VHDL)

'FE' reads out these 'chips'



FE with ECAL 'Test-Panel'

WP2.2 - PCB Status

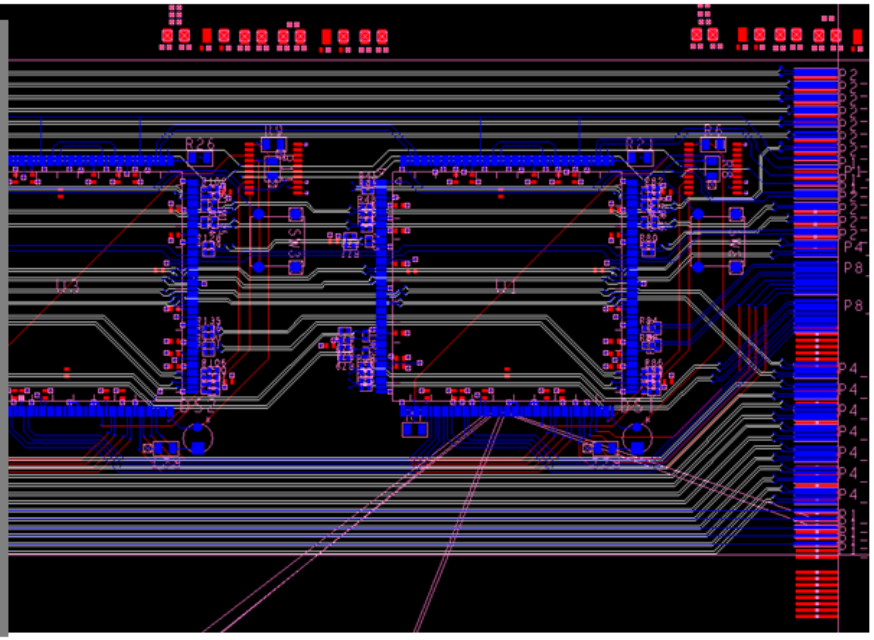
UNIVERSITY OF CAMBRIDGE

Features thin (64mum) layers and narrow (75mum) traces

Traces for various clock distrib'n schemes and/or readout architectures incorporated in design

Rows of 4 FPGAs/board

Every FPGA mimics 2 VFE chips



- Board schematics are 'finished'
- PCB layout now completed

Maurice Goodrick & Bart Hommels , University of Cambridge

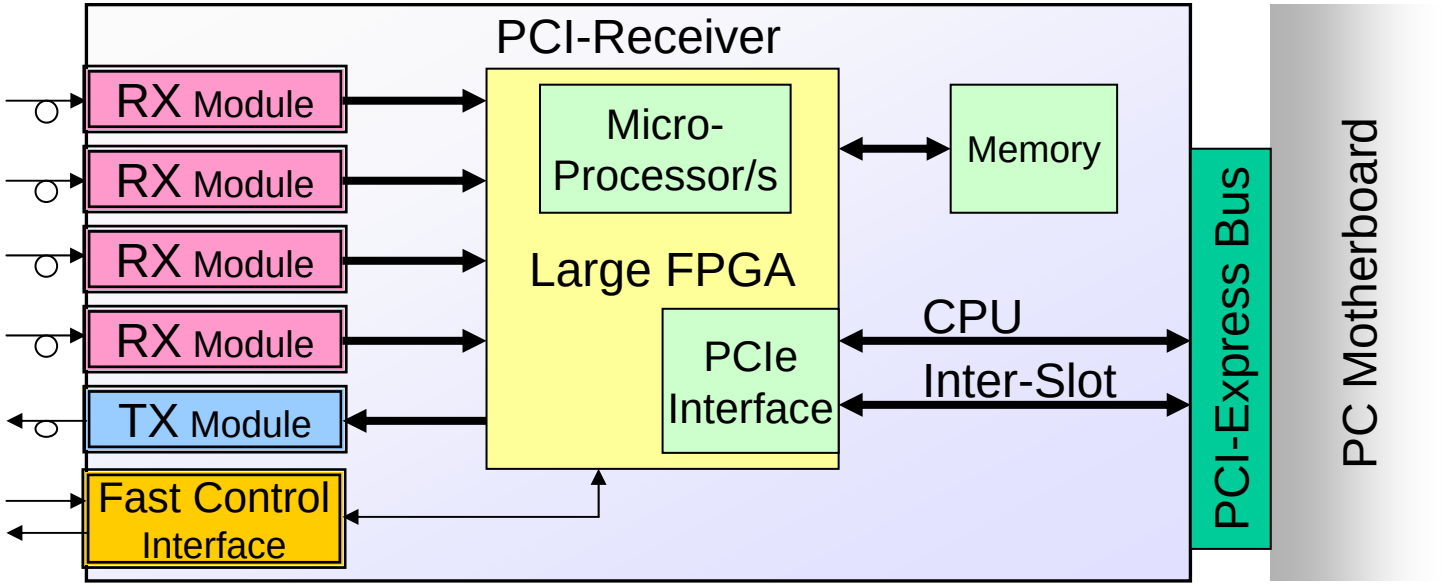
Data-link

- This is the physical link (regardless of protocol)
  -Both ends
- Use commercial components and standards
  -E.g. HSSDC2, SFP with Ethernet, S-Link etc.
- Can be copper or fibre
- Assume multi-Gigabit rates
- No-brainer (if it works at all) – first time we see the data is when presented by a FIFO inside the FPGA

HSSDC2 SFP

Off-Detector Receiver (ODR)

- PC based, with PCI-Express cards
- Cards as generic as possible
  - Detector specific firmware
  - Interfaces to data-link via plug-in modules
- Can act as an FE – good for testing FE firmware early
- Provides capability for fast-controls



ODR(2) - Hardware

Using development board that suits our needs well:

"PLDA XpressFX" (www.plda.com)

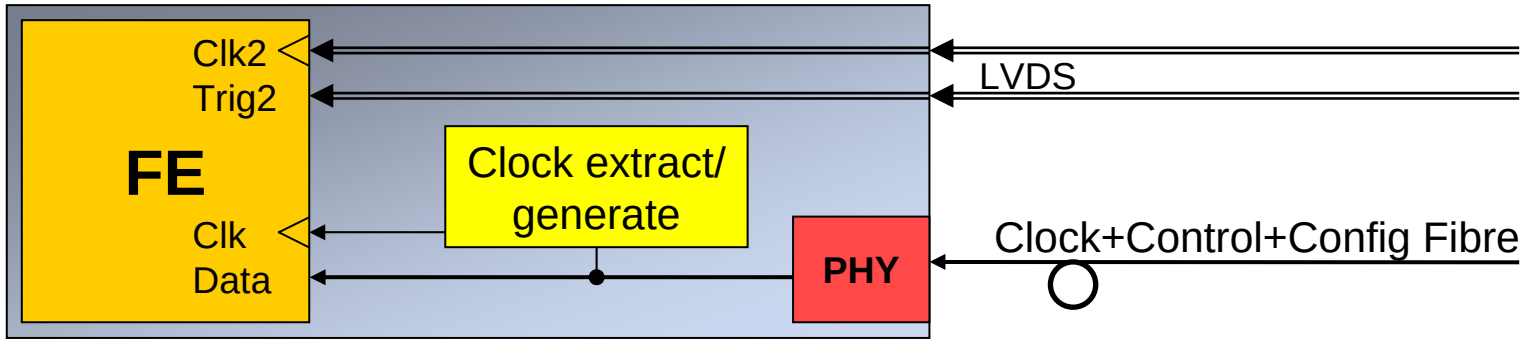
- PCI-Express endpoint firmware 'core' included.
- Based on Xilinx Virtex 4 FX100 FPGA (huge + 2xCPU)
- Suitable for 'Module 0' DAQ
- 4x 2.5 Gbit interfaces (bi-dir)
- 4 more via plug-ins
- 128 MByte RAM
- 8 lane PCI-Express

ODR(3) - Status

- Cambridge, Manchester, RHUL, UCL each have a PLDA board (late June).
- Each have a hardware development PC
- Basic Linux driver software working (SLC4)
- PCI-Express core working
  - Can read/write to the board (flash LEDs!)
- Ethernet interface is working
- Memory controller in progress
- Complete data transfer system by end of year.

Control-link (Clock and Control)

- Provides timing synchronisation and configuration for FE and ASICs
- Use data-link hardware:
  - -Attempt to recover clock and timing from link
  - -Good trigger/timing signals too?
- Fall-back: provide discrete interfaces
  - -Clock
  - -Trigger
  - -Power-pulsing



Datastore and Software

Keep it simple!

Raw data written to locally mounted/NFS disk

If data volume increases – use generic firmware algorithms to compress data (ZIP)

Could use LCIO if feasable …

Status:

- Data storage software is under-development
  - Part of driver
- Full-scale DAQ:
  -UK meeting in 2 weeks to discuss.
  -Share load with other detectors?

Summary

- Front End: **IN-PROGRESS**
  - FE 'Test-Panel'

- Off-Detector Receiver: **IN-PROGRESS**
  - Hardware in place
  - Driver working
  - Firmware under-development

- Control Link: **LATER**
  - Can use some ODR firmware.
  - Fall-back solution not difficult

- DAQ software: **TBA**

Prototype DAQ using ODR's as source and destination by the year end.