TDC-based readout electronics for LP TPC



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Annual EUDET meeting MPI Munich

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- The time of arrival is derived using the leading edge discriminator.
- The charge of the input signal is encoded into the width of output digital pulse.

Proof-of-principle experiments with GEM TPC at DESY



Measurements with laser induced tracks.



"First version" 16 channel ASDQ board: preamplifier and charge-to-time converter + CAEN TDC (VME, model v767)

Size of the connectors limits the size of the board.

First tests: 128 channels

Calculated residuals for all hits. Resolution in Z: RMS ~0.4 mm (@ Z=30cm)

> A.Kaukher, "A study of readout electronics based on TDC for the international linear collider TPC detector", IEEE Trans. Nucl. Sci. 53 (2006) 749.

The goal is to provide several hundred channels of compact readout electronics.

• Unified interface to the endplate of the LP TPC.

Allows concurrent or simultaneous data taking with TDC-based or ADC-based(ALTRO) readout electronics (University of Lund).

- Larger number of channels allows larger tracking area of the LP TPC endplate.
 - a) Study of the tracking performance with multi-GEM modules.
 - b) Calibration issues.
 - c) dE/dx capability.
 - d) ...even more exotic topics
- Data in LCIO format.

TPC data analysis "regardless" of the data source: TDC or ADC.

ASDQs and HPTDCs

Compact readout electronics can be built, if one places ASDQs and HPTDC on the same board.



photo by B.Warmbein

200 ASDQ ASICs have been purchased. Up to 1600 readout channels will be available.

5 HPTDC samples are available (Thank J. Christiansen, CERN). To study the feasibility of the operation of the sensitive analogue (ASDQ) and the digital (TDC) components on the same board, an *evaluation board* is being designed.

- Performance/Signal Integrity check.
 - an achievable threshold level of the ASDQ.
- TDC readout development.
 - digital data transmission with multiplexing.

Design: *A.K.* Implementation: *ZE-group at DESY.* (Spring 2007)

Test of readout electronics with mini-TPC

1. For simple tests with readout electronics signals from a pulse generator will be used.

- operability and calibration of the readout channels.

2. For standalone test of the readout electronics a simple mini-TPC detector (triple-GEM chamber) is being designed.

Main sources of signals: cosmics particles, radioactive-source (Fe⁵⁵). UV-laser induced tracks or charged particles at a test-beam facility, if available.

Design: *Oliver Schäfer* (PhD, University of Rostock) Implementation: *Workshop of the University of Rostock.* (Spring 2007)

Main features of the chamber:

- Triple GEM (gas gain $\ge 10^4$)
- No field cage: only short drift path (up to few cm)
- Interchangeable endplates:
 - for the "first version" of the readout electronics and
 - for the evaluation board/Final design.

Front End Card (FEC)/"Final design"



The Front End Card is (still) based on existing components:

- Four 8-channel ASDQ ASIC (UPenn/FNAL)
- 32-channel general purpose HPTDC (CERN)

The input connector: WR-40P-HF-HD (proposed by L. Jönsson, Lund)

The design of the FEC is (almost) the same as the design of the evaluation board.

Small footprint of the board allows TPC pads as small as 1x4 mm².

No clear mechanical interface to the LP TPC endplate exists (yet).

Advantage of the TDC-based readout electronics: low output data rate.

A single TPC hit is encoded into 32-bit word: Header & TDC ID (8 bit) Channel ID (5 bit) + <u>Width</u> (7 bit) + <u>Leading time</u> (12 bit)

+ Event header & trailer (2 words per event)

HPTDC offers parallel (word & byte-wise) readout and serial readout. Serial readout with programmable speed up to 80 MHz clock rate.

A *daisy-chained serial readout* is possible: 16 TDC chips (512 channels) can be readout via 2 LVDS links.

Independent data readout from every TDC.

- Simple FEC design. No token ring no interconnections between FECs.
- Increases number of required LVDS links/cables from the TPC.

Two possible solutions are currently under study:

- General purpose VME module CAEN v1495
- PCI FPGA Computing Card, an example from *Nallatech*:



BenIO[™]-V4 Virtex-4 Digital IO Module



BenOne[™]-PCI (with an analogue module BenADDA)

- PCI-express interface + USB/Ethernet optionally
- Standalone operation. PC is not necessary for data taking.

up to 76 differential pair IO lines (LVDS) An estimated power consumption of a single FEC is 2 W.

4 ASDQ ASICs, 40mW/channel: 1.28 W HPTDC (typical power consumption): 0.65 W

TDC-based readout electronics: ~ 60 mW/channel. The power consumption is similar to the ALICE TPC readout boards: ~54mW/channel.

Area occupied by 1600 readout channels (assuming 1x4 mm² pads) would have size of ~100 x 64 mm². Power dissipation: ~100 W.

It is relatively easy to implement air cooling, but it is not that effective as the water cooling, which is used for the ALICE TPC readout electronics.

The effect of the thermal influence of the FEC on the LP TPC performance shall be studied.

S.Popescu et al., "Thermal Influences of the Front-End Electronics on the Alice TPC Readout Chamber", IEEE Trans. Nucl. Sci. 52 (2005) 2879. The study of the TDC-based readout electronics for a GEM TPC is ongoing.

Readout electronics with larger number of channels (compared to smaller TPC readout systems) will be assembled for LP TPC.

The Front End Card is *still* based on existing components.

• An evaluation board will be used to study performance of the ASDQ and HPTDC chips(Spring 2007). Next step: *Front End Card.*

• First test will be done with mini-TPC(Spring 2007). Next step: *LP TPC.*

Some questions need to be answered:

- unified electrical interface (connectors)
- mechanical support of the TPC electronics
- cooling
- common data acquisition: TPC + Silicon telescope

Hope some of them could be addressed already during this meeting.