The design of the TimePix chip

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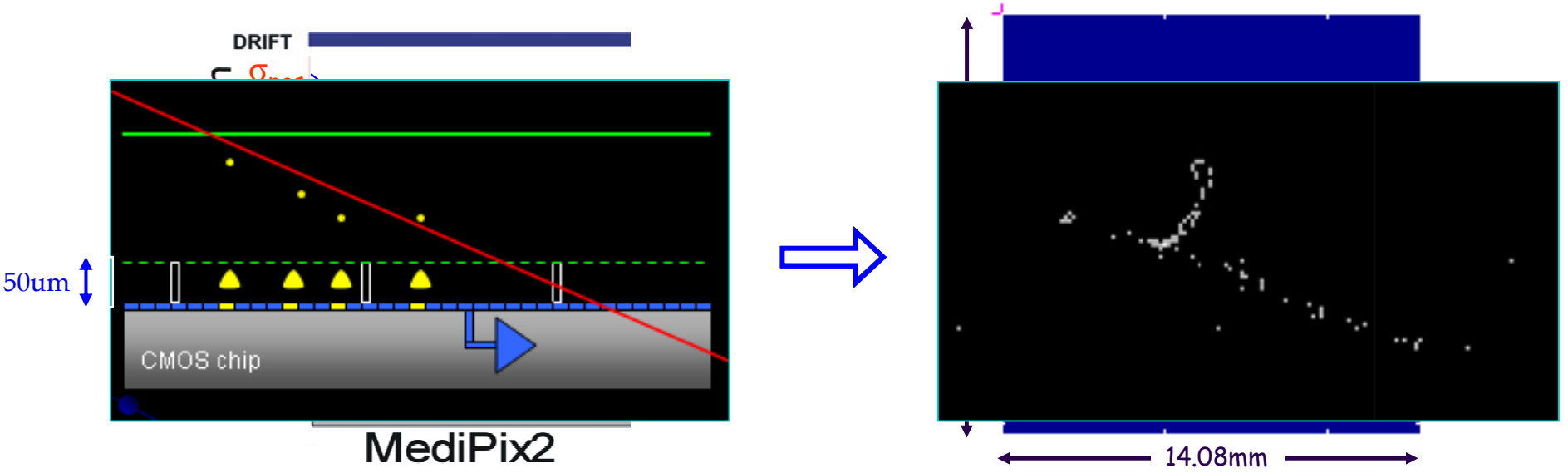
From Medipix to Timepix

- A novel approach for the readout of a TPC at the future linear collider is to use a CMOS pixel detector combined with some kind of gas gain grid
- Using a *naked* photon counting chip Medipix2 coupled to GEMs or Micromegas demonstrated the feasibility of such approach



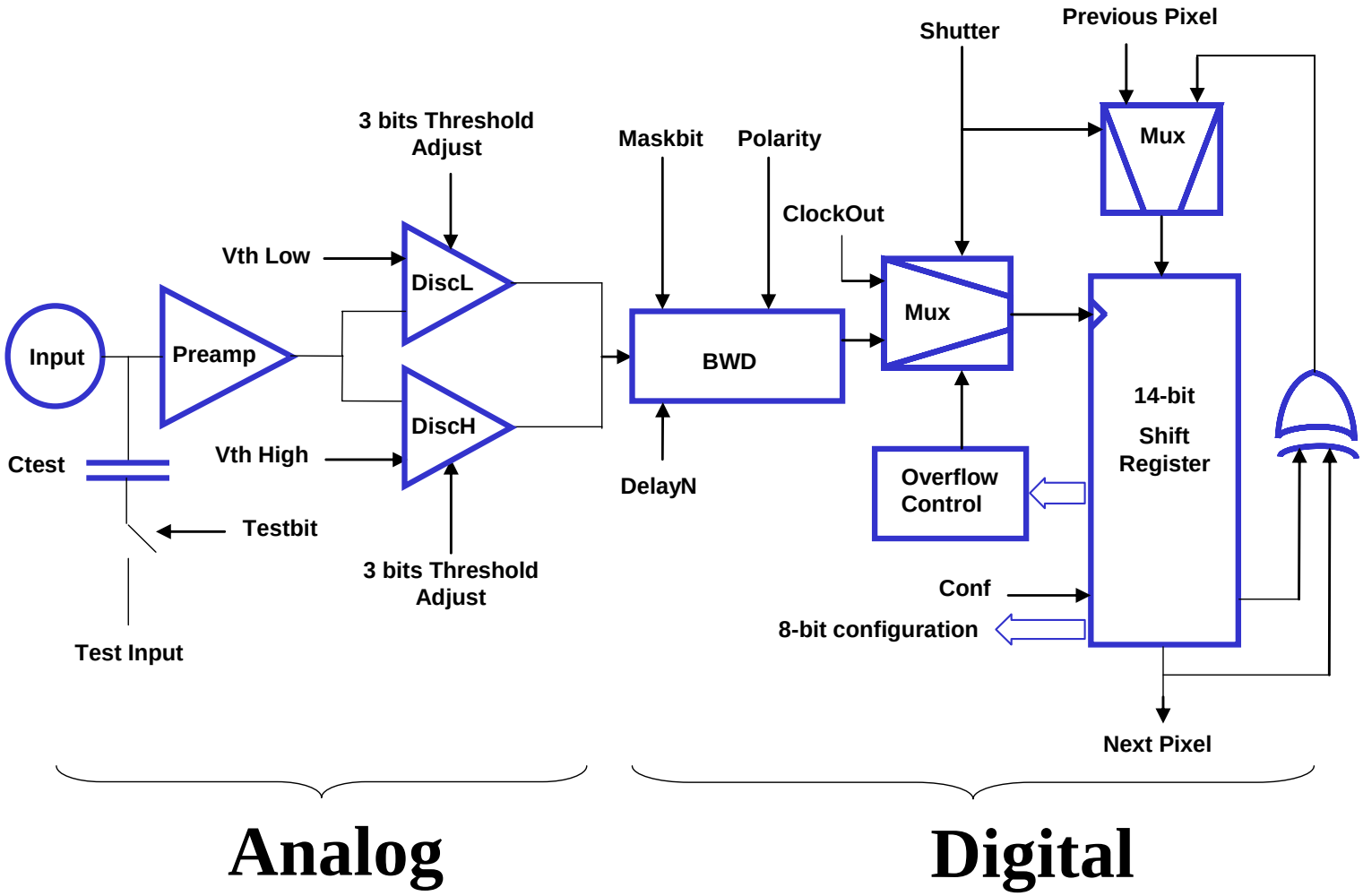
Motivation

- These experiments (by NIKHEF/Saclay, Freiburg 2004/2005) demonstrated that single electrons could be detected using a *naked* Medipix2 chip ⇒ 2D
- Did not provide information on the arrival time of the electron in the sensitive gas volume ⇒ 3D (position + time) !!!
- To further exploit this approach the Medipix2 is being redesigned to incorporate a time stamp with a tunable resolution of 100 to 10ns.
- Requirements:
  - Keep Timepix as similar as possible to Medipix2 in order to benefit from large prior effort in R/O hardware and software
  - Avoid major changes in pixel and/or readout logic – risk of chip failure due to poor mixed mode modelling
  - Eliminate 2nd threshold
  - Add possibility of programming pixel by pixel arrival time or TOT information
- This modification is supported by the JRA2/EUDET Collaboration (www.eudet.org)

Where we come from (Mpix2MXR20 Schematic)

Pixel Configuration Bits

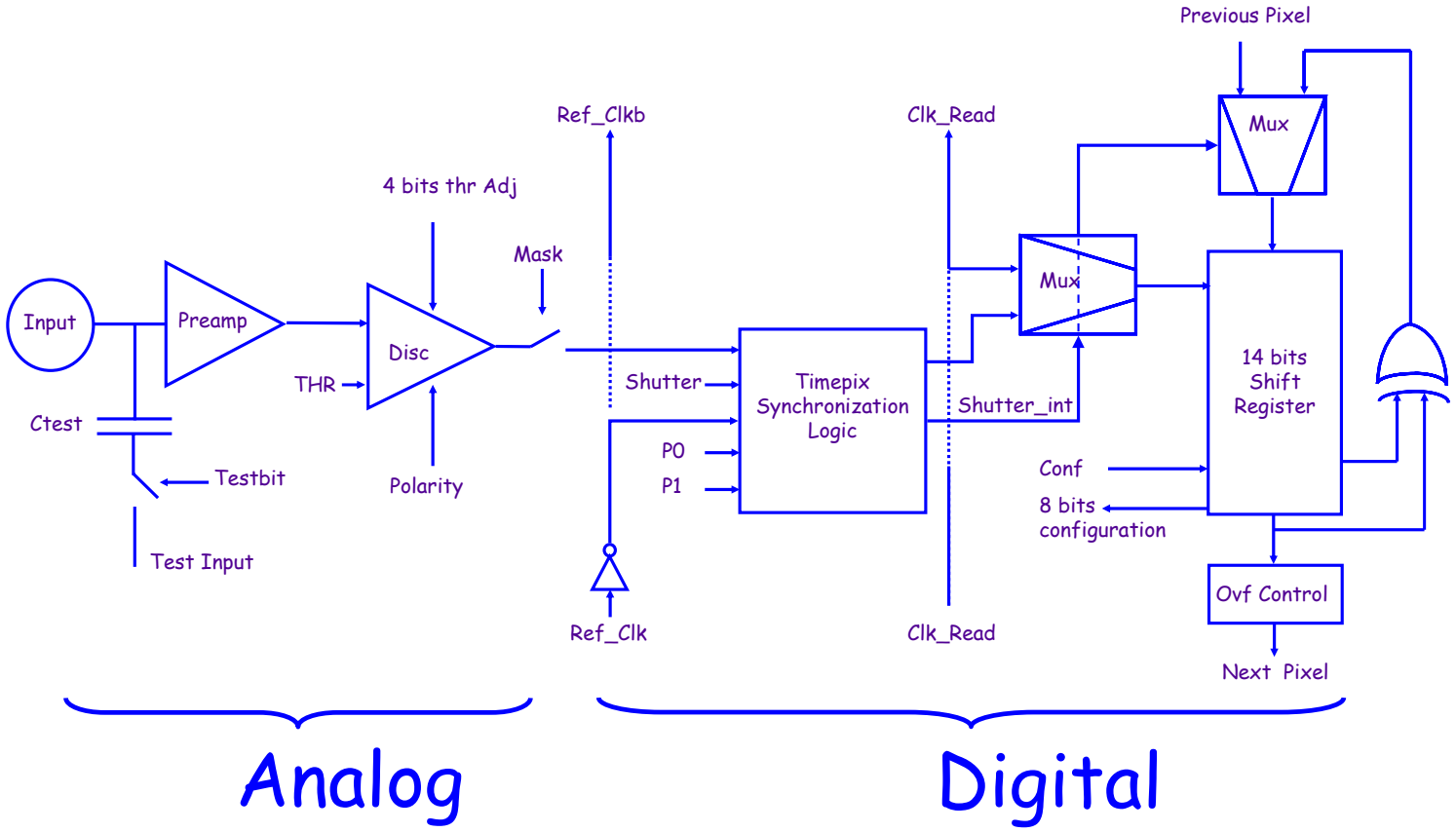
Maskbit	Masks pixel
TestBit	Enables TestPulse
BL0	Low Threshold – B0
BL1	Low Threshold – B1
BL2	Low Threshold – B2
BH0	High Threshold – B0
BH1	High Threshold – B1
BH2	High Threshold – B2



Where we go… (Timepix Schematic)

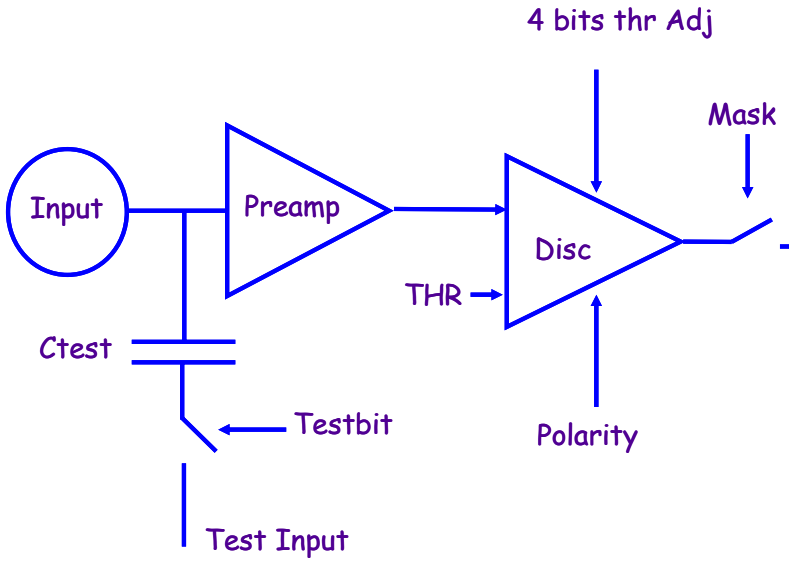
Pixel Configuration Bits

Maskbit	Masks pixel
TestBit	Enables TestPulse
BL0	Low Threshold – B0
BL1	Low Threshold – B1
BL2	Low Threshold – B2
BL3	Low Threshold – B3
P0	Mode Selection – P0
P1	Mode Selection – P1



Medipix → Timepix: Analog side changes

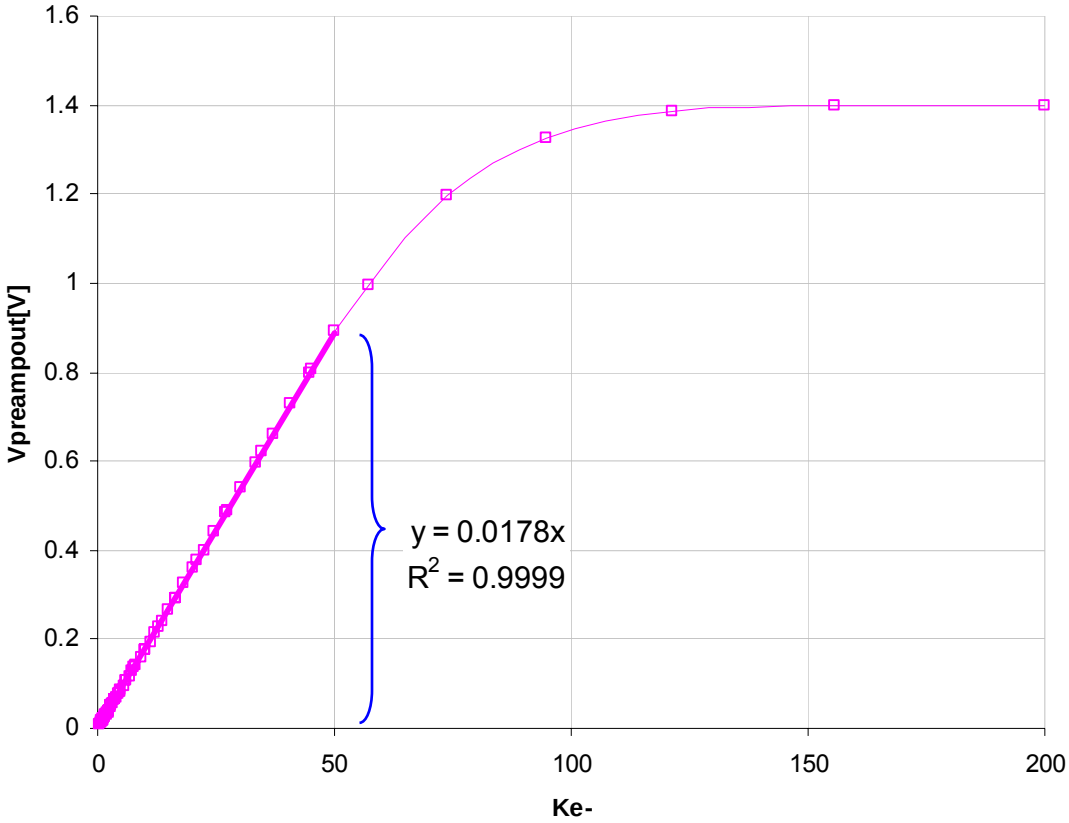
- Changes in Preamp:
  - Added cascode to preamp
- Changes in the discriminator:
  - Only 1 discriminator
  - 4-bit threshold equalization
  - Polarity control
  - Added hysteresis



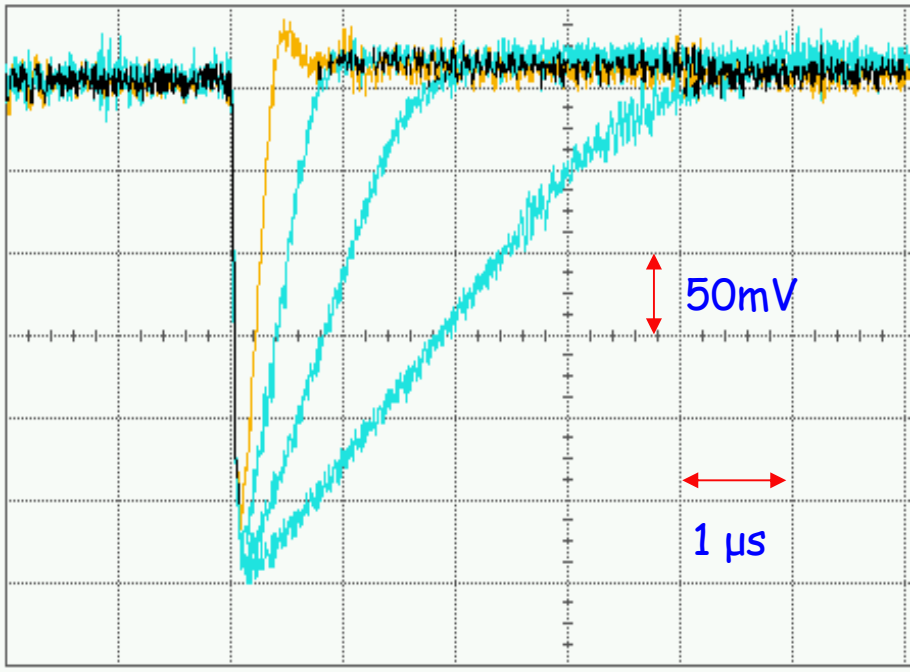
Analog

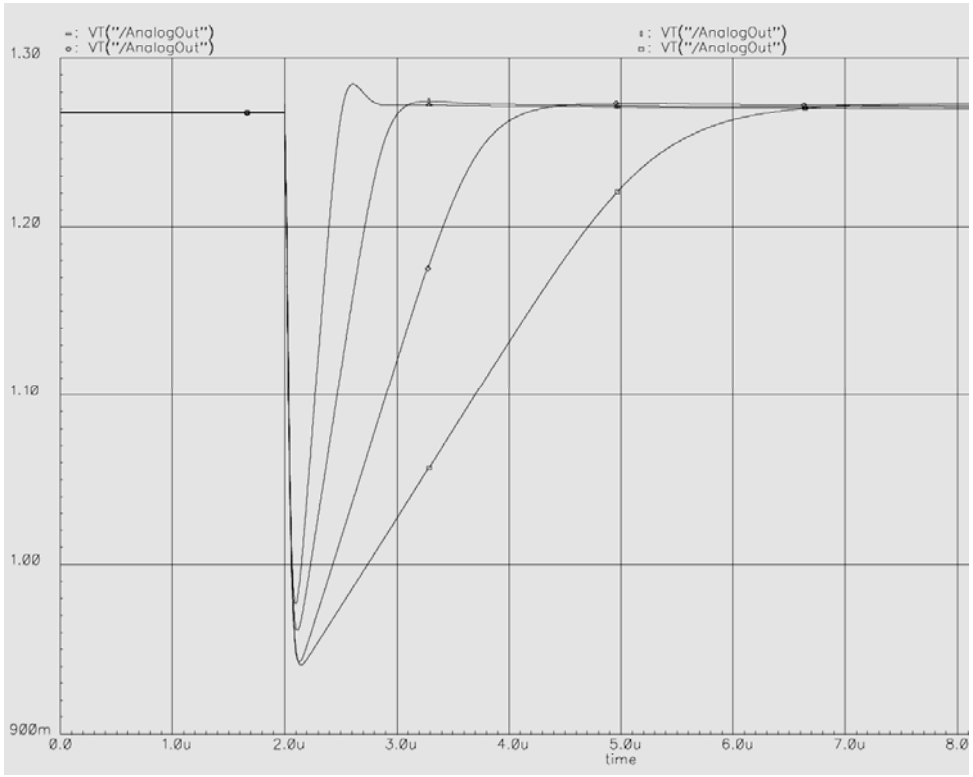
Medipix → Timepix: Preamplifier change

- Added cascode (8-bit DAC controlled):
  - Gain ↑ (~18mV/Ke$^-$) keeping V_{outrms} noise ≅ cte → SNR ↑
  - Expected ENC ≅ 75e$^-$
  - Expected Linearity: 0.6 to 1.5 Volts → ≅50Ke$^-$ linear range
  - Expected Missmatch: σ_{vt} ≅ 2.11mV → σ_{vt} ≅ 117e$^-$



Medipix → Timepix: Preamp Out vs Ikrum DAC



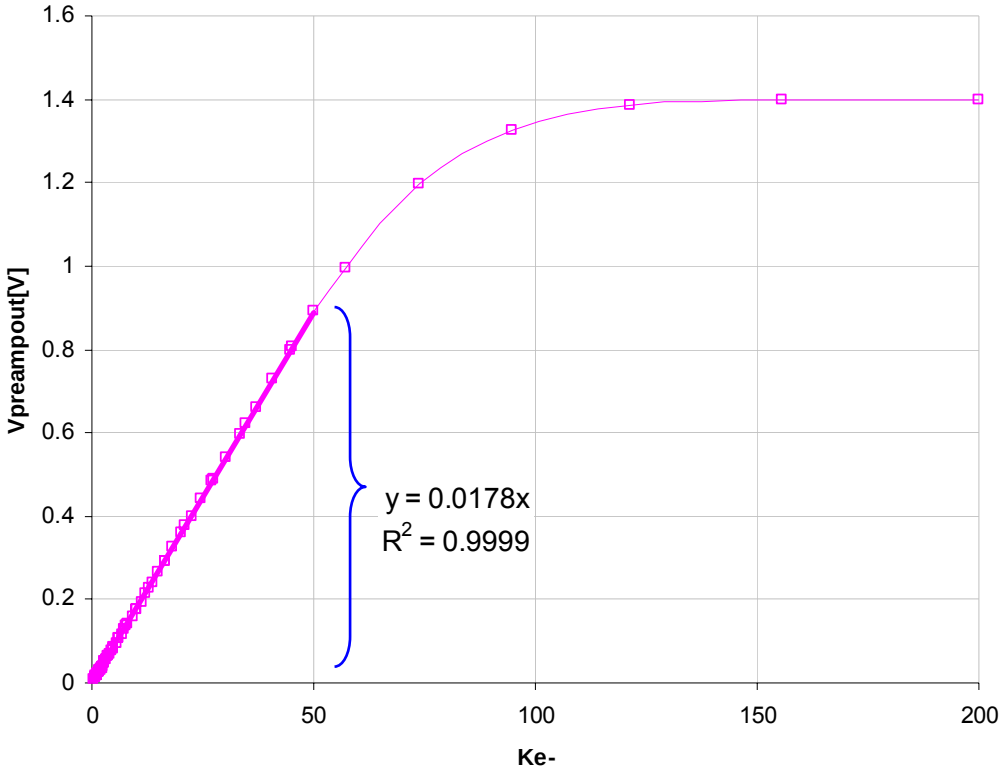


- 18.75 Ke input charge
- Ikrum DAC set: 5, 10, 20 and 40
- Direct measurement on the Timepix test output pads

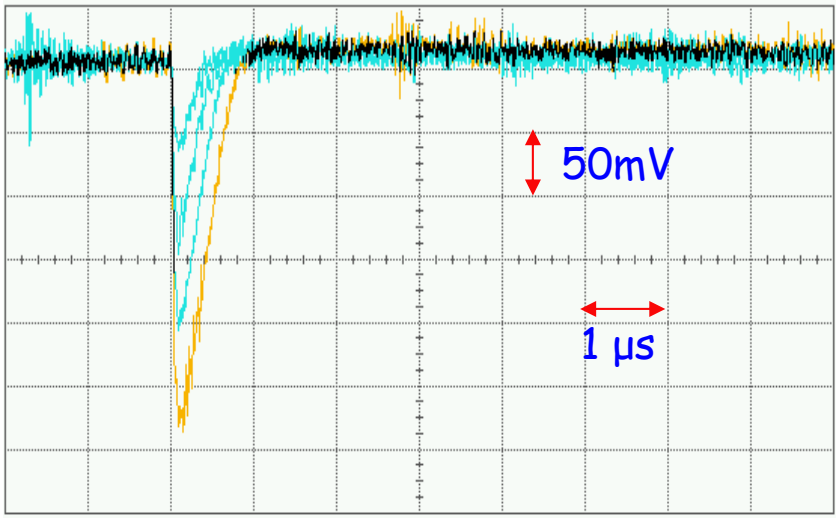
- 18.75 Ke input charge
- Ikrum current set: 1.7, 3.4, 6.8, 13.6 nA

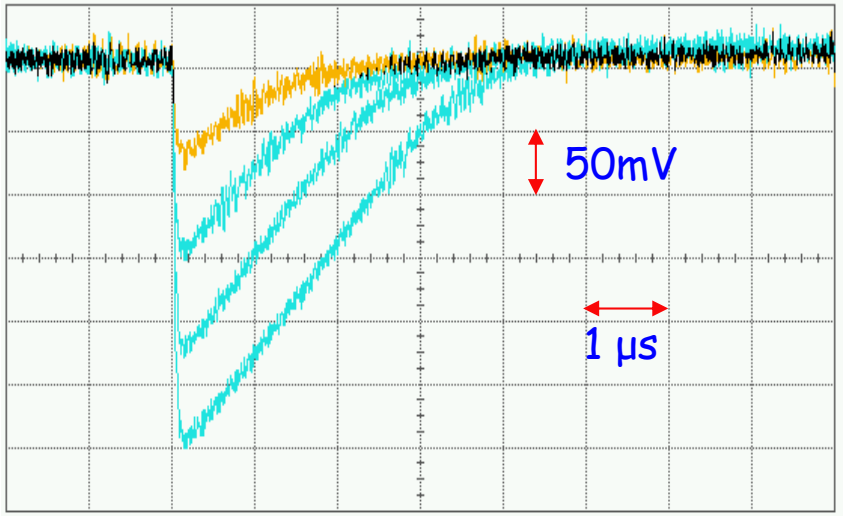
Medipix → Timepix: Gain Linearity

- Expected gain linearity up to ~50Ke⁻
- >50Ke⁻ the Preamp output saturates



Simulation

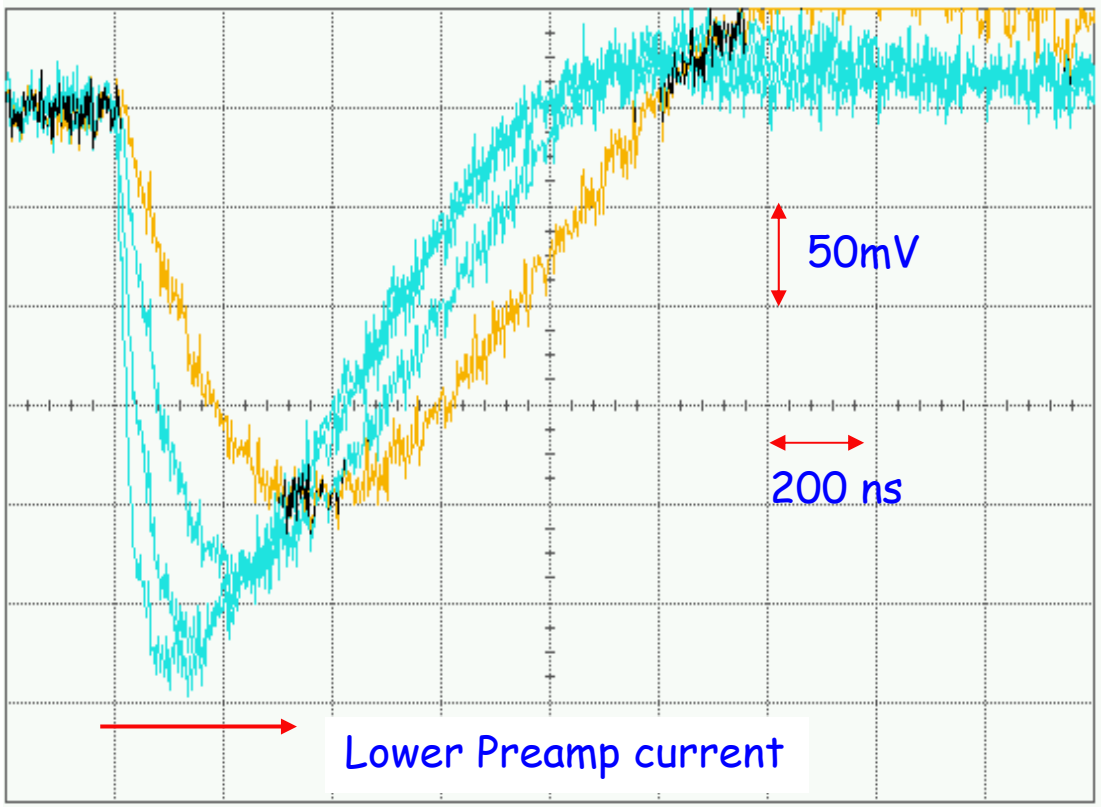




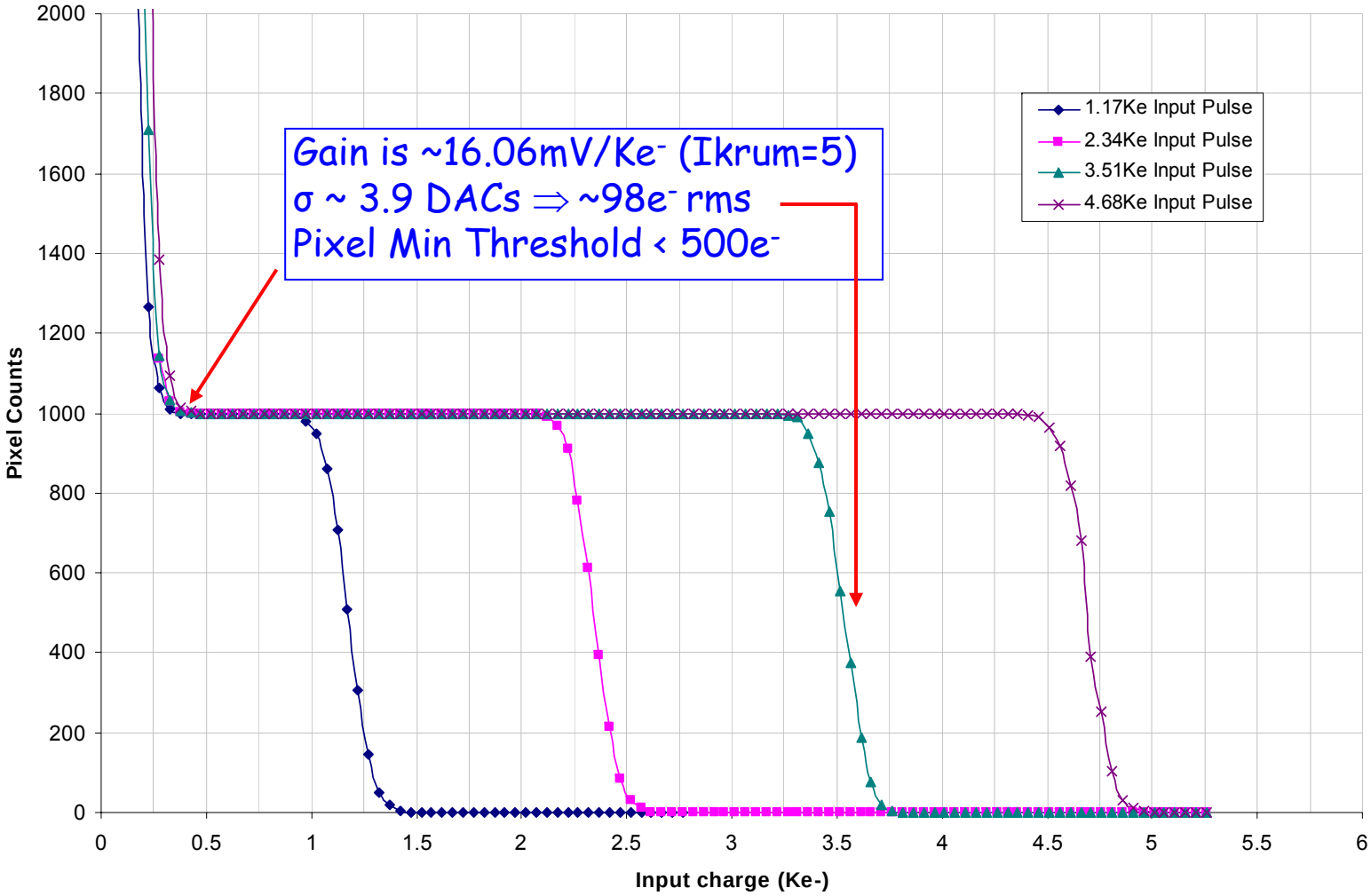
Measurement: ΔQin and ΔIkrum

Medipix → Timepix: Preamp Out vs Preamp DAC

- Gain (ENC noise) depends on the preamp current
- Tunable peaking time: ~90ns to 400ns → check Time-walk!

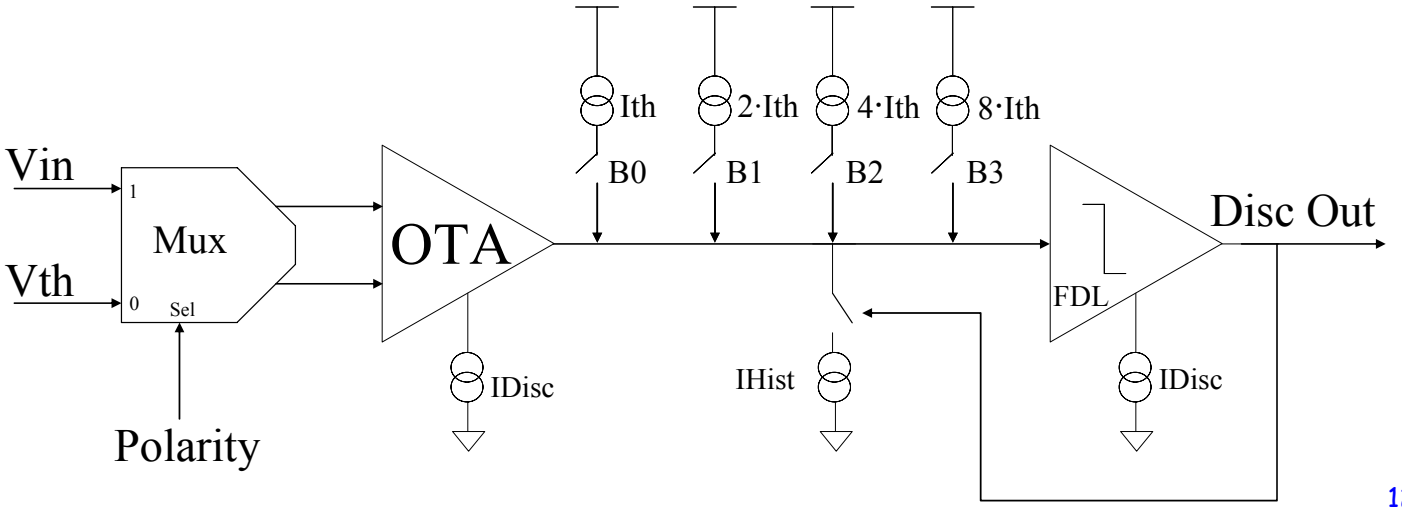


TestPulse on 1 pixel (Medipix Mode) Ikrum=5

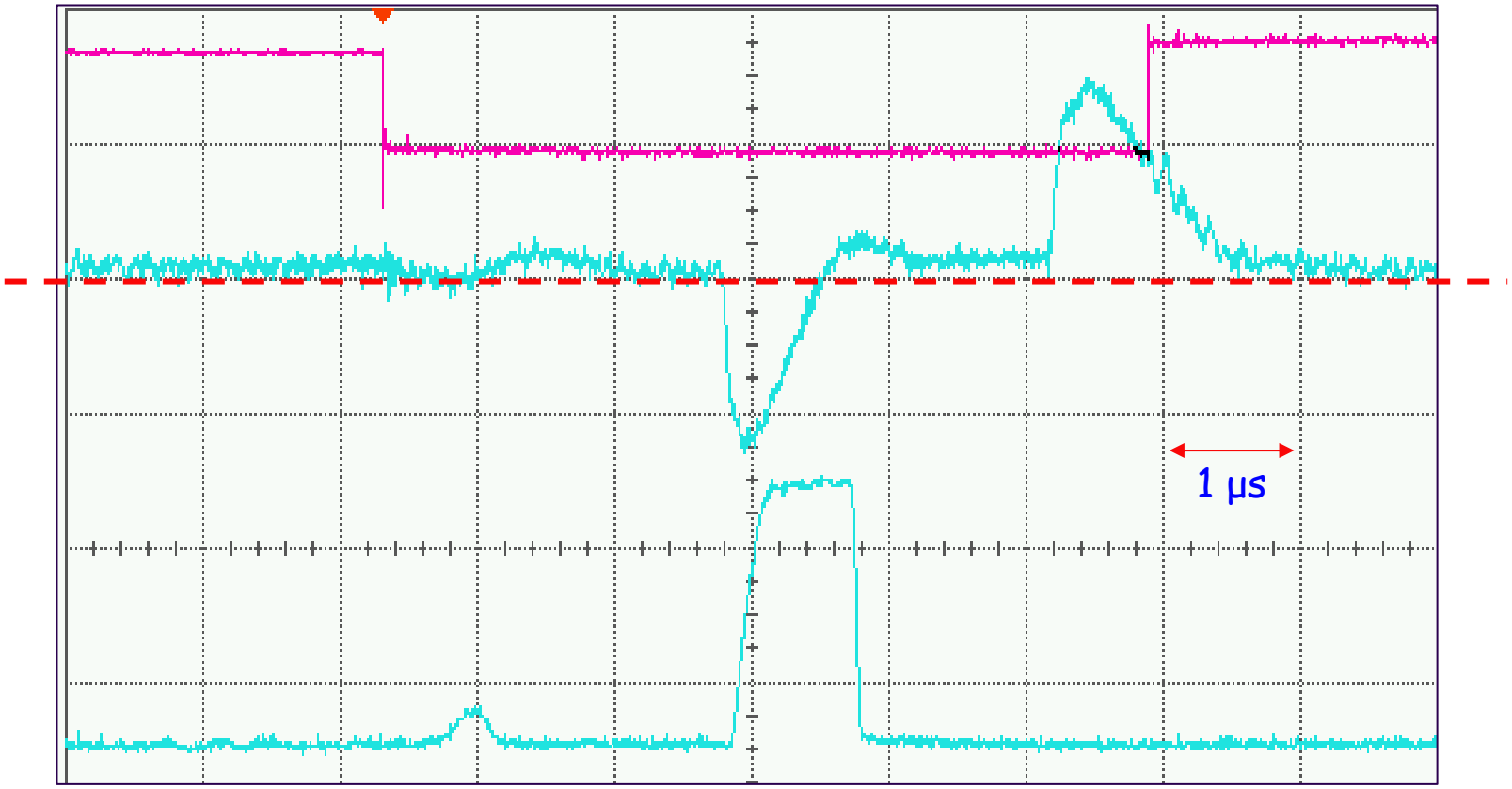


Medipix → Timepix: Discriminator changes

- Added hysteresis (8-bit DAC controlled) in discriminator:
  - ~200e⁻ lower threshold and no glitches at the disc output
  - It can be turned off
- Polarity selection on the discriminator:
  - Hysteresis possible
  - Optimization of the zero crossing design
- 4-bit threshold adjustment:
  - Expected Threshold dispersion after adjustment ~25e⁻

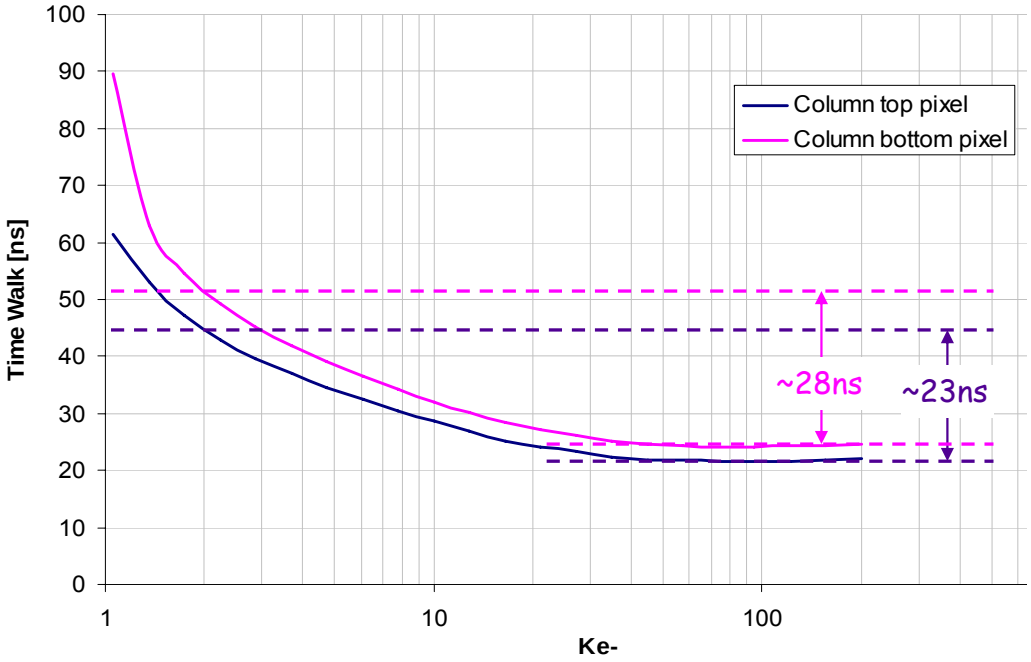


Medipix → Timepix: Discriminator Output

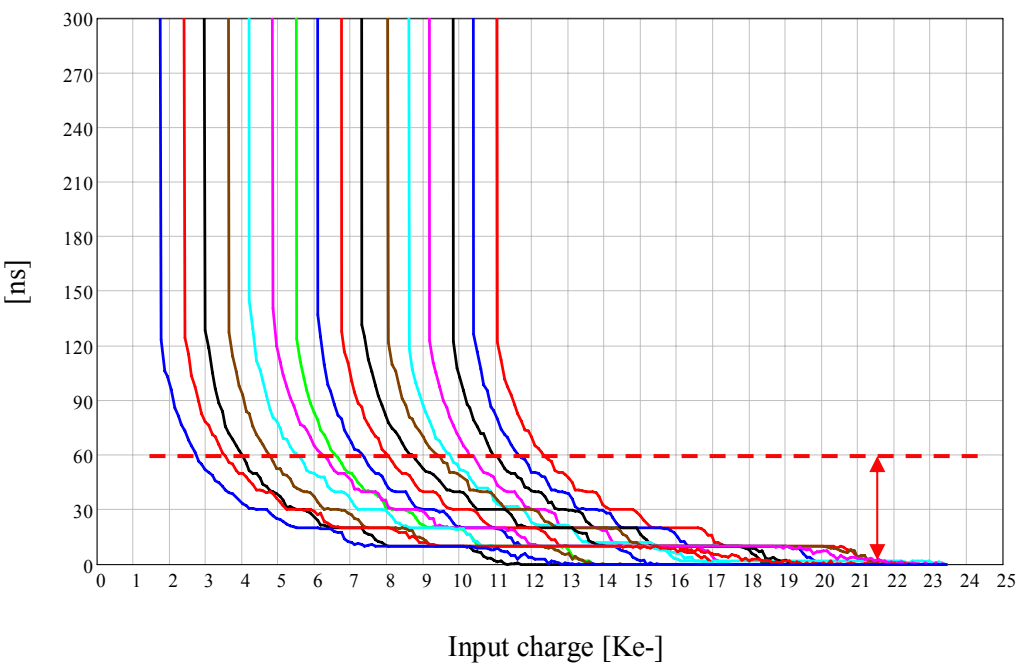


Medipix → Timepix: Time walk Simulation-Measurement

- Measured timewalk with the default DAC values
- Possible offline correction combined with TOT measurement can bring timewalk < Ref_Clk period

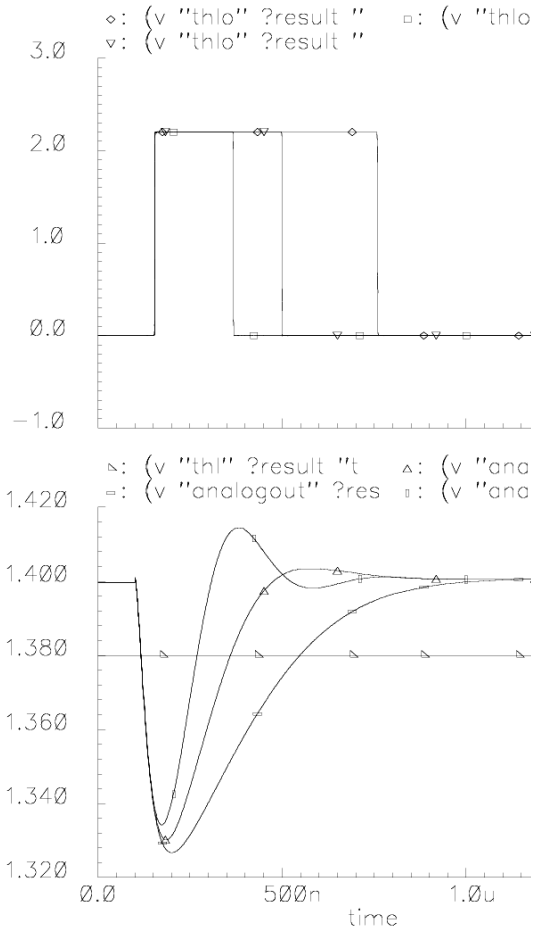


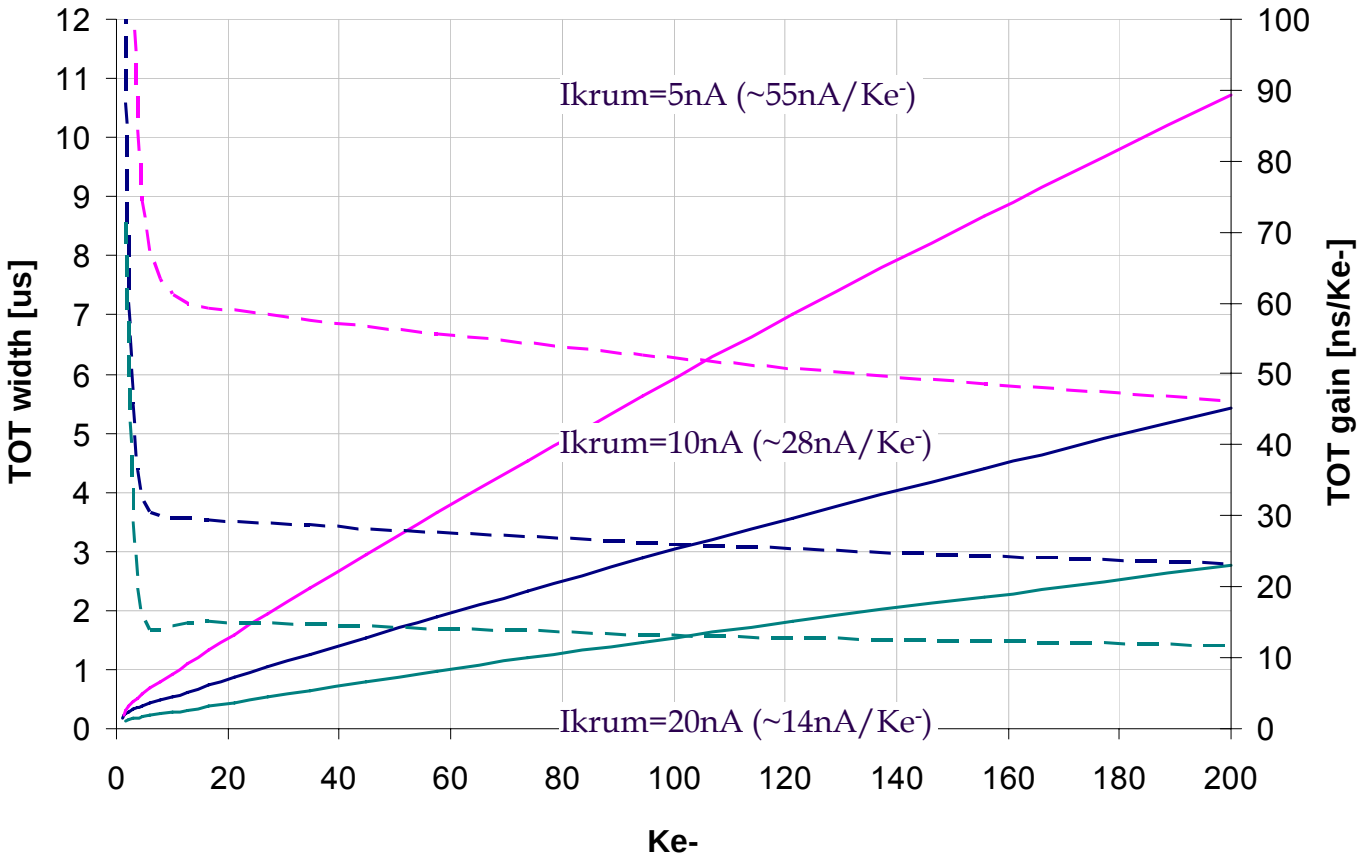
Simulation



Measurement: ΔThr

Medipix → Timepix: TOT vs Ikrum (simulation)

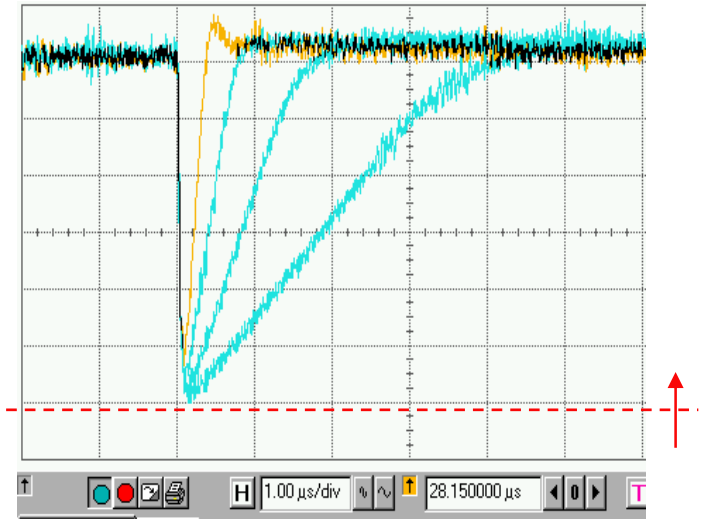


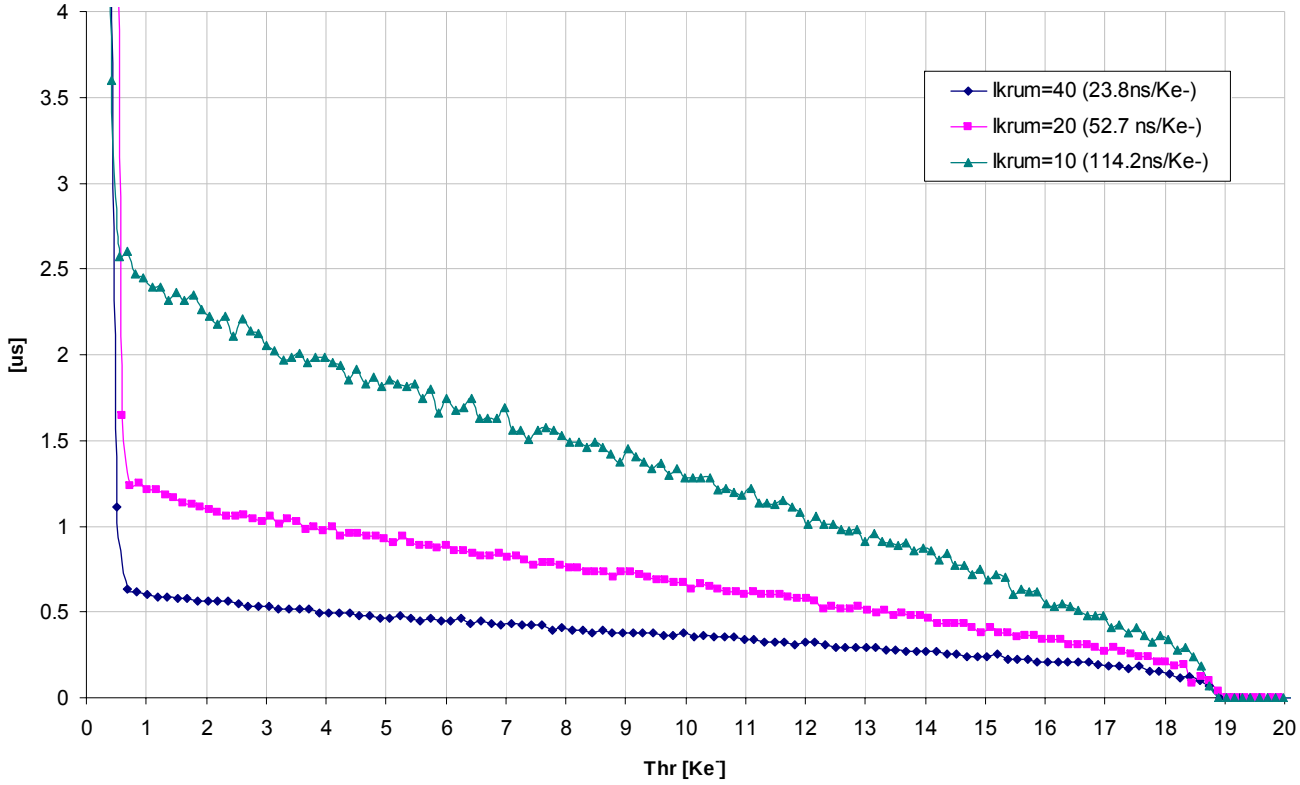


- TOT Linearity > 200 Ke-

Medipix → Timepix: TOT vs Ikrum (measurement)

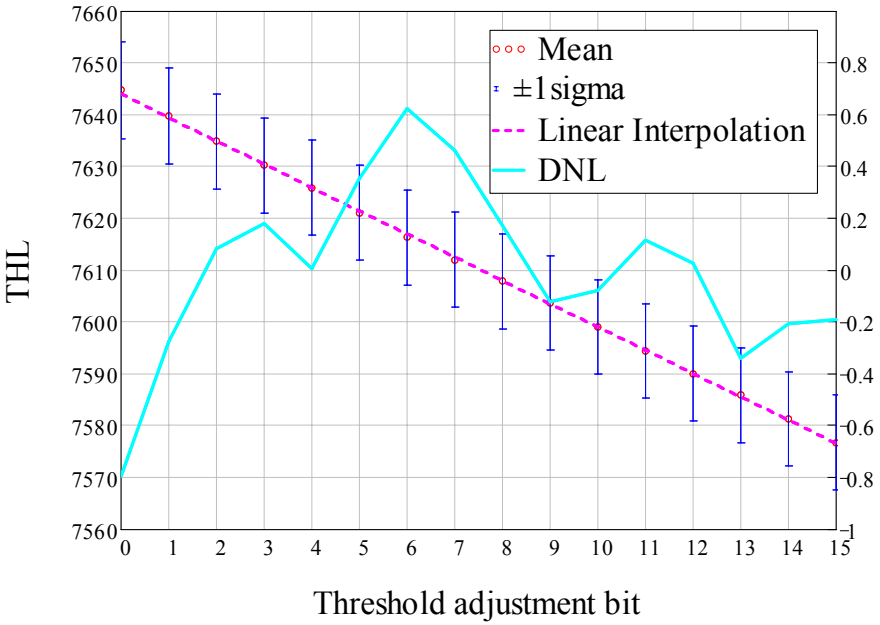
- TOT gain is a function of Ikrum DAC setting
- Ref_Clk=71.1MHz

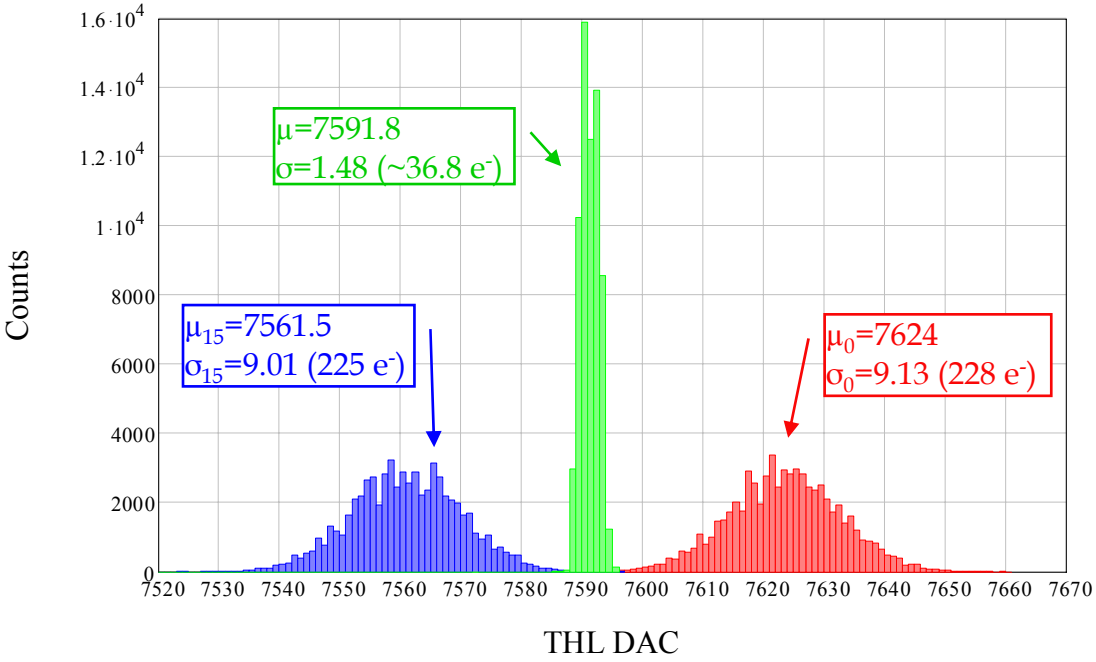




Timepix equalization (I)

- Equalization using the noise as trigger and Medipix Mode (P0=P1=0)
- The measured DNL of the 4-bit DAC is < 1THL DAC -> Interpolation in the equalization can be used





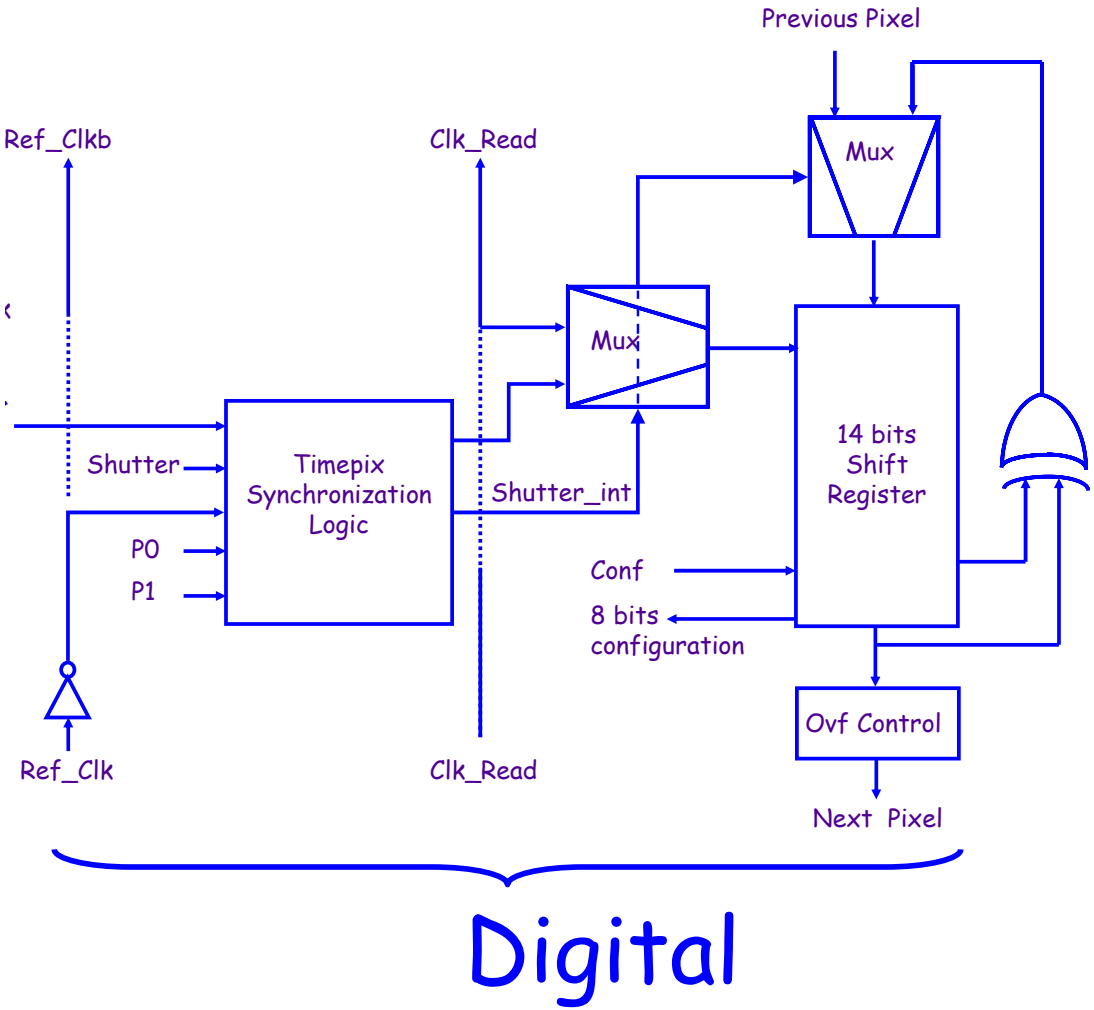
Analog pixel summary

	Simulated	Measured
Amplifier Gain	~18mV/Ke$^-$	~16.06mV/Ke$^-$
Peaking Time (Δ Preamp)	90ns…400ns	90ns…400ns
Pixel noise	~75e$^-_{rms}$	~98e$^-_{rms}$
Threshold dispersion	~170e$^-$	~225e$^-$
Adjusted Threshold dispersion	~25e$^-$	~38e$^-$ (not optimized)
Voltage linear range	0 to 50 Ke$^-$ (< 2%)	Measured up to 20Ke$^-$
TOT linear range	>200Ke$^-$	Measured up to 50Ke$^-$
Time Walk	~25ns (2Qth to ∞)	~60ns (with default DACs)
TOTgain	~55ns/Ke$^-$ (Ikrum=5nA)	52.7ns/Ke$^-$ (Ikrum$_{DAC}$=20)
Analog Pixel consumption (Max)	2.9μA x 2.2V = 6.38 μW (30% less than Mpix2MXR20)	

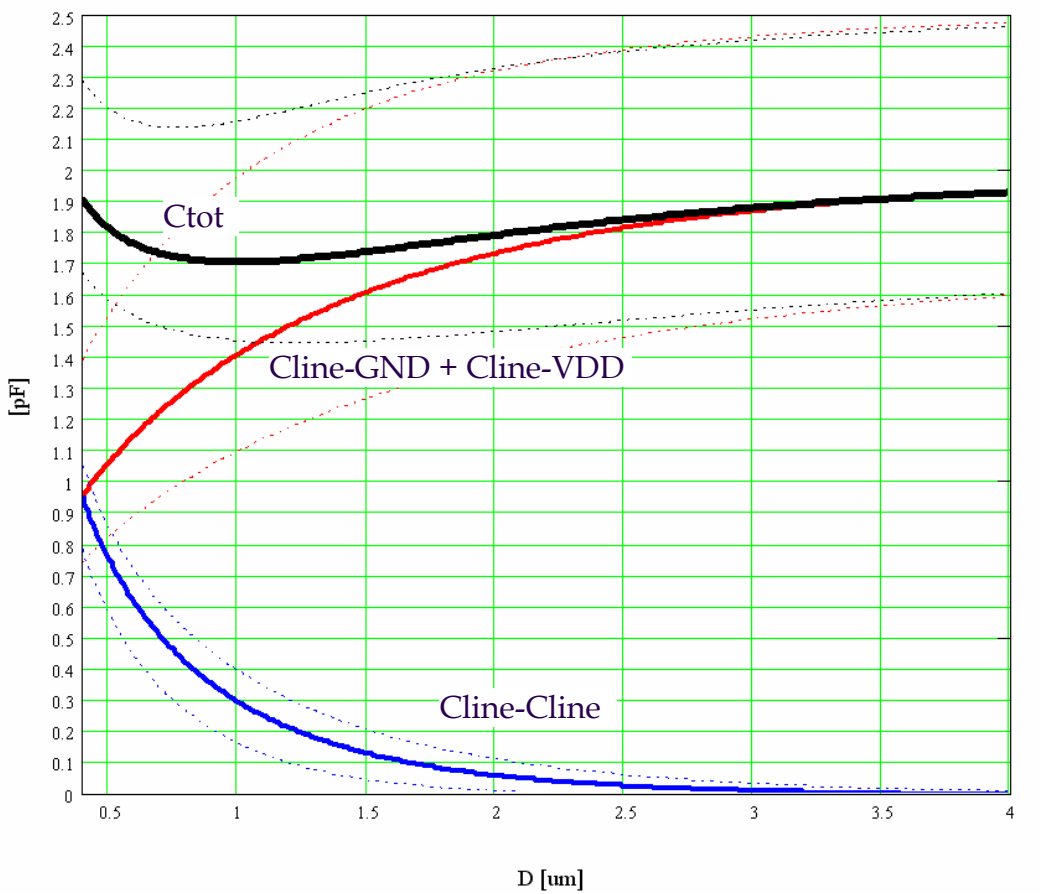
- Maximum possible Qin injected via Testpulse is ~50Ke$^-$

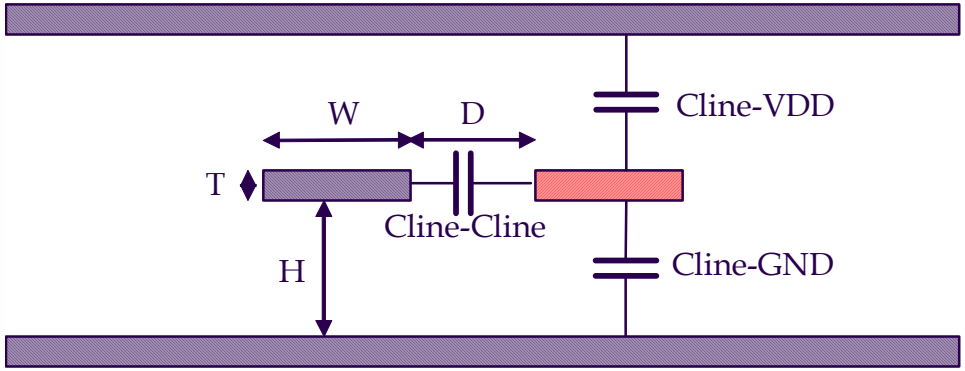
Medipix → Timepix: Digital side changes

- Added time reference (Ref_Clk)
- Selectable operation modes (P0 and P1)
- TSL (Timepix synchronization Logic)
- Pixel-by-pixel synchronized Shutter



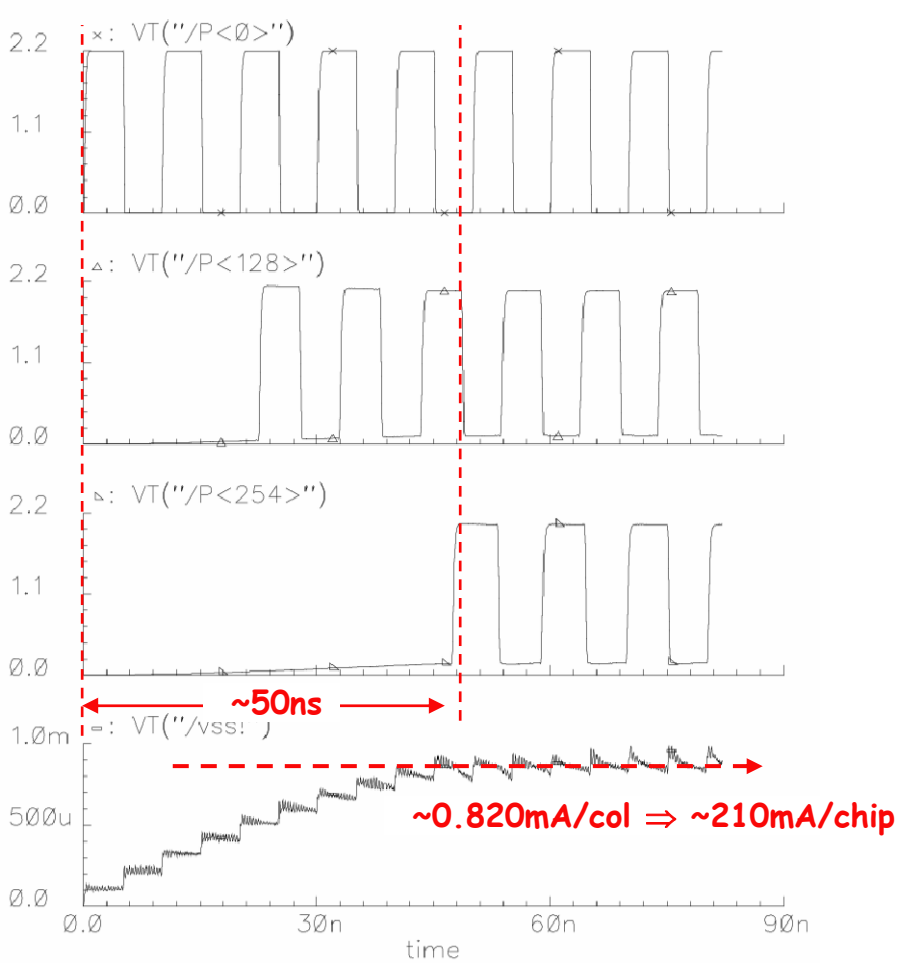
Medipix → Timepix: Added Time reference (I)





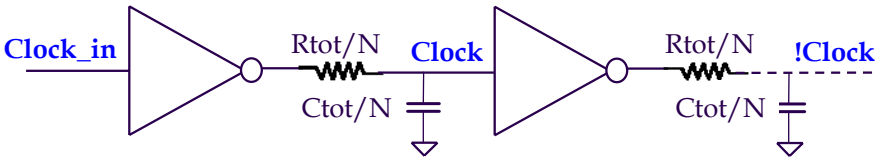
- Column length= 55x256= 14080µm
- W=0.4µm, T=0.54µm, H=0.8µm
- R≅2.8KΩ
- Ctot<=2pF
- Parasitic cap negligible at D>3 µm

Medipix → Timepix: Added Time reference (II)



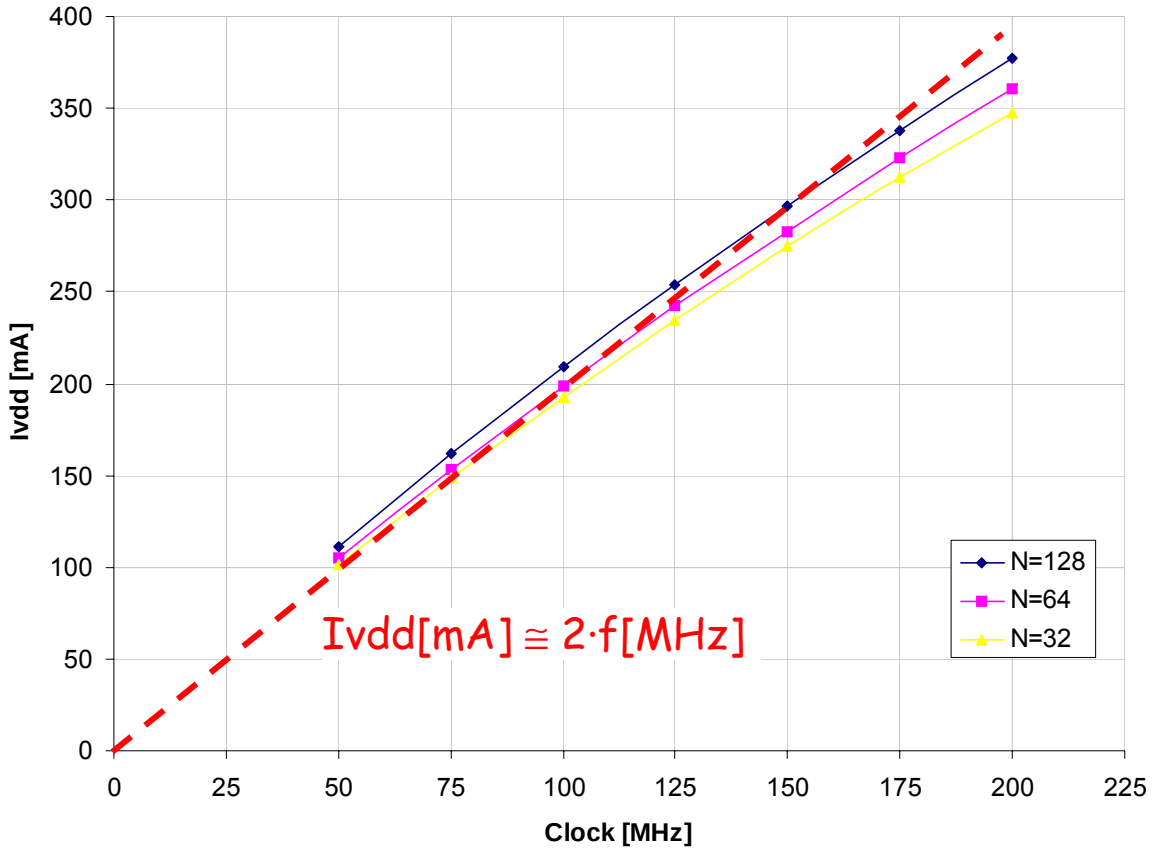
N buffer per column:

- Min size buffer ⇒ inverter per pixel
- No differential signals needed
- Power uniformly distributed over clock period



- N=256, f=100MHz
- Propagation delay = ~50ns (~195ps/inv)
- Simulation takes care of parasitic capacitances and top-down resistive power lines.

Medipix → Timepix: Expected digital power dissipation



- $Pvdd = V^2 \cdot f \cdot Ctot$
- Simulation @ Vdd=2.2V but digital part could work to 1.8V (33% less power)

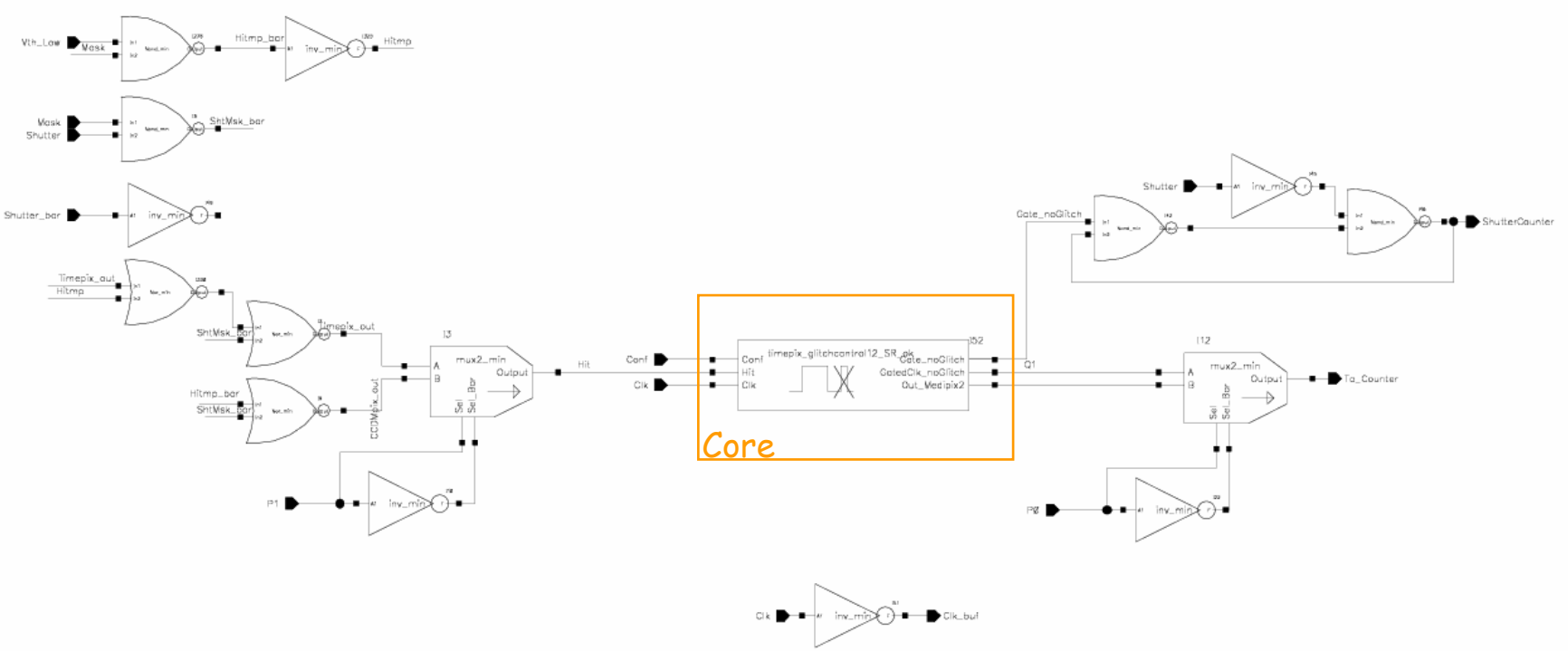
Medipix → Timepix: TSL

- Use of 3-bit High threshold adjustment bits for : 4th equalization bit and P0, P1.
- Each pixel can be configured independently in 5 different modes.
- This logic needs 128 Trts (Mpix2MXR20 had 92 Trts)

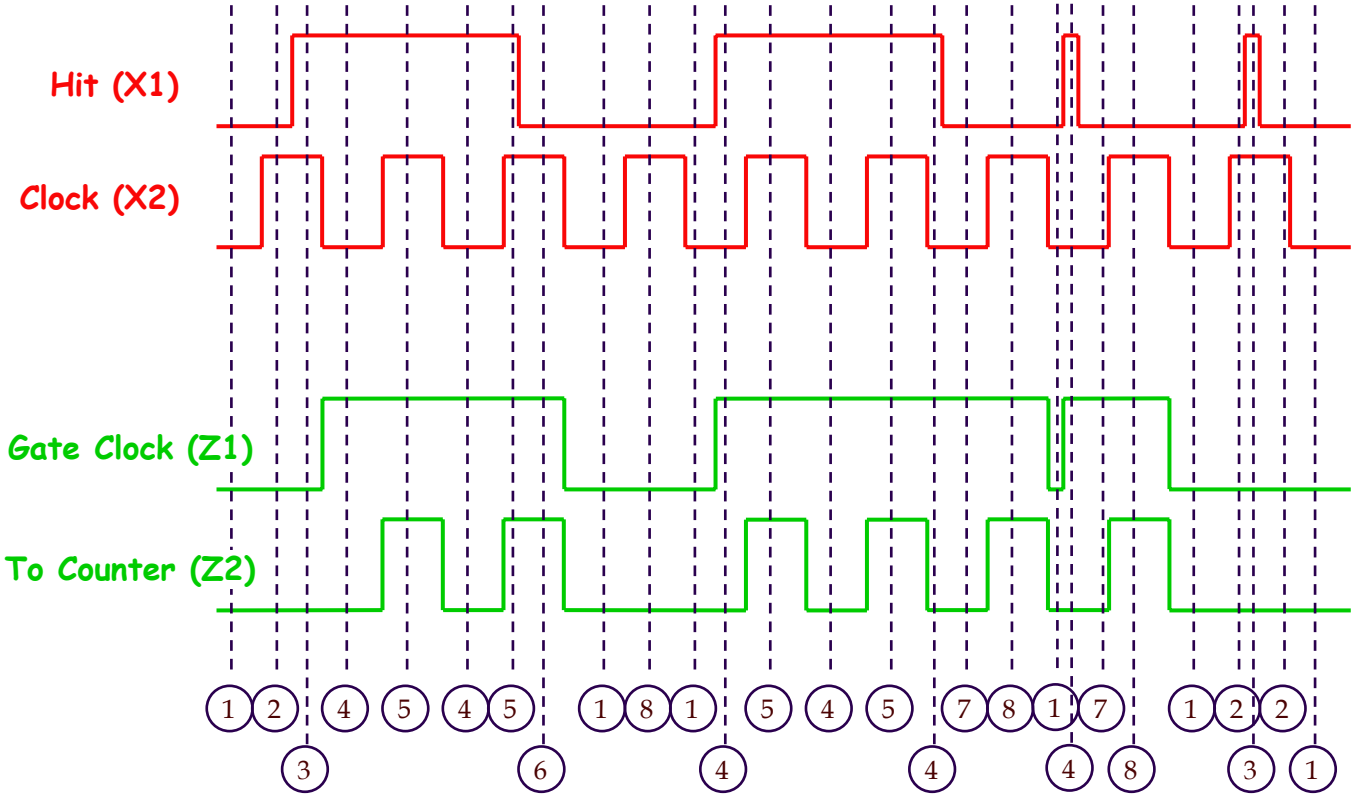
Mask	P1	P0	Mode
0	0	0	Masked
0	0	1	Masked
0	1	0	Masked
0	1	1	Masked
1	0	0	Medipix
1	0	1	TOT
1	1	0	Timepix-1hit
1	1	1	Timepix

Timepix Synchronization Logic (TSL)

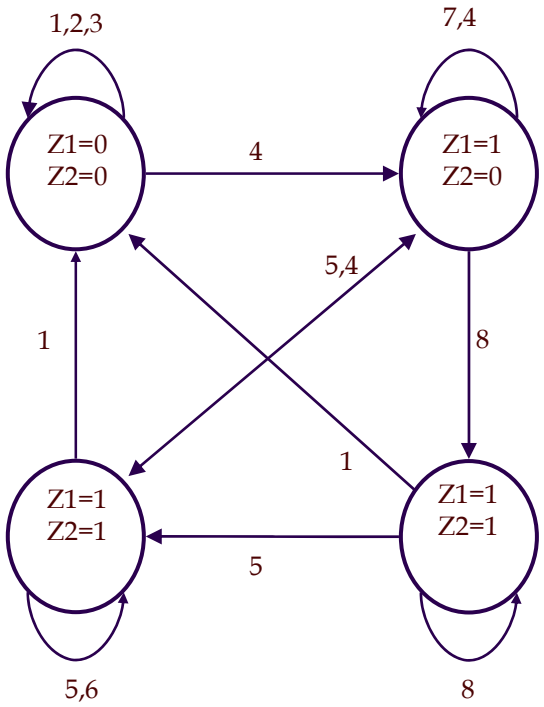
- *Hit* is synchronized with *Ref_Clk* and *Shutter* generating the signal to the counter and internal Shutter depending on P0, P1 and Mask bits.
- Power consumption only when *Hit* is present
- TSL Core is divided in 2 blocks: Core1 used for the Timepix and TOT modes and Core2 used for Medipix mode.
- Core blocks have being designed using an asynchronous network with S-R Flip-flops with race-free state assignment



TSL Core1 Asynchronous design

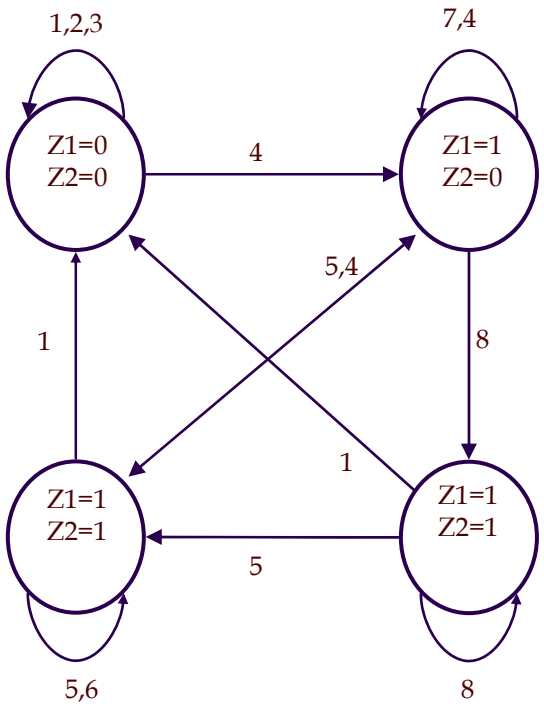


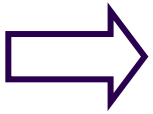
- TSL desired time diagrams

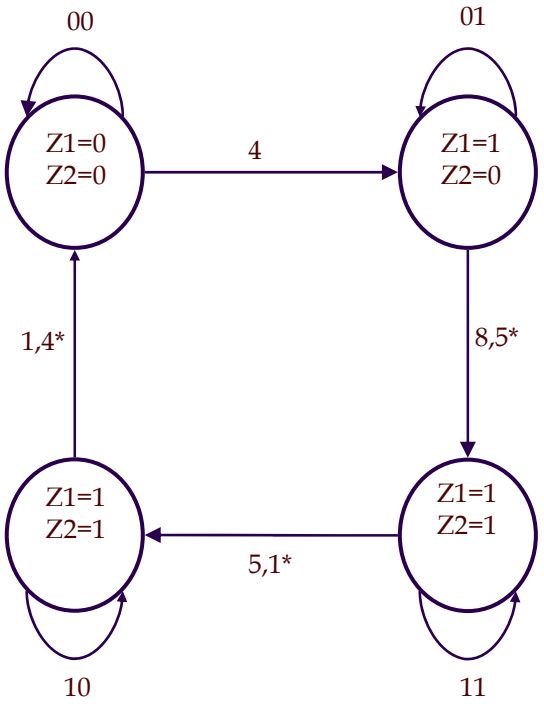


- State diagram

TSL Core Asynchronous design (II)

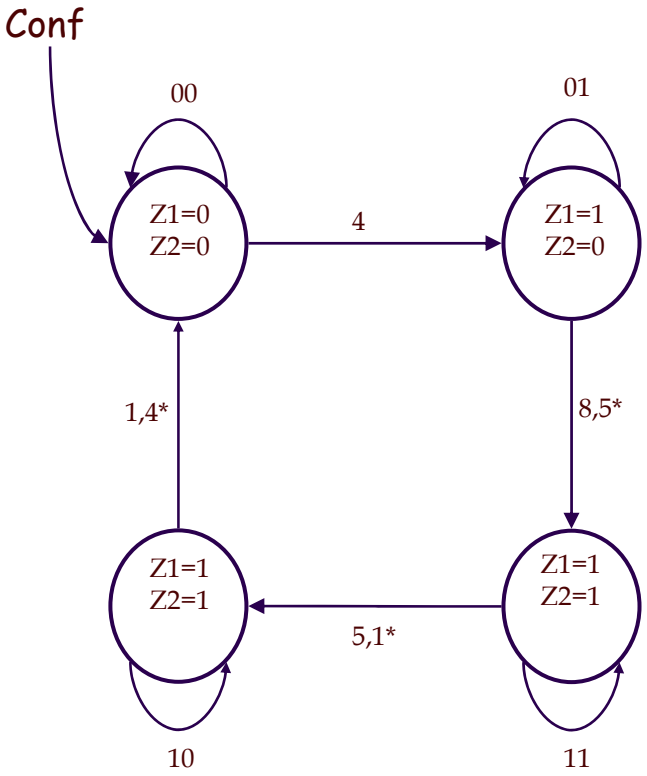




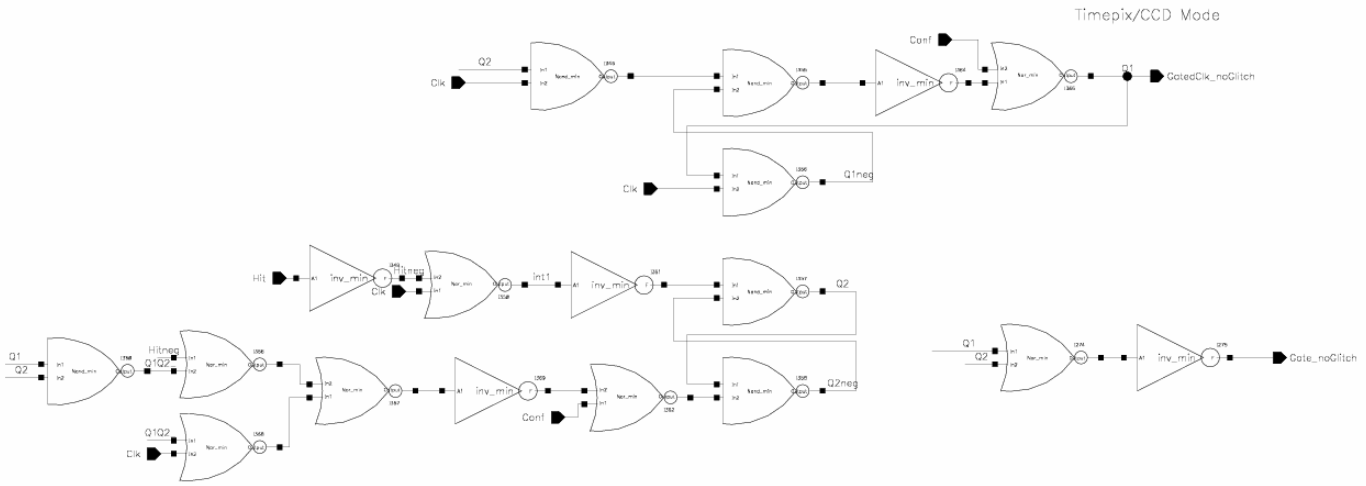


- State diagram
- Reduced State diagram

TSL Core Asynchronous design (III)

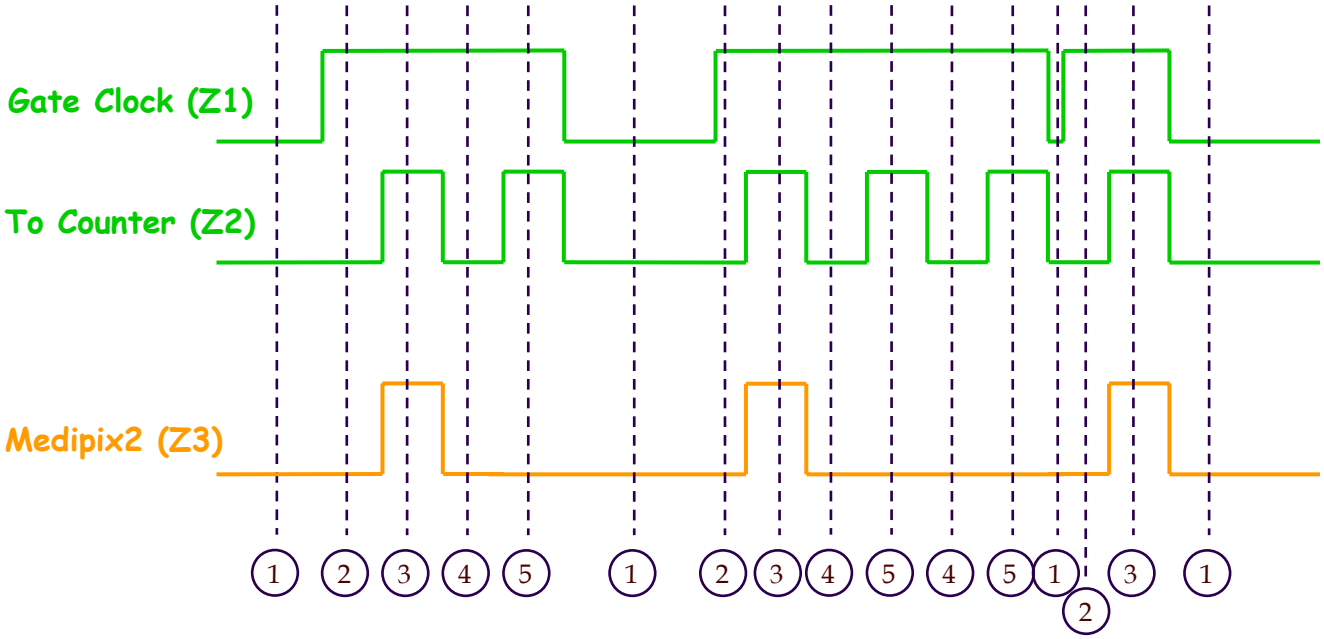


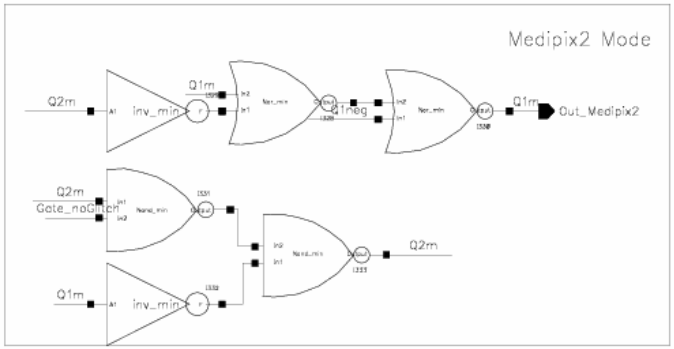
- Reduced State diagram with initialization



- Implementation with SR flip-flops (62 trts)

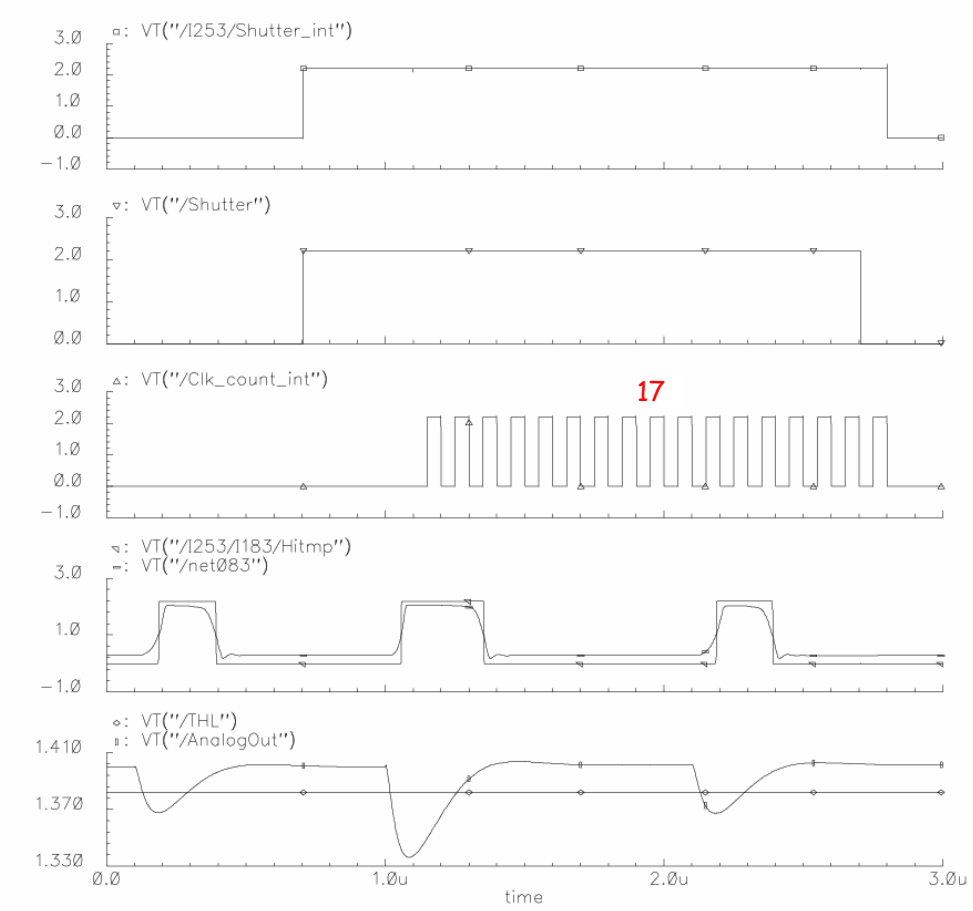
TSL Core2 Asynchronous design



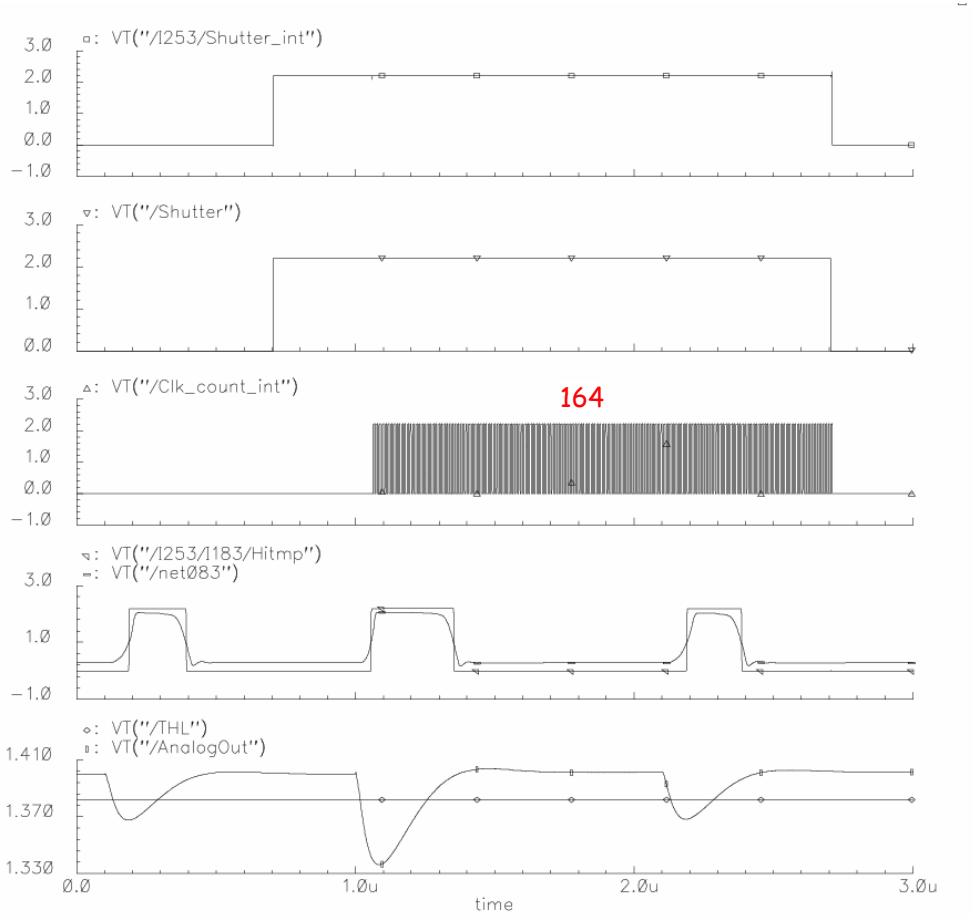


- TSL desired time diagrams
- Implementation using gates (20 trts) since inputs are race-free "by design"

Timepix Mode (P0=1,P1=1)

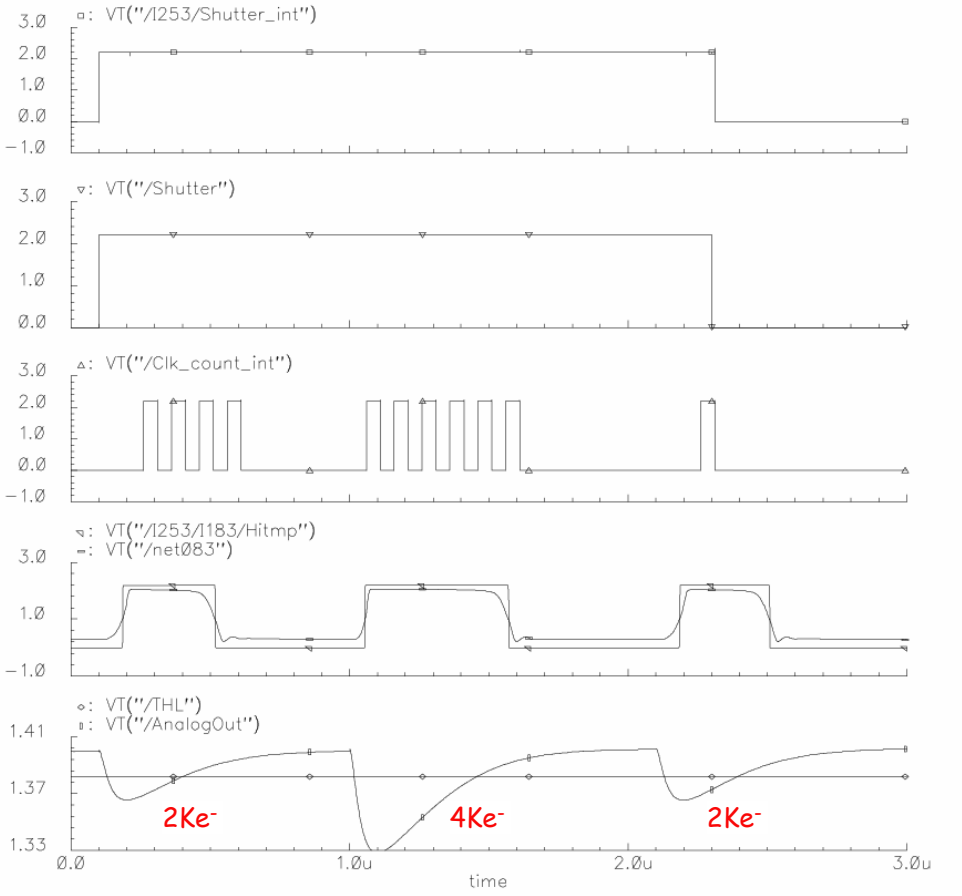


10MHz

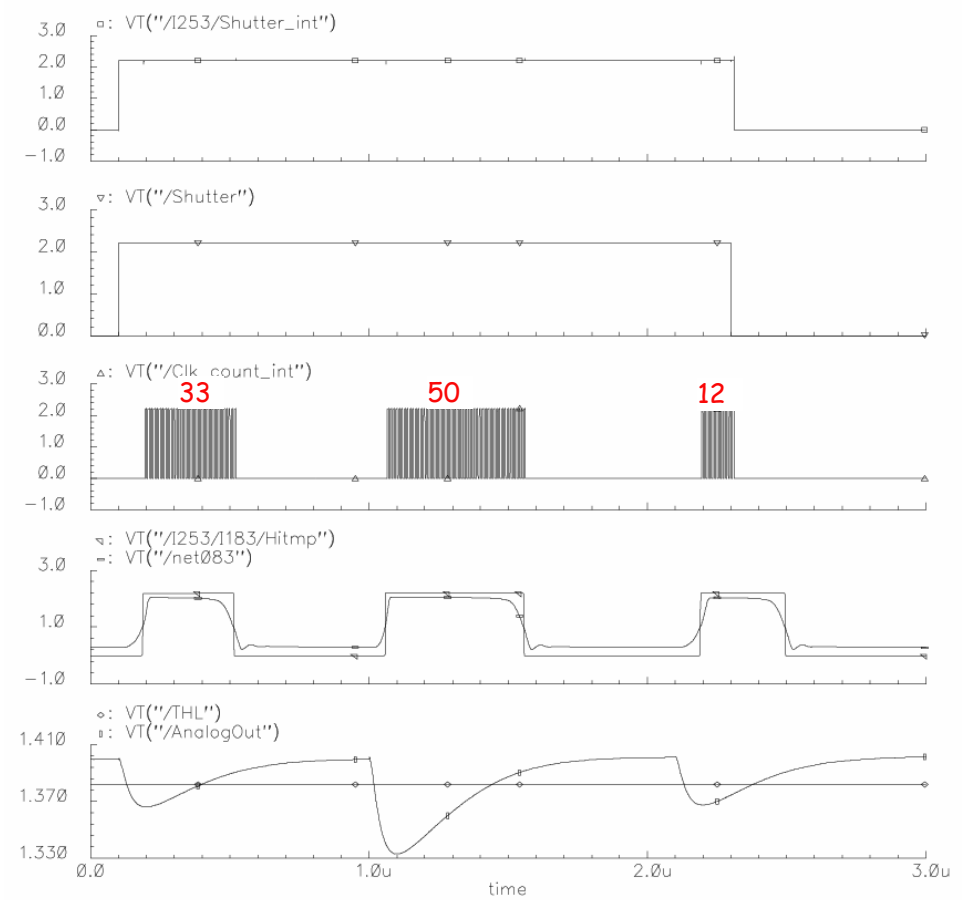


100MHz

TOT Mode (P0=1,P1=0)

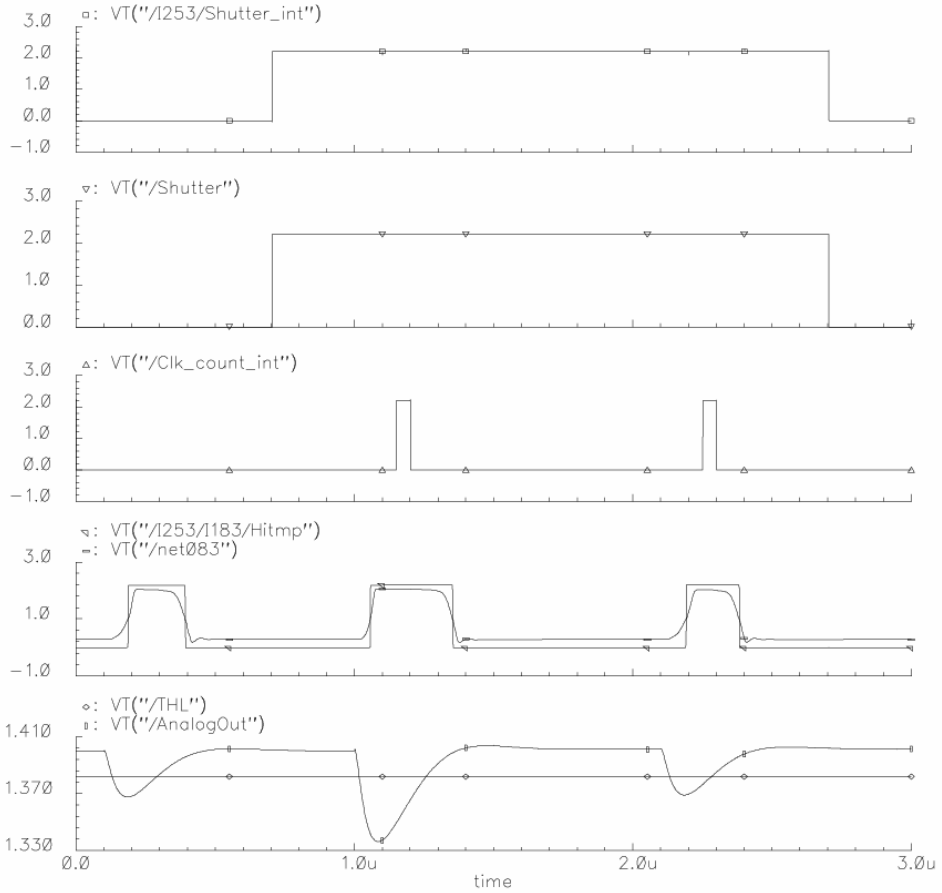


10MHz

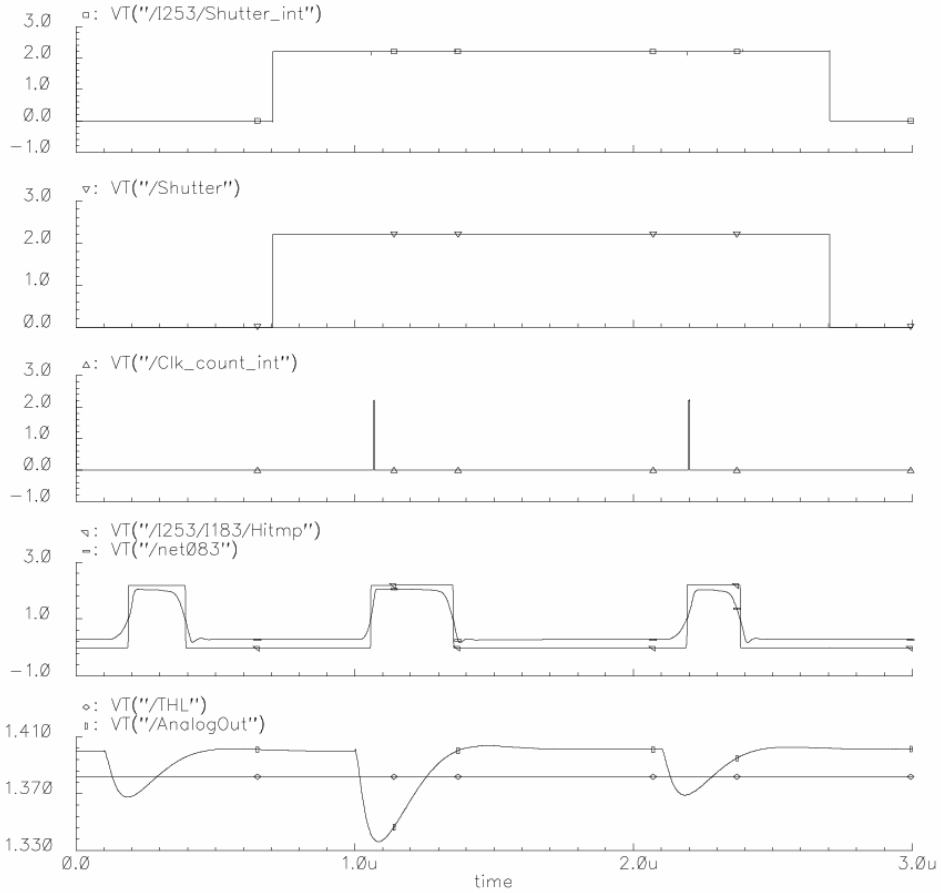


100MHz

Medipix Mode (P0=0,P1=0)

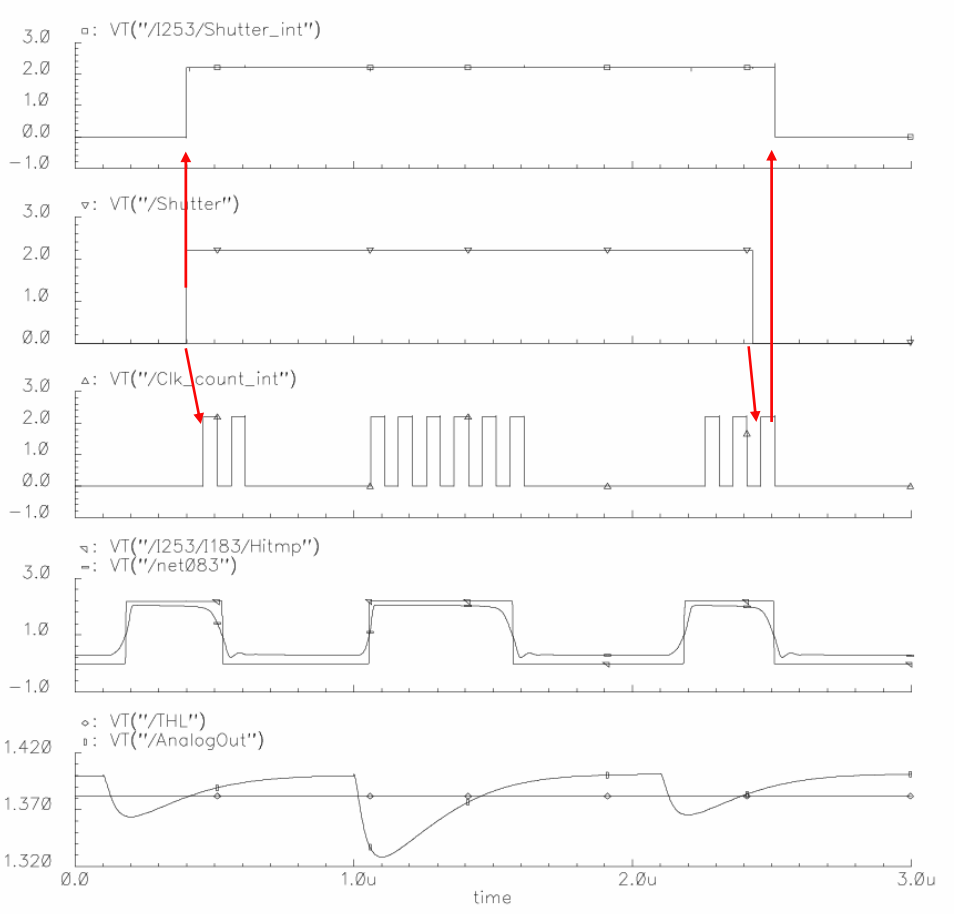


10MHz



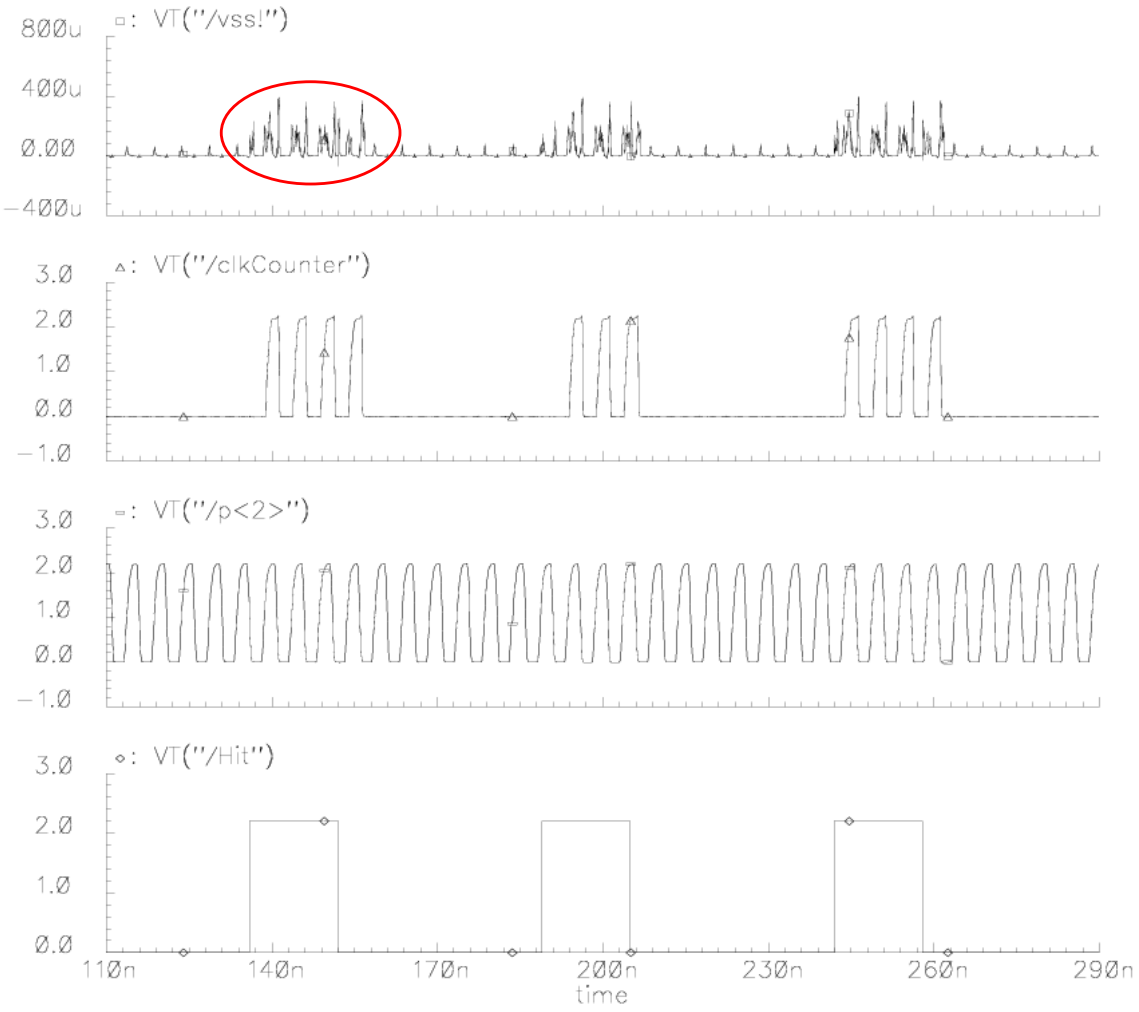
100MHz

Internal Shutter control



- Internal Shutter is always synchronous to the clock to avoid glitches
- Counter starts counting if a hit is present when shutter starts
- Shutter closing happens with a maximum delay of 1Tclk if a hit is present when shutter closes

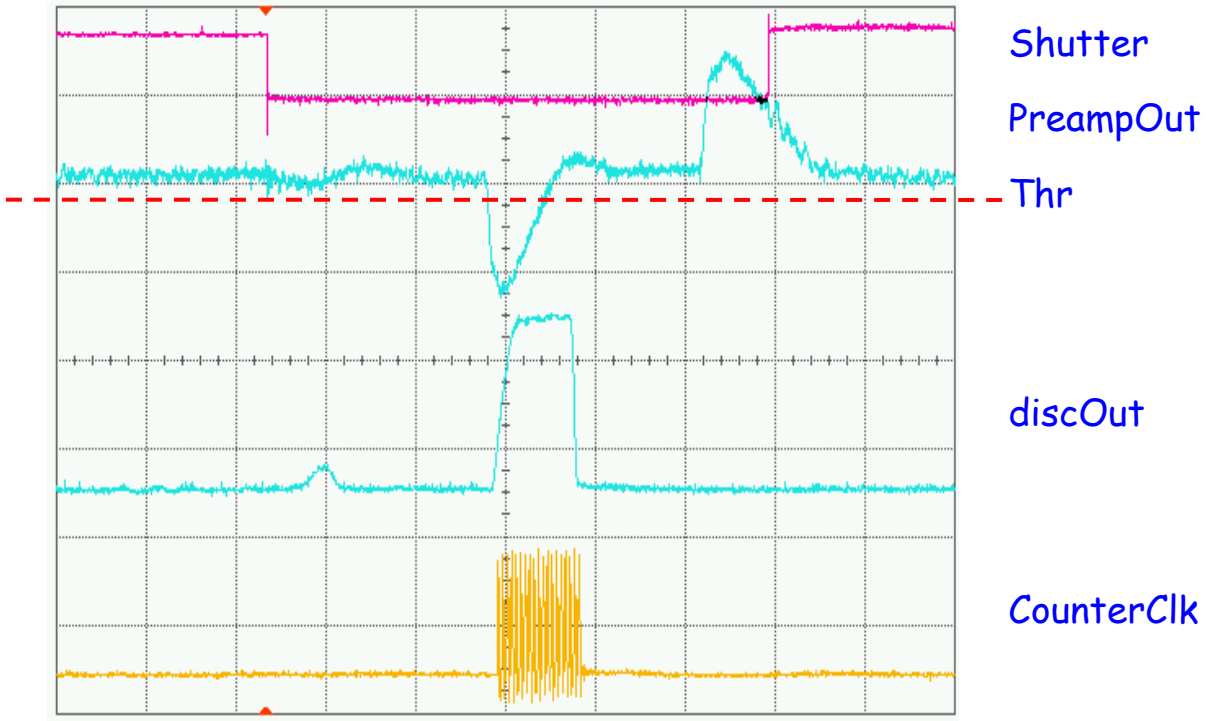
Digital power consumption



- Reduce digital power of the TSL cores → No power consumption in stand-by (no hit)
- In stand-by the only digital consumption is the buffering of the Ref_Clk
- Controlled by design of the core1 asynchronous network.

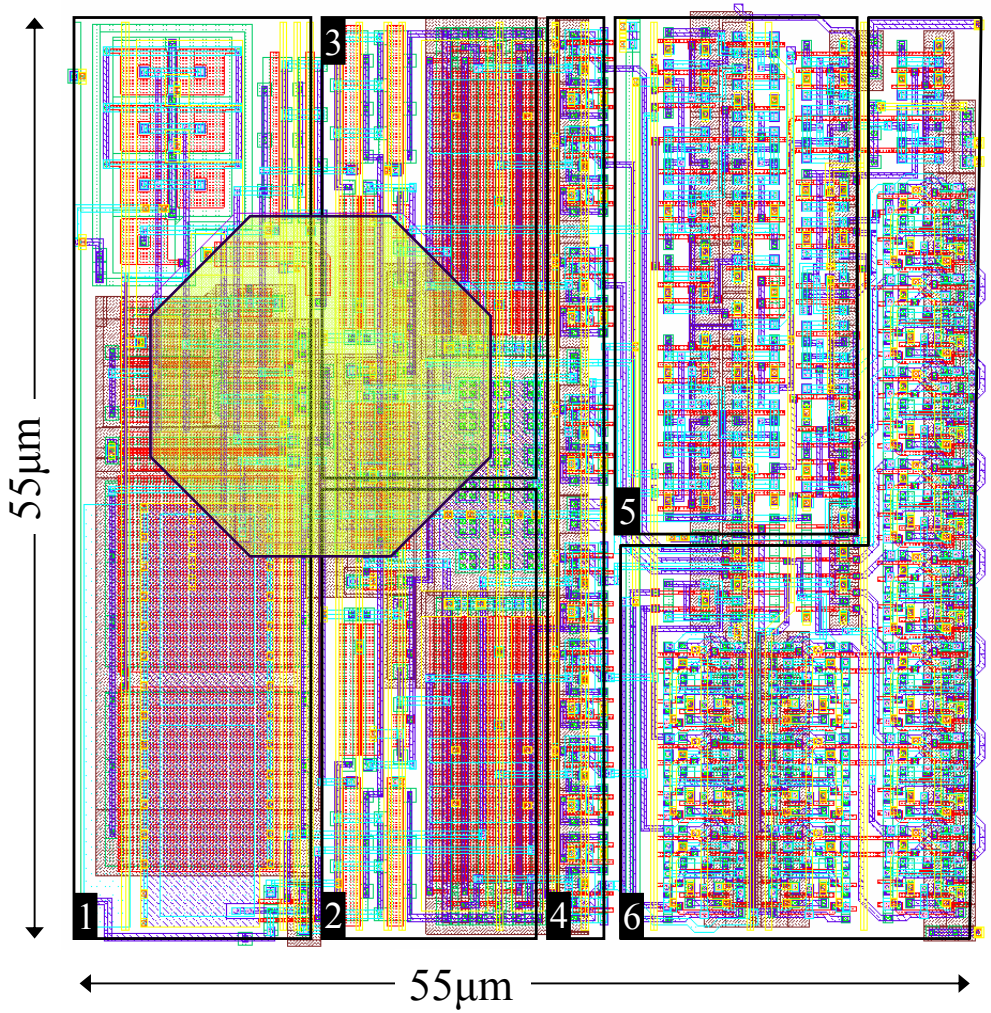
Pixel measurements

- From the 2 test pixels [120:121,0] one can measure the preampOut, discOut, internal Ref_Clk and the counter clock
- State Machine of the counter Modes (P0, P1) work as expected
- No visible coupling of the Ref_Clk signal into the analog signals (preampOut and discOut)

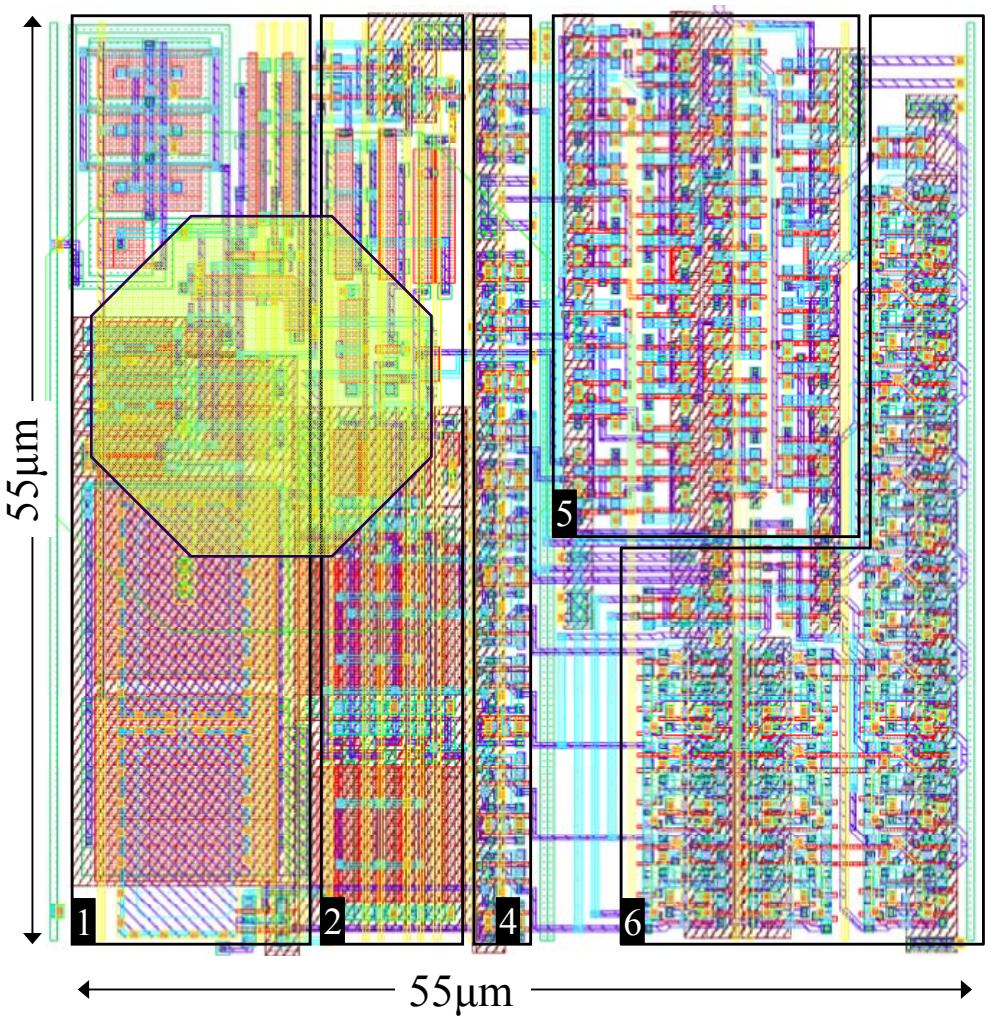


Timepix Layout status

Mpix2MXR20 layout

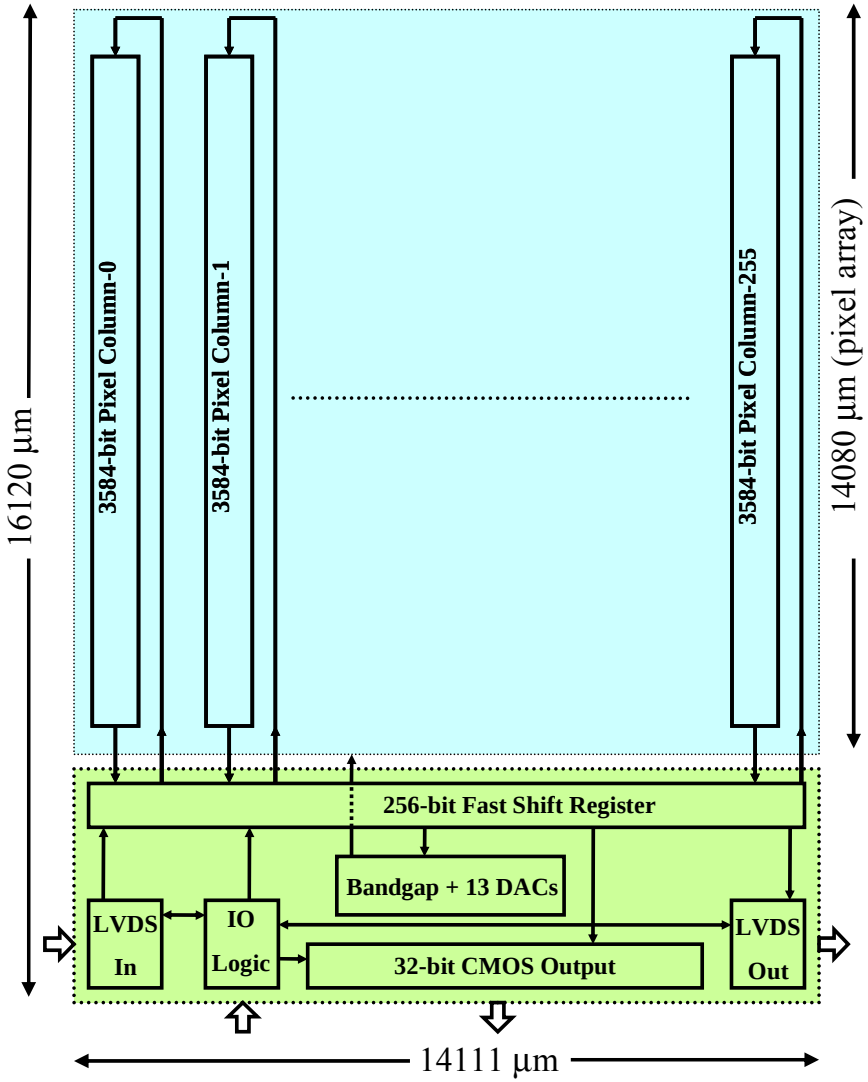


Timepix layout



Timepix chip architecture

- Chip architecture almost identical to Mpix2MXR20
  - M0=M1=1 and Shutter ON -> FClock used as Ref_Clk
- 256x256 55μm square pixels
- Analog Power -> 440mW
- Digital Power (Ref_Clk=50MHz) -> 220mW
- Serial readout (@100MHz) -> 9.17 ms
- Parallel readout (@100MHz) -> 287 μs
- > 36M Transistors

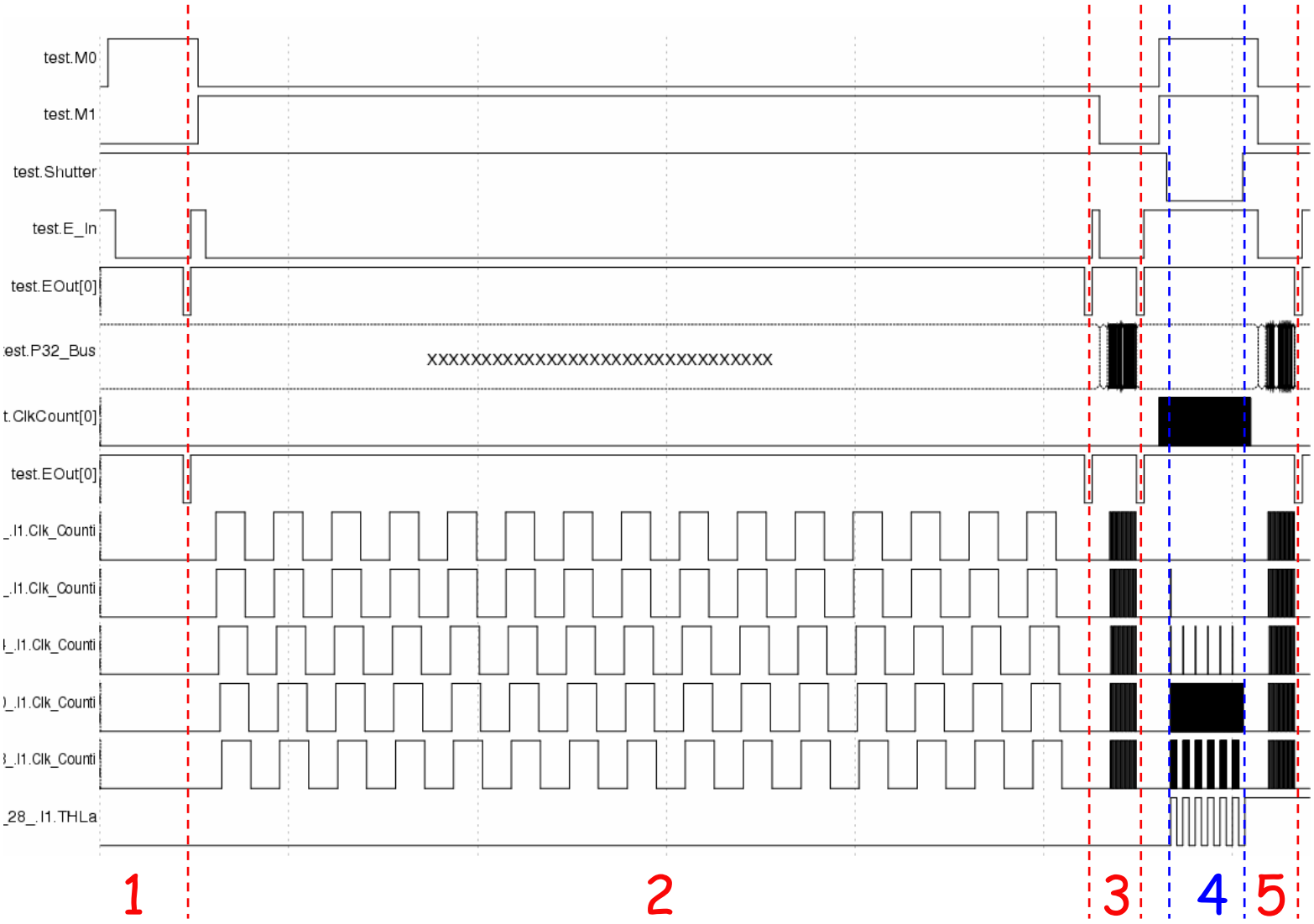


Periphery Verilog Simulations

- This simulation tests 1 row of pixels and the full chip control logic
- Tested with normal and corner ($\pm 3\sigma$) parameters successfully
- Pixel control logic is initialized after a set mask command
- M0=1 and M1=1 when counting will enable the clock distribution to the pixel matrix

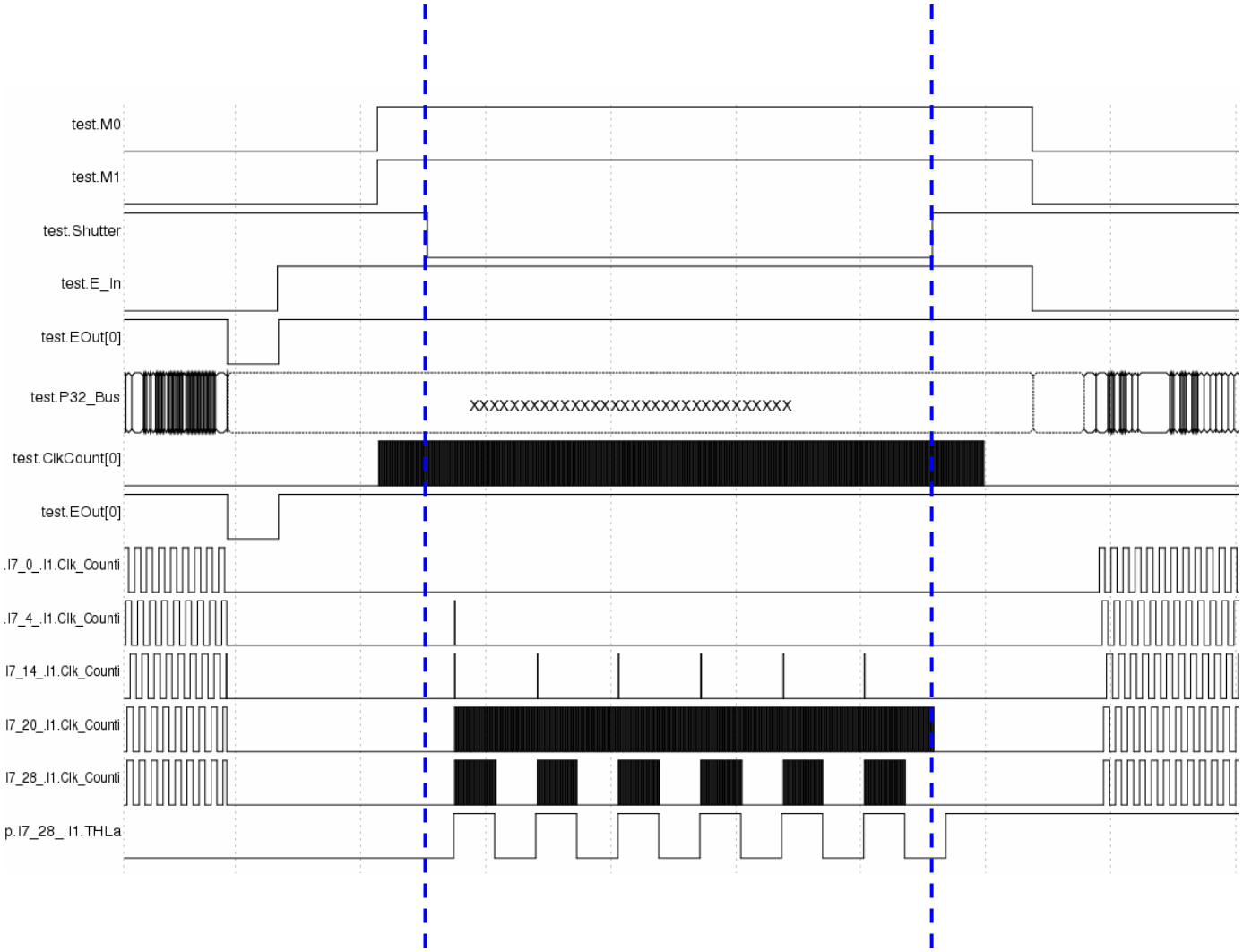
M0	M1	Enable_IN	Shutter	Reset	P_S	I/O	FClock num (per chip)	Operation
X	X	X	X	0	X	I	X	**General reset of the chip**
1	1	X	0	1	X	X	X	**Counting**
0	0	0	1	1	0	I/O	917768	**Serial Readout Matrix (Slow Reset Matrix)**
0	0	0	1	1	1	I/O	28688	**Parallel Readout Matrix (Fast Reset Matrix)**
0	1	0	1	1	X	I	917768	**Set Matrix**
1	0	0	1	1	X	I/O	264	**Write/Read FSR (DACs and CTPR)**

Single chip Verilog simulation



1:SetDACs
2:SetMatrix
3:ResetMatrix (PS=1)
4:Counting
5:Readout (PS=1)

Counting Modes (Mask,P0 and P1)



⇐ Pixel Masked P0=X, P1=X and Mask=1

⇐ Tpix-1h mode P0=0, P1=1 and Mask=0

⇐ Mpix2 mode P0=0, P1=0 and Mask=0

⇐ Tpix mode P0=1, P1=1 and Mask=0

⇐ CCD mode P0=1, P1=0 and Mask=0

Medipix2 vs Timepix

	Medipix2	Timepix
Physical dimensions	=	=
IO PADs	=	=
Charge collection	e^-, h^+	e^-, h^+
Pixel functionality	PhotonCounting	PhotonCounting, TOT, Timepix
Amplifier Gain	~10mV/Ke$^-$	~18mV/Ke$^-$
Noise	~110e$^-$	~75e$^-$
Linearity	Up to 100Ke$^-$	Up to 50Ke$^-$
Thresholds	2 (3+3 bits adj)	1 (4bits adj)
σ equalized	~100e$^-$	~25e$^-$
Minimum Threshold	~900e$^-$ (measured)	~500e$^-$ (expected)*
Counter Depth/Overflow	14-bits/Yes	14-bits/Yes
Max Analog power	10μW/pix 300mA/chip	6.5μW/pix 190mA/chip
Static Digital Power	none	200mA@100MHz
Readout	Serial/Parallel	Serial/Parallel
Readout compatibility	100%	95% (Clock active when shutter ON)

Summary & Conclusions

- Timepix is a modification of the Medipix chip
- Improvements in Gain and threshold equalization -> expected lower threshold (~900e^- → ~600e^-)
- Pixel operation mode is selectable for each pixel
- TimeStamp reference (Ref_Clk) generated by a common clock distributed all over the chip
- Timepix time line:
  - Desgin: 6 months (January06-June06)
  - Fabrication: 2 months (July06-August06)
  - Testing: 1 months so far (mid September06-?)