Silicon strips readout using Deep Sub-Micron Technologies

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on behalf of

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Work in the framework of the SiLC
(Silicon for the Linear Collider) R&D Collaboration and the EUDET I3-FP6 Europeean Project

EUDET Annual meeting October 18-20 2006 Muenchen

Outline

- Detector data
- Technologies
- Front-End Electronics
- 180nm chip
- 130nm chips
- Future plans

Example:
A Silicon strips tracker at the ILC

- A few 10^6 Silicon strips
- 10 - 60 cm long
- Thickness 200-500 μm
- Strip pitch 50-200 μm
- Single sided, AC or DC coupled

Silicon strips data at the ILC

- Pulse height: Cluster centroid to get a few µm position resolution
  Detector pulse analog sampling

- Time: Two scales:
  - Coarse : 150-300 ns for BC identification, 80ns sampling

    Shaping time of the order of the microsecond
  - Fine: nanosecond timing for the coordinate along the strip
    10ns sampling

    Not to replace another layer or double sided
    Position estimation to a few cm using pulse reconstruction from samples

Shaping time: 20-50 ns

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Technologies

Silicon detector and VLSI technologies allow to improve detector and front-end electronics integration

Front-end chips:

- Thinner CMOS processes 250, 180, 130, 90 nm now available from Europractice (IMEC, Leuven)
- SiGe, less 1/f noise, faster
- Chip thinning down to 50 μm

More channels on a chip, more functionalities, less power

Connectivity:

- On detector bump-bonding (flip-chip)
- 3D

Smaller pitch detectors, better position and time resolution. Less material

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Integrated functionalities

- Full readout chain integration in a single chip

  - Preamp-shaper
  - Trigger decision (analog sums) → sparse data
  - Sampling: Analog pipe-lines
  - On-chip digitization
  - Buffering and pre-processing:
    Centroids, Least square fits, Lossless compression and error codes

  - Calibration and calibration management
  - Power switching (ILC)

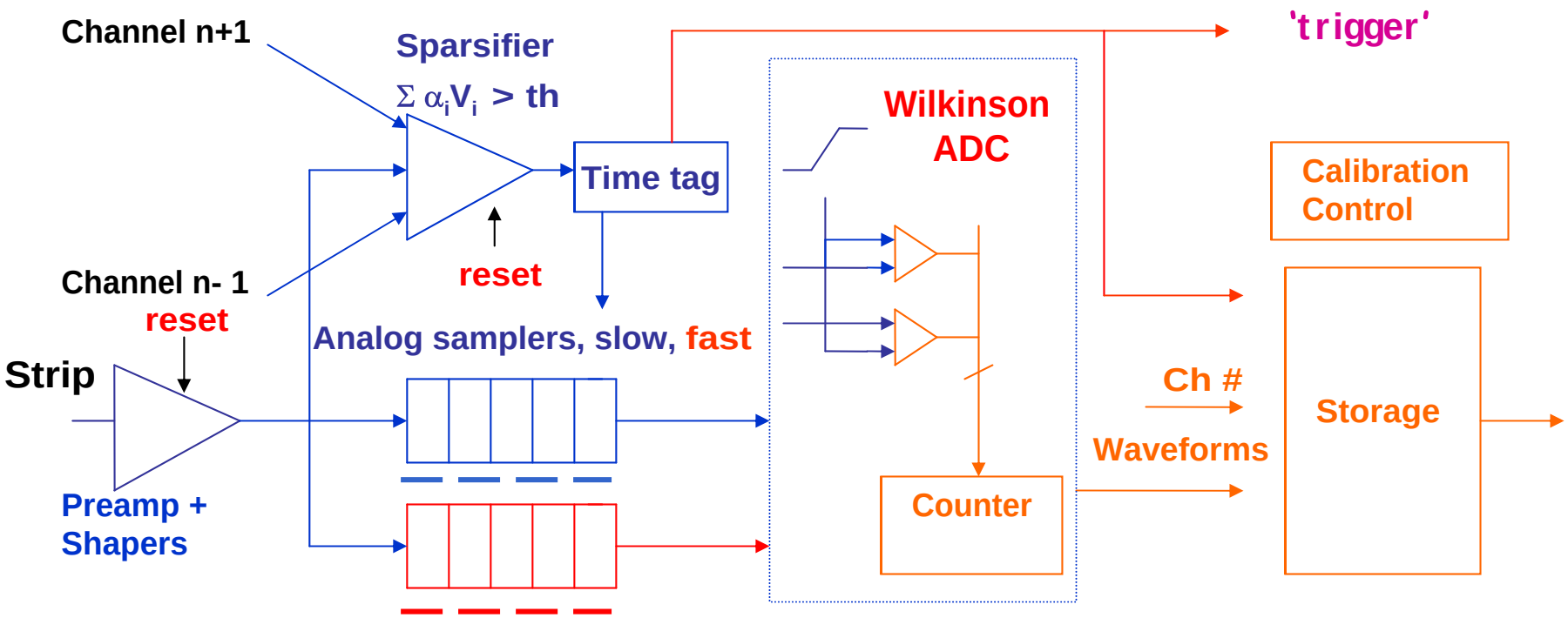
- Presently 128 channels (APV, SVX), 256-1024 envisaged (Kpix)

Front-End Chip goals

- Integrate 512-1024 channels in 90nm CMOS:
  - **amplifiers:** **20- 30 mV/MIP over 30 MIP**
  - **shapers:**
    - **slow option 500 ns – 1 μs**
    - **fast option 20- 50 ns**
  - **sparsifier:** **threshold the sum of adjacent channels**
  - **samplers:**
    - **8- 16 samples**
      80 ns and 10 ns sampling clocks
    - **Event buffer 16- deep**
  - **ADC:** **10 bits**
  - **Buffering, digital pre- processing**
  - **Calibration**
  - **Power switching saves a factor 200 at more:**

ILC timing: **1 ms: ~ 3- 6000 trains @150- 300ns / BC**
200ms in between

Foreseen Front-end architecture



Charge 1- 40 MIP, Time resolution: BC tagging 150- 300ns, fine: ~ 1ns

Technologies: Deep Sub-Micron CMOS 180-130nm
Future: SiGe &/or deeper DSM

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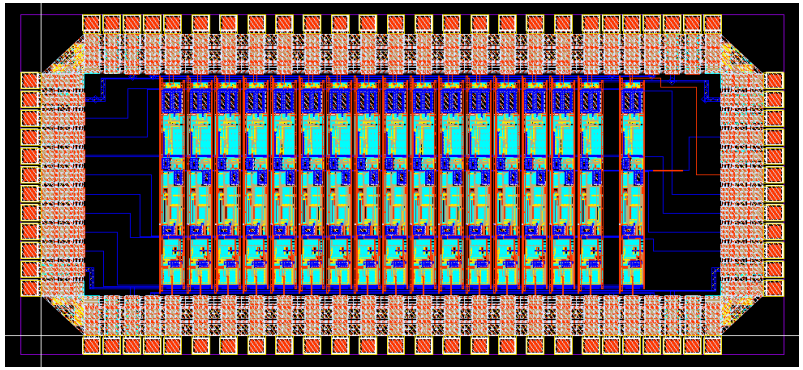
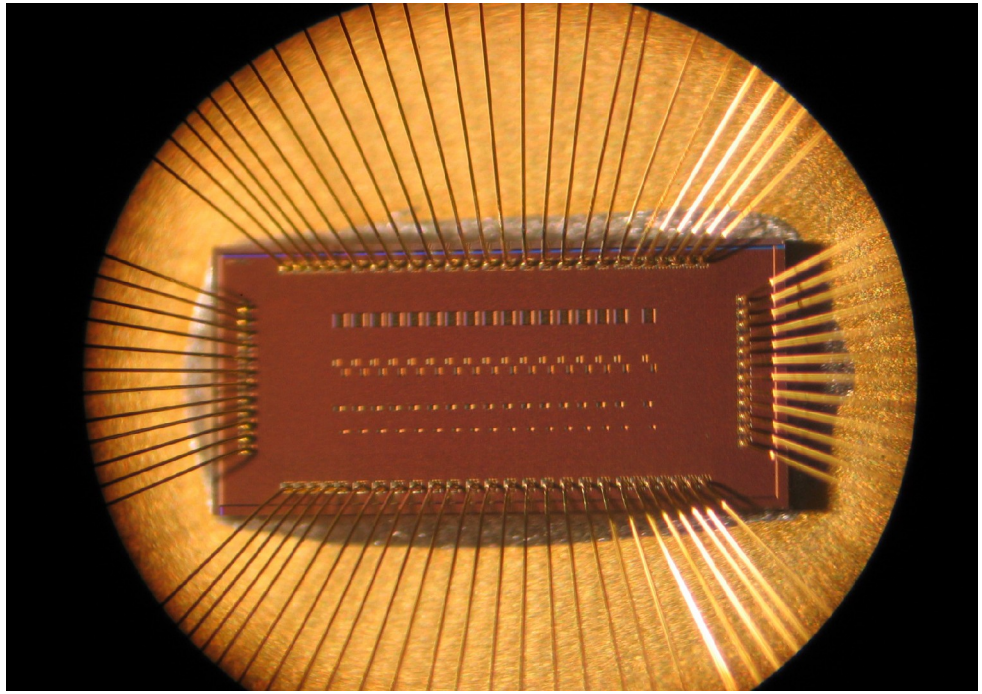
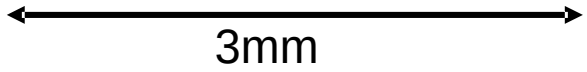
Silicon



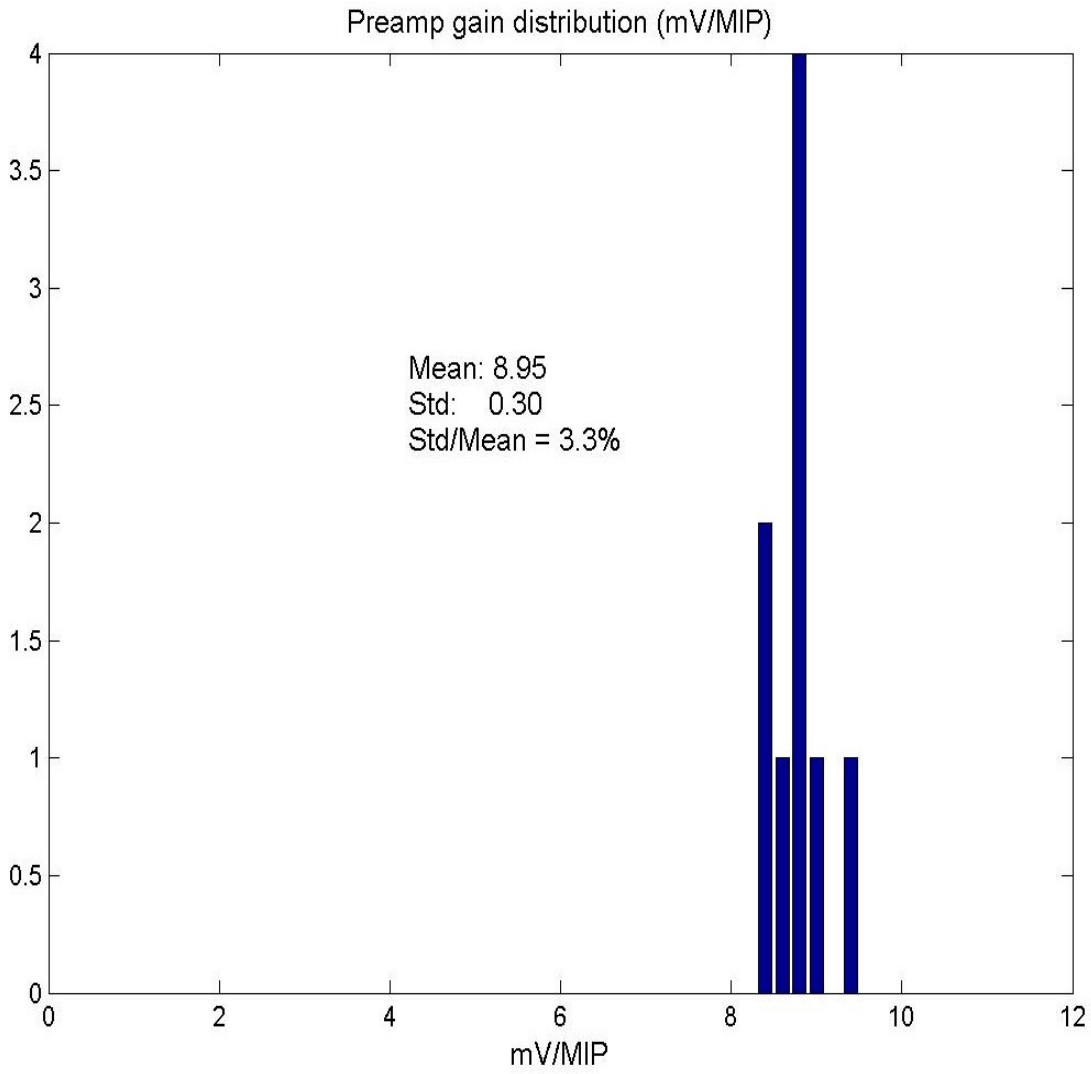


- Preamp
- Shaper
- Sample & Hold
- Comparator



16 + 1 channel UMC 180nm chip (layout and picture)
Europractice (Leuven)

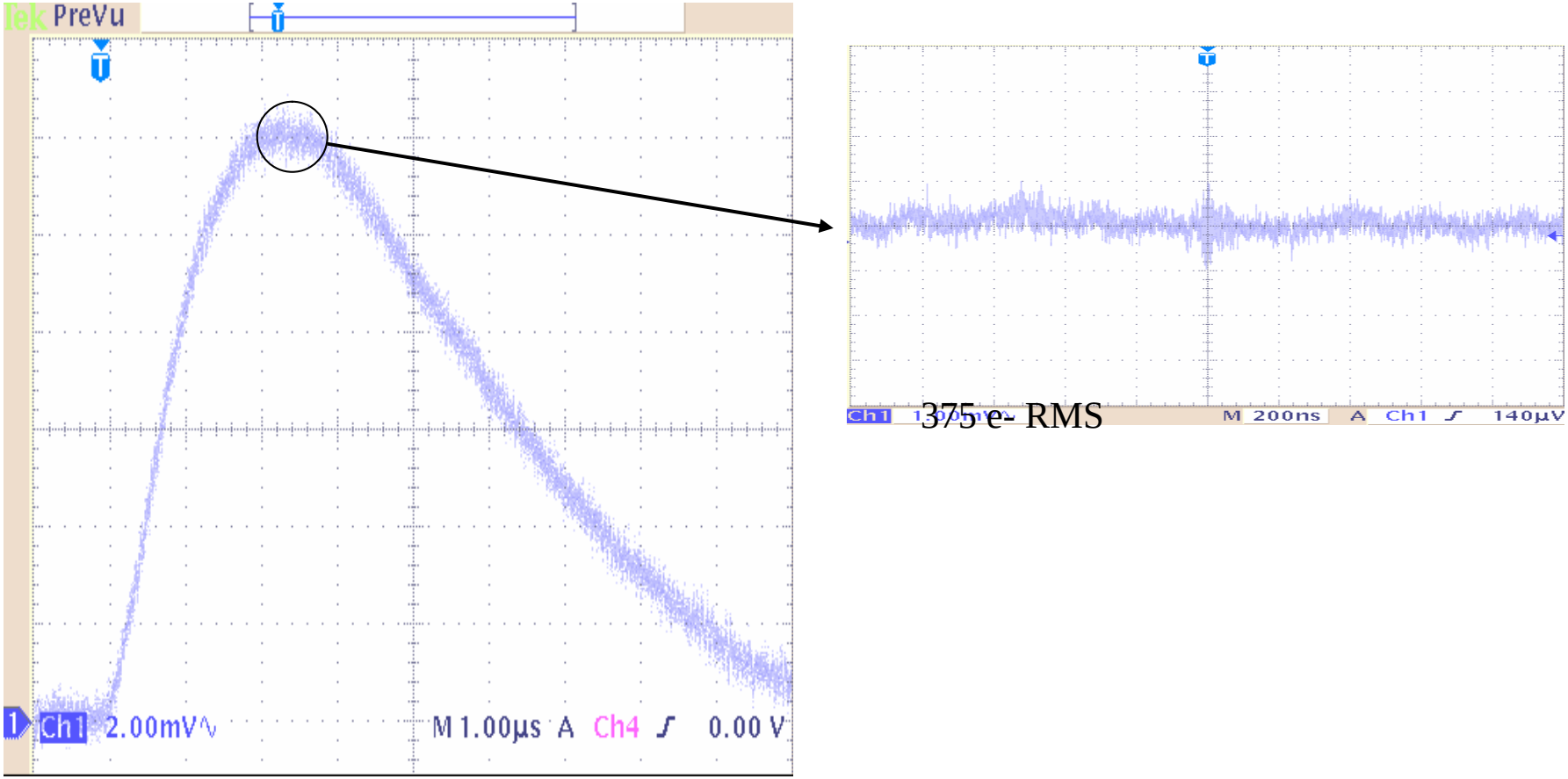
Process spreads



Preamp gains statistics

Process spreads within a wafer: 3.3 %

Shaper output noise



375 e- RMS

375 e- +10.4 e-/pF input noise with chip-on-board wiring
275 + 8.9/ pFsimulated

Tests Conclusions

12 chips tested ('05)

The UMC CMOS 180nm process is mature and reliable:

- Models mainly OK
- Only one transistor failure over 12 chips
- Process spreads of a few %

Beam tests in October '06 at DESY

Encouraging results regarding CMOS DSM

→ go to 130nm

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Front-end in CMOS 130nm

130nm CMOS:

- Smaller
- Faster
- More radiation tolerant
- Less power
- Will be (is) dominant in industry

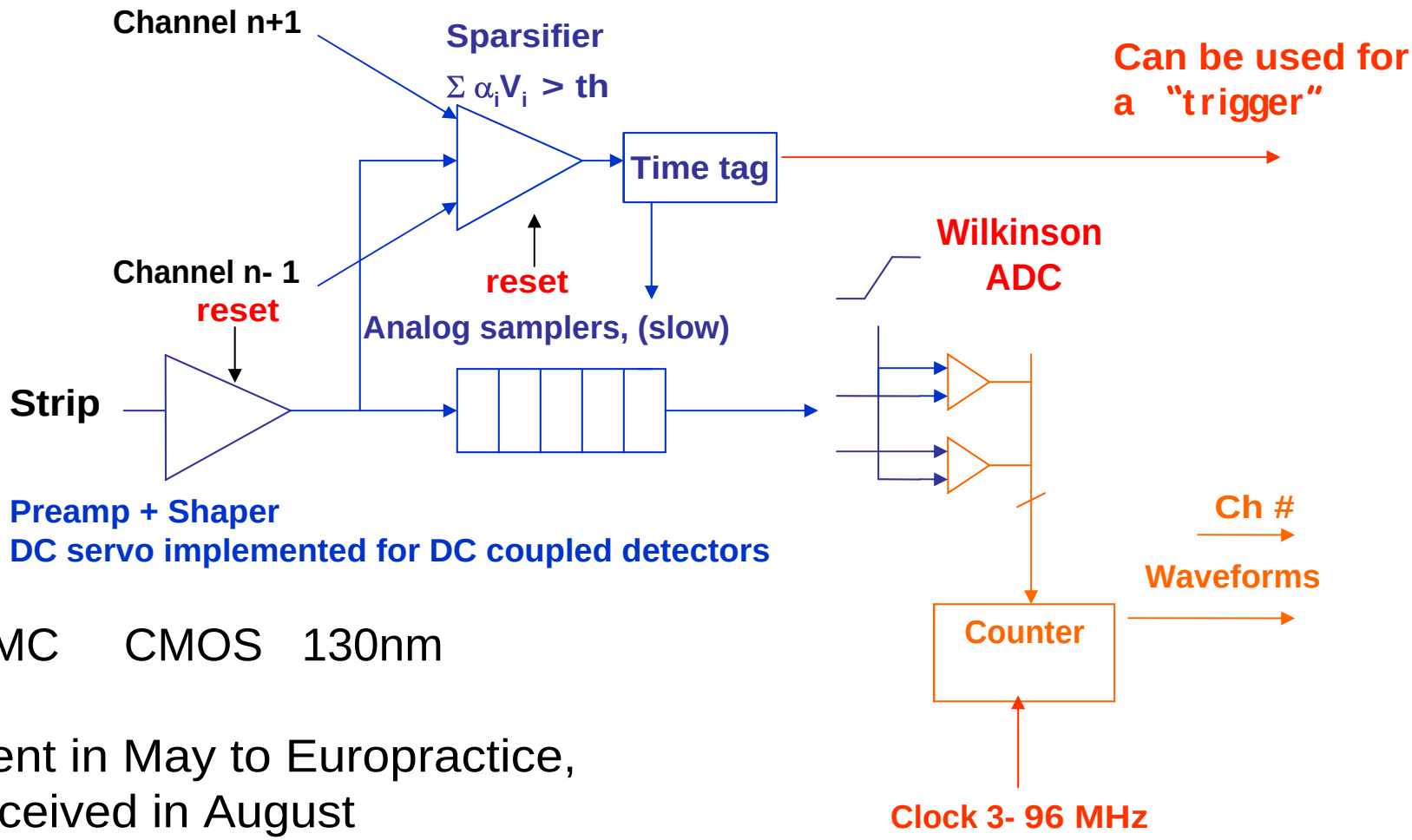
Features:

- Design more constraining
- Reduced voltage swing (Electric field constant)
- Leaks (gate/subthreshold channel)
- Models more complex, sometimes not accurate

UMC Technology parameters

	180 nm	130nm
• 3.3V transistors	yes	yes
• Logic supply	1.8V	1.2V
• Metals layers	6 Al	8 Cu
• MIM capacitors	1fF/mm²	1.5 fF/mm²
• Transistors	Three Vt options	Low leakage option

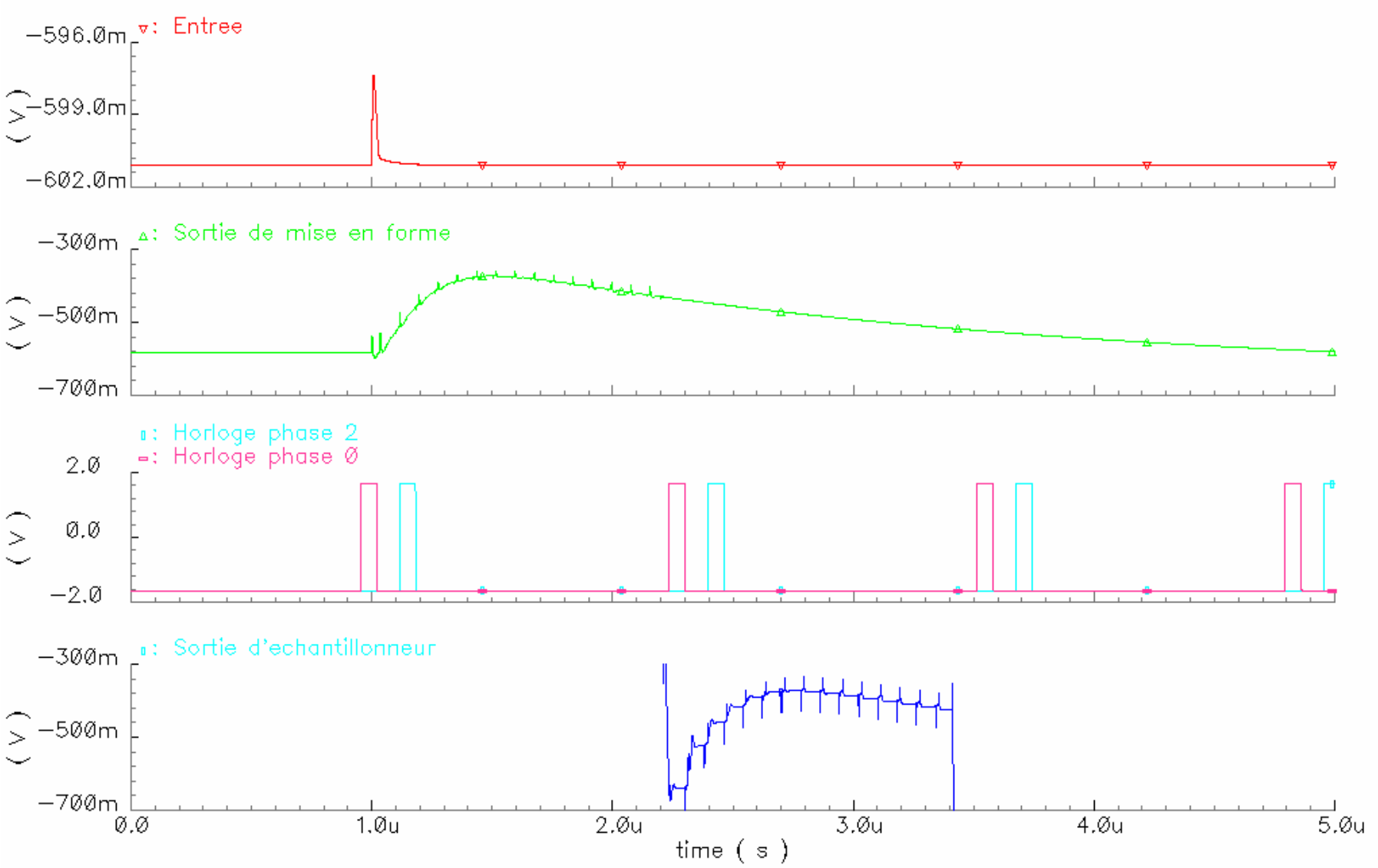
130nm 4-channel test chip



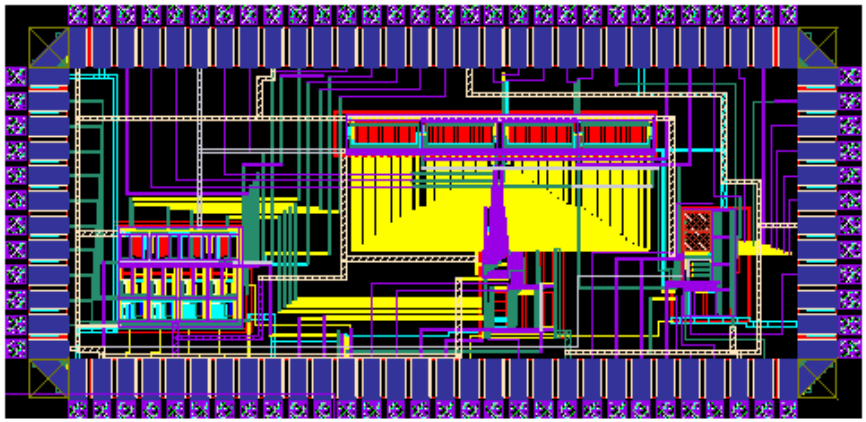
UMC CMOS 130nm

Sent in May to Europractice,
received in August
Being tested

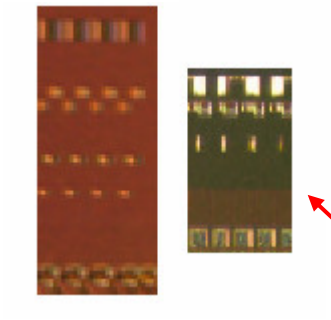
Analog pipeline simulation



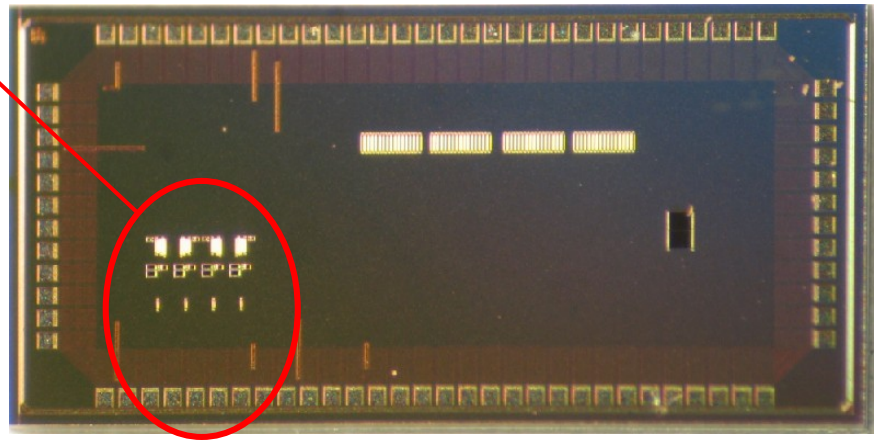
Silicon



Layout of the 130nm chip including sampling and A/D conversion



180nm 130nm

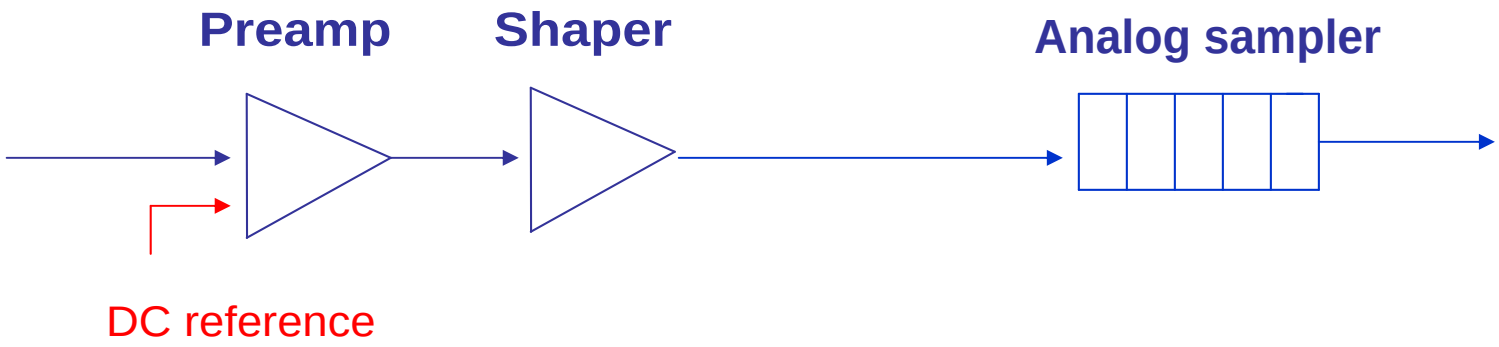


Picture

Presently
Under tests

One channel chip with DC servo

DC servo to accommodate DC coupled detectors



Sent beg October

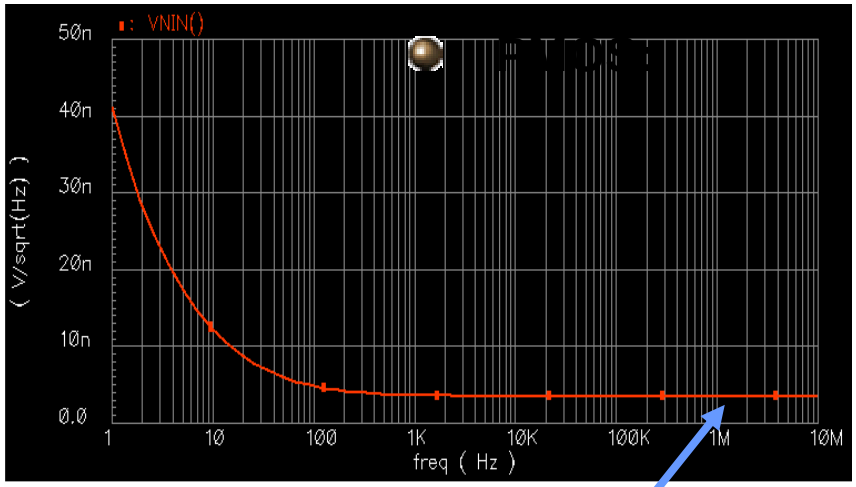
Some issues with 130nm design

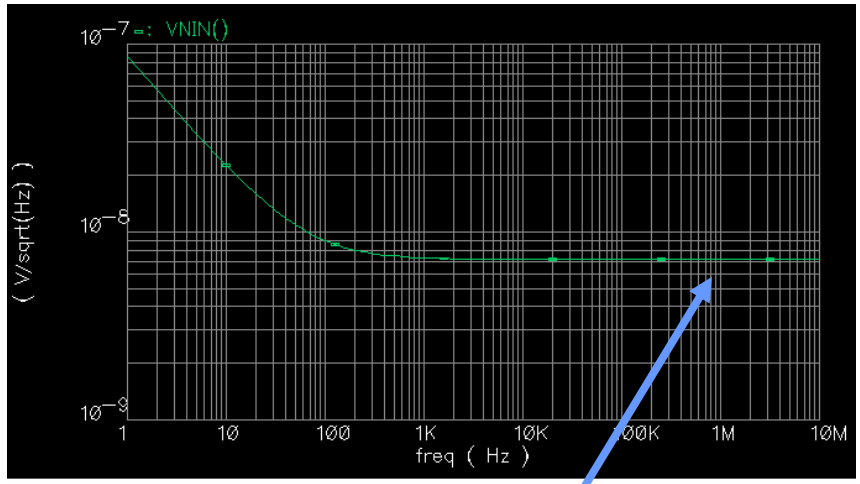
- Noise likely not properly modeled (UMC dixit, to be checked)
- Design rules more constraining
- Some design rules (via densities) not available under Cadence

  Calibre (Mentor) required
- Low Vt transistors leaky (Low leakage option available)

Possible issues: noise: 130nm vs 180nm (simulation)

PMOS





180nm

gm=944.4uS

1MHz → 3.508nV/sqrt(Hz)

Thermal noise hand calculation = 3.42nV/sqrt(Hz)

130nm

gm=815.245uS

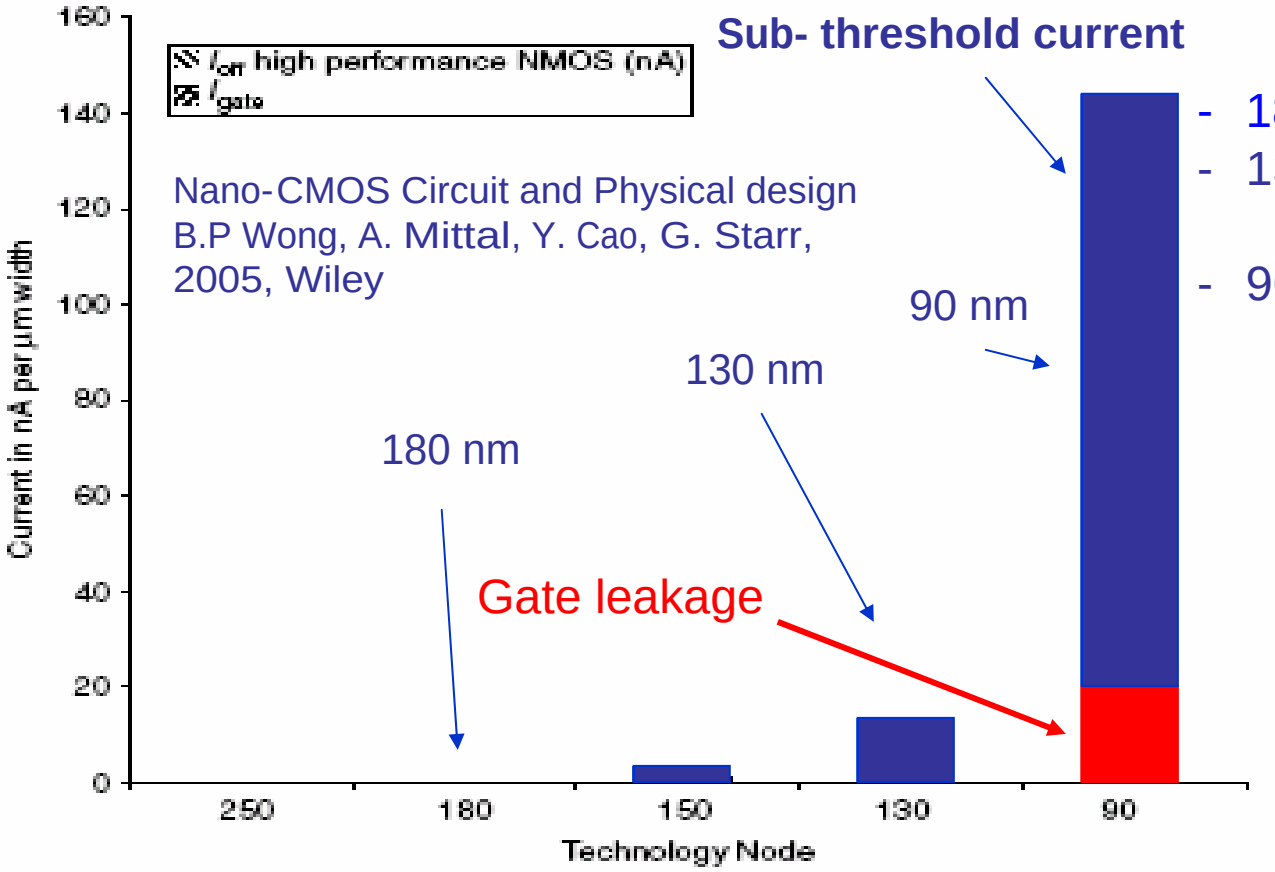
1MHz → 7.16nV/sqrt(Hz)

Thermal noise hand calculation = 3.68nV/sqrt(Hz)

Thermal noise measured by Wladimir Gromov (NIKHEF) with IBM130nm OK

Transistors leaks

- Gate-channel due to tunnel effect
- Through channel when transistor switched-off



- 180nm OK
- 130nm, no gate leaks
  sub-threshold leaks
- 90nm, gate +
  sub-threshold leaks

Figure 1.2 I_{gate} and subthreshold leakage versus technology.

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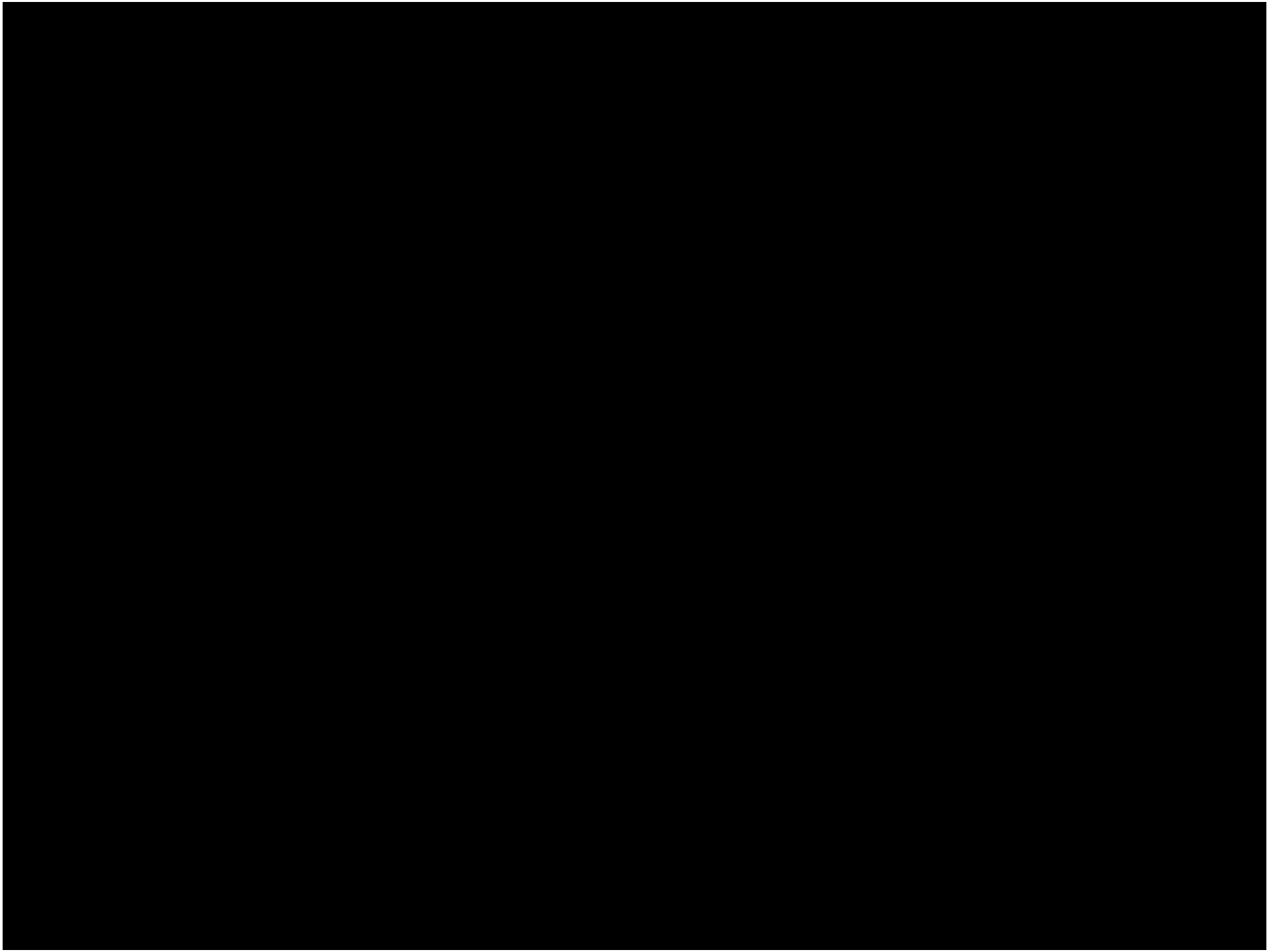
Planned on-chip digital

- Chip control
- Buffer memory
- Processing for
  - Calibrations
  - Amplitude and time least squares estimation, centroids
  - Raw data lossless compression
- Tools
  - Digital libraries in 130nm CMOS available (Artisan, VST)
  - Place & Route tools: Cadence + design kits
  - Synthesis from VHDL/ Verilog
  - Some IPs: PLLs, SRAM

Next developments

- Submit a full 32-64 channel version including slow and fast analog processing, power cycling, digital
- Implement the fast (20-50ns shaping) version including:
  - Preamp + Shaper (20-100ns)
    - Fast sampling



backup

Beam-tests at DESY

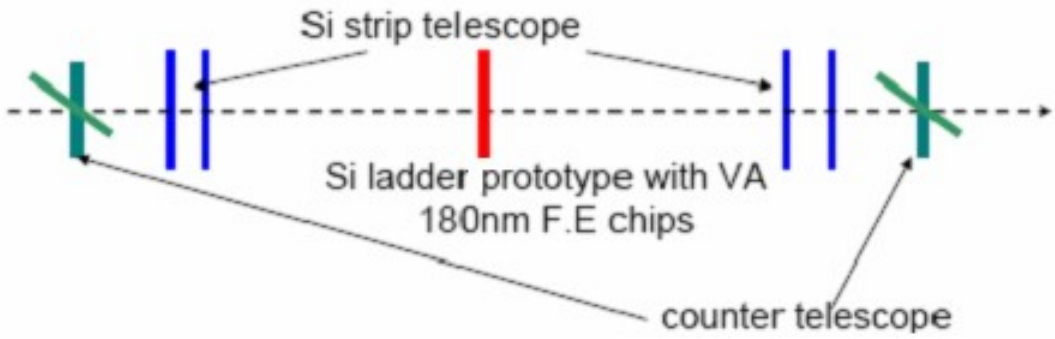
At 5 Gev e- beam in DESY

Very simple telescope set-up in Silicon strips ladders of CMS read out with VA1 FE and a few channels with present version of new FE chip together with a reference telescope

Purposes:

Check S/N for the first proto measured at Lab test bench

Characterize performance of the new FE chip in realistic conditions after Lab test bench and comparing with ref FE electronics (VA1)

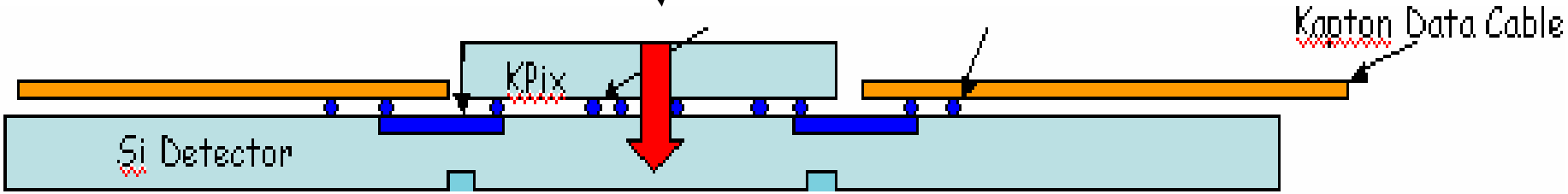


October 2006

Wiring Detector to FE Chips

~~Wire bonding~~

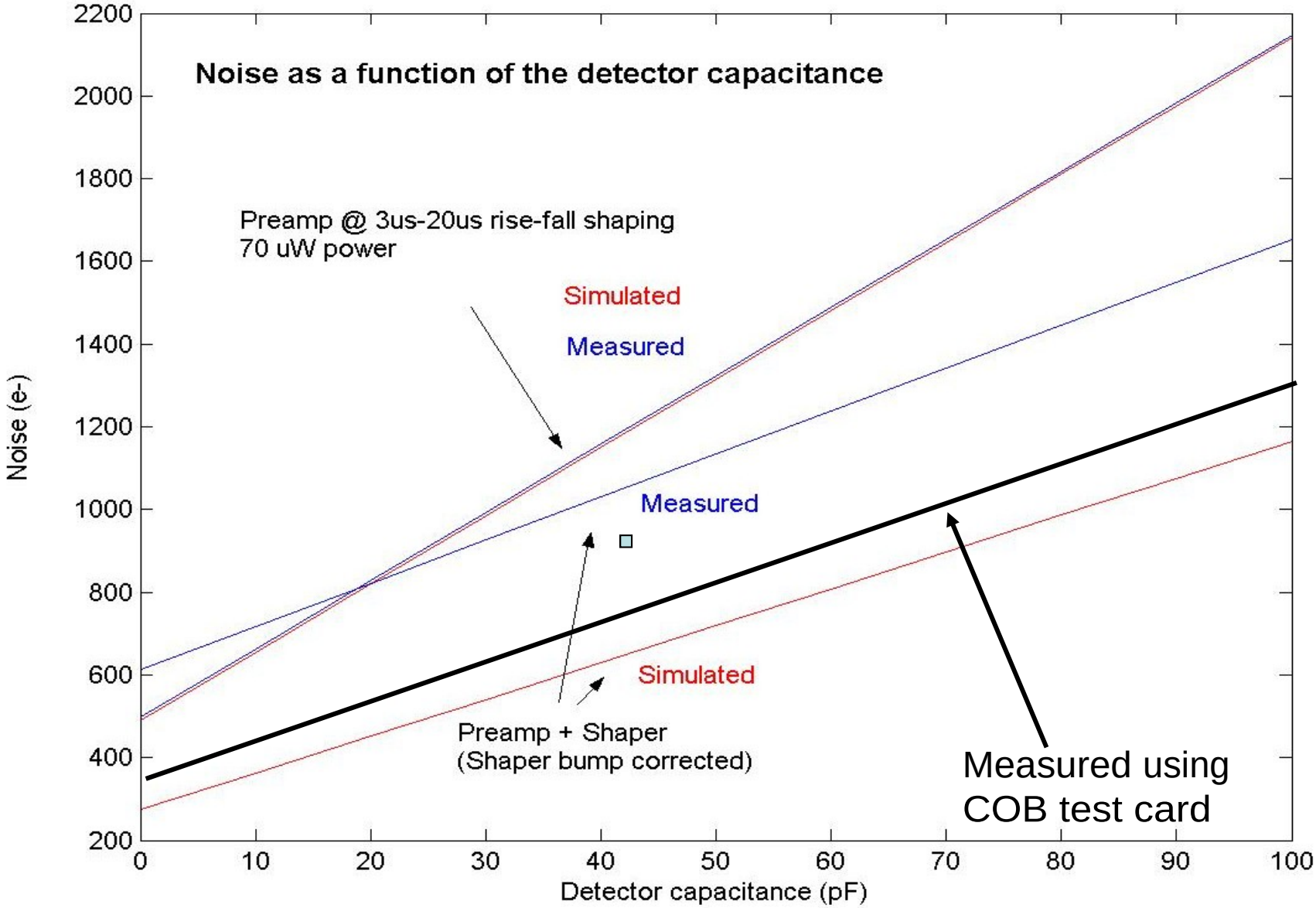
Flip Chip Technology



Courtesy: Marty Breidenbach (Cal SiD)

OR (later)

Noise summary (180nm)

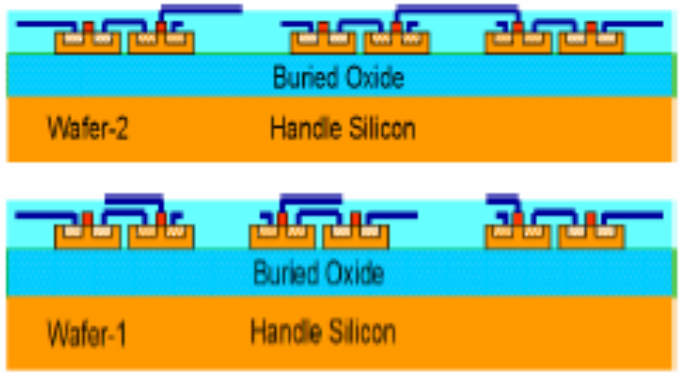


3D Wiring

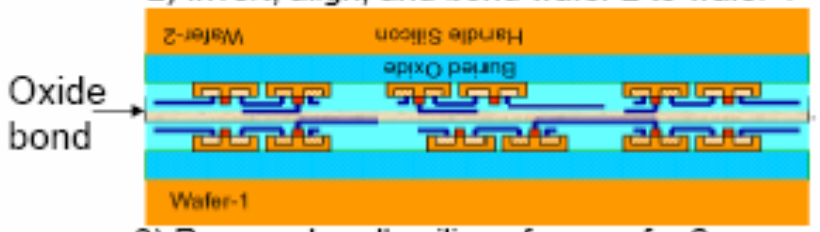
Process flow for 3D Chip

- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

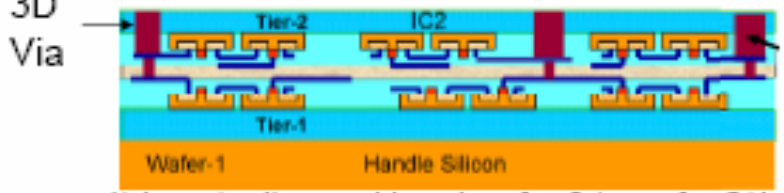
1) Fabricate individual tiers



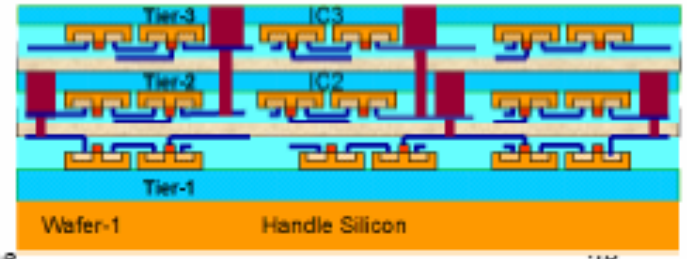
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



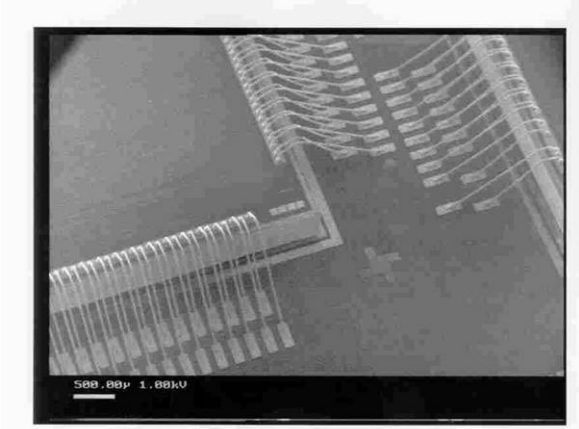
May 2006 FEE 2006 36

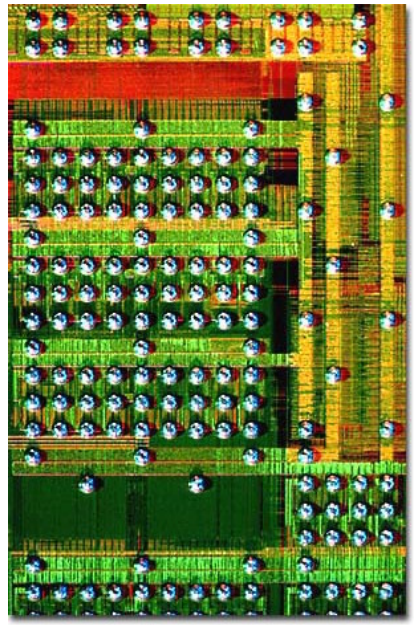
Courtesy: Ray Yarema, FEE 2006, Perugia

Manuel Lozano (CNM Barcelona)

Chip connection

- Wire bonding
  - Only periphery of chip available for I O connections
  - Mechanical bonding of one pin at a time (sequential)
  - Cooling from back of chip
  - High inductance (~1nH)
  - Mechanical breakage risk (i.e. CMS, CDF)
- Flip-chip
  - Whole chip area available for I O connections
  - Automatic alignment
  - One step process (parallel)
  - Cooling via balls (front) and back if required
  - Thermal matching between chip and substrate required
  - Low inductance (~0.1nH)





Manuel Lozano (CNM Barcelona)

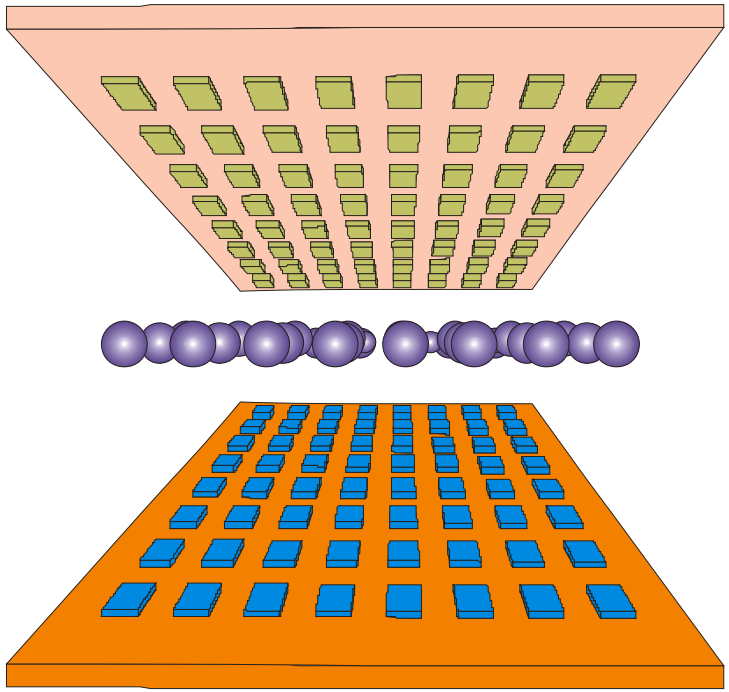
Bump bonding flip chip technology

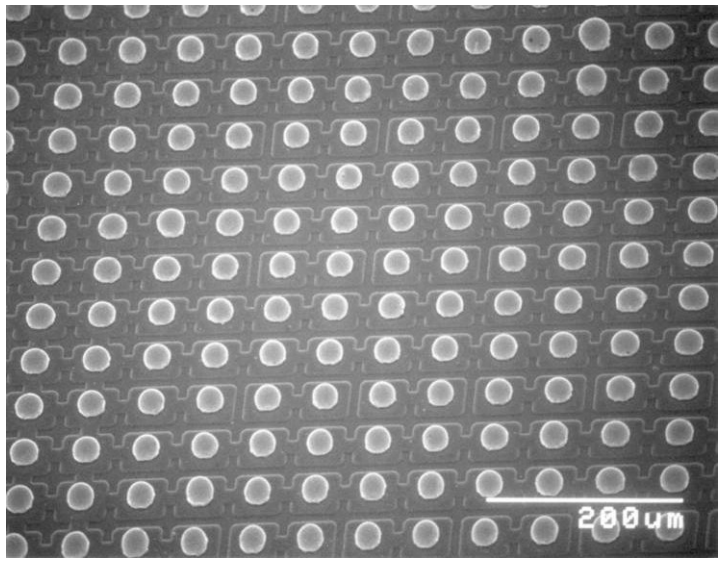
- Electrical connection of chip to substrate or chip to chip face to face

flip chip

- Use of small metal bumps

bump bonding





CNM

- Process steps:
  - Pad metal conditioning: Under Bump Metallisation (UBM)
  - Bump growing in one or two of the elements
  - Flip chip and alignment
  - Reflow
  - Optionally underfilling

Manuel Lozano (CNM Barcelona)

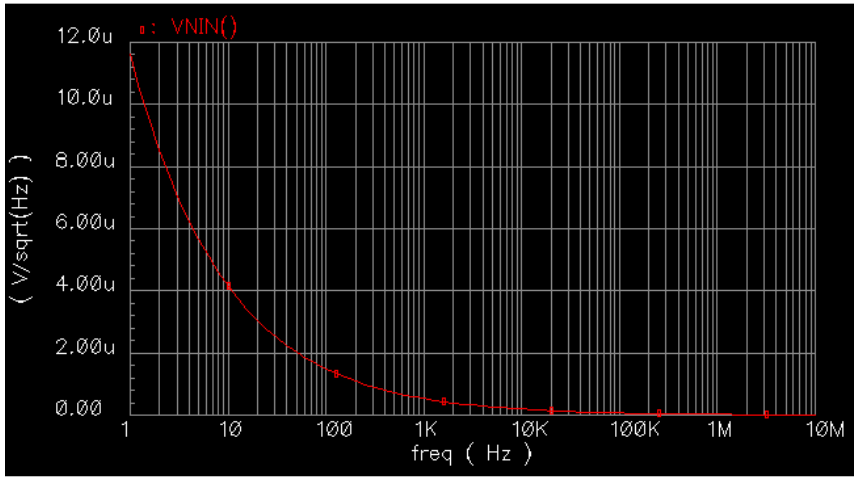
Bump bonding flip chip technology

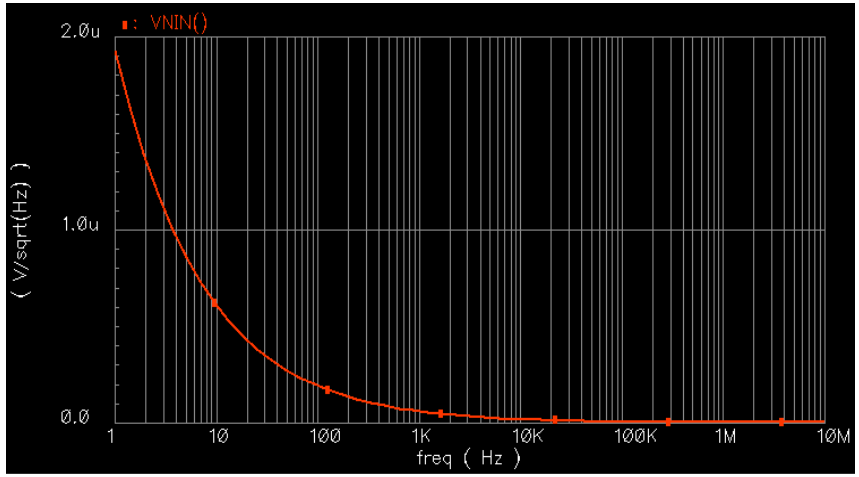
- Expensive technology
  - Especially for small quantities (as in HEP)
  - Big overhead of NRE costs
- Minimal pitch reported: 18 µm but ...
- Few commercial companies for fine pitch applications (< 75 µm)

- Bumping technologies
  - Evaporation through metallic mask
  - Evaporation with thick photoresist
  - Screen printing
  - Stud bumping (SBB)
  - Electroplating
  - Electroless plating
  - Conductive Polymer Bumps
  - Indium evaporation

Noise: 130nm vs 180nm (simulation)

NMOS :





130nm
W/L = 50u/0.5u
Ids=48.0505u,Vgs=260mV,Vds=1.2V
gm=772.031uS,gms=245.341uS,gds=6.3575uS
1MHz --> 24.65nV/sqrt(Hz)
100MHz --> 5nV/sqrt(Hz)
Thermal noise hand calculation = 3.78nV/sqrt(Hz)

180nm
W/L=50u/0.5u
Ids=47uA,Vgs=300mV,Vds=1.2V
gm=842.8uS,gms=141.2uS,gds=16.05uS
1MHz --> 4nV/sqrt(Hz)
10MHz --> 3.49nV/sqrt(Hz)
Thermal noise hand calculation = 3.62nV/sqrt(Hz)