A General Purpose Charge Readout Chip for TPC Applications

Munich, 19 October 2006

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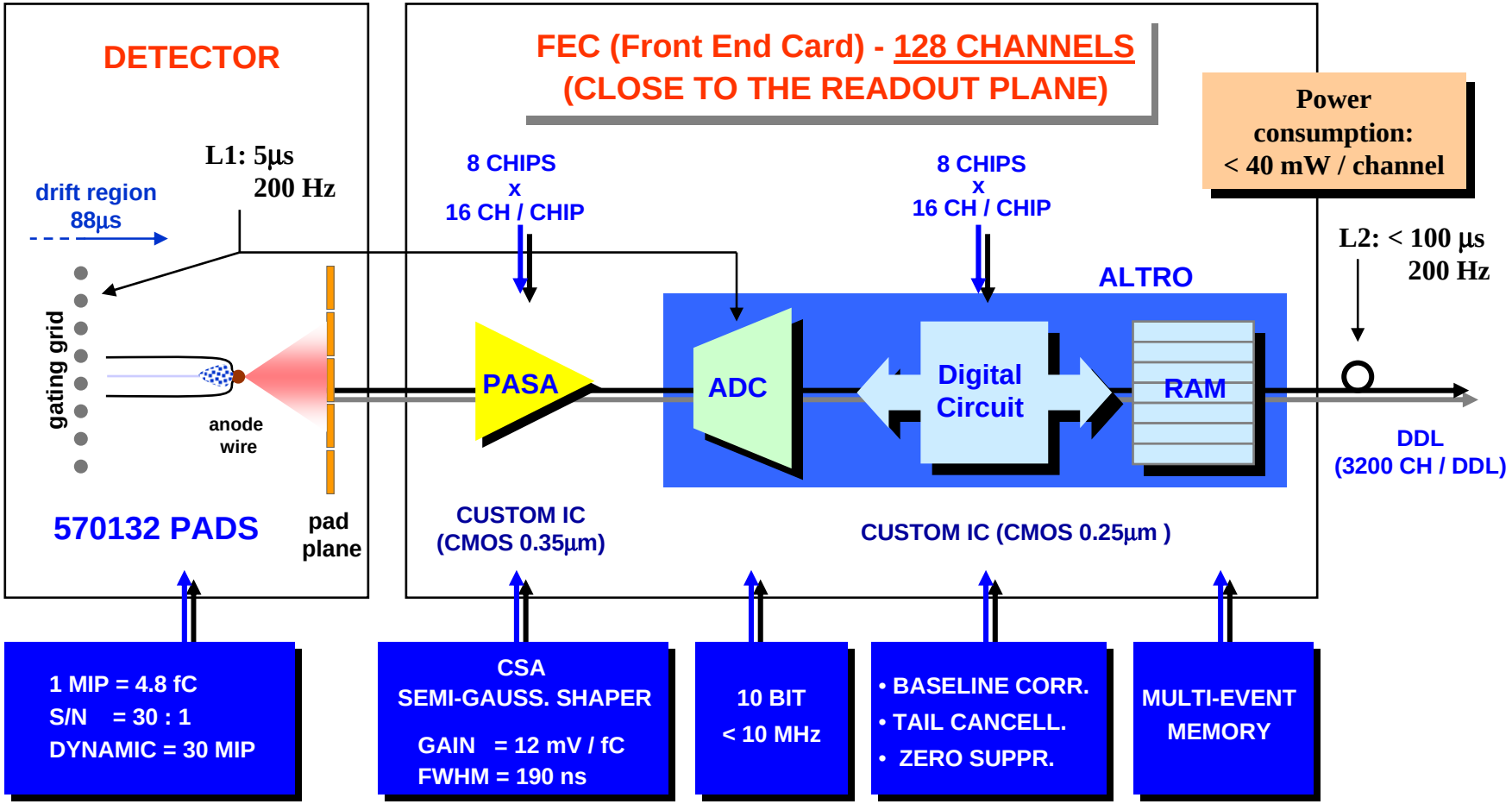
OUTLINE

R&D on the readout electronics for the LC TPC

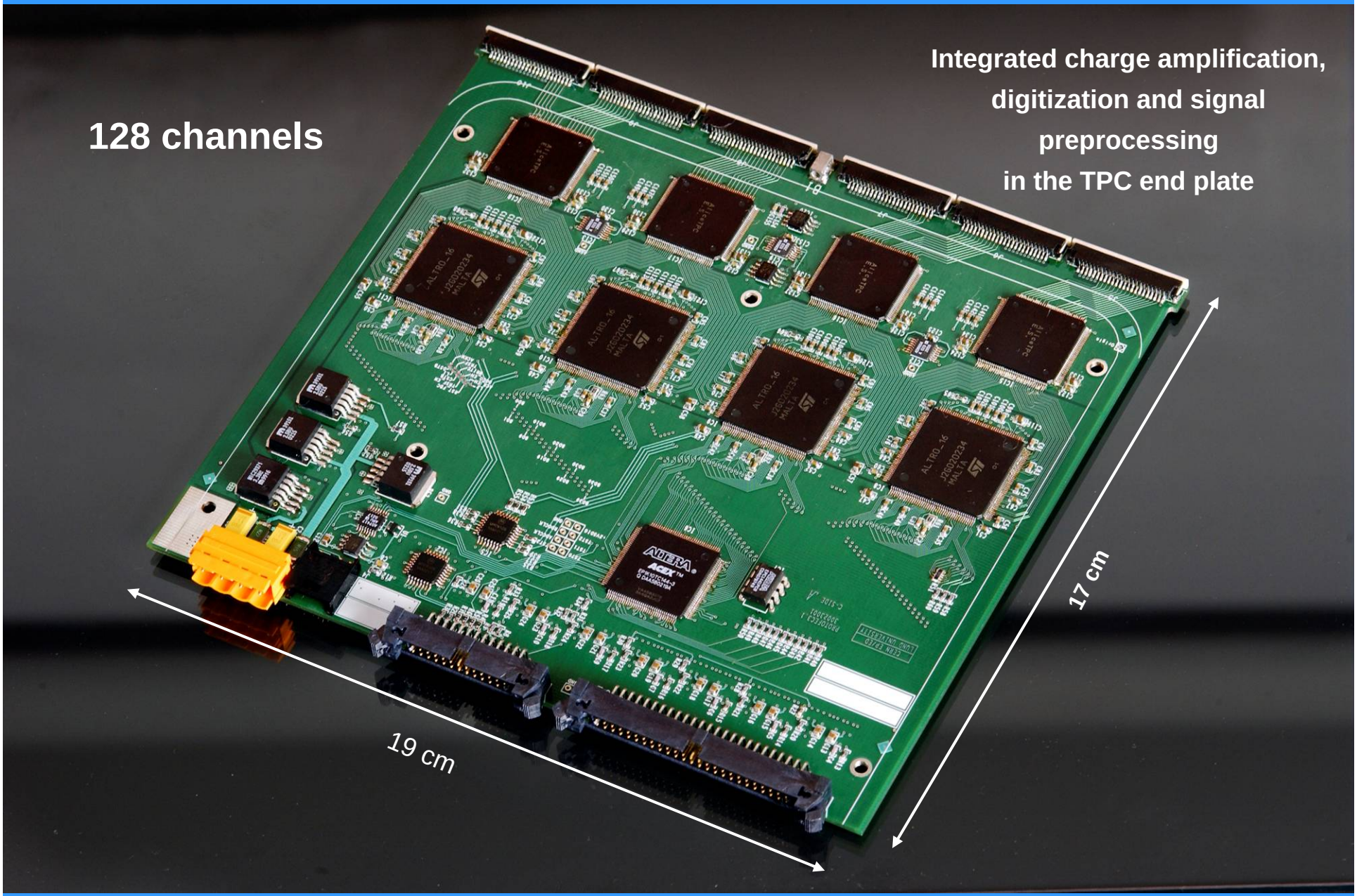
- Alice TPC Readout - MWPC
- General Purpose Charge Readout Chip
- Prototype Submission of the Analog Front End
- Multi Rate ADC
- Project Milestones
- Next Steps

Alice TPC – MWPC Readout

Front End Electronics Architecture



ALICE TPC Front End Card



Motivations & Specifications 1/2

- Requirements of the front-end and readout electronics for High Energy Physics Experiments:

  low power, high speed, high density, low mass, radiation tolerance

- These requirements can only be met by highly integrated systems implemented with very deep submicron CMOS technologies.

- The volumes of ICs required for a typical HEP detector remain low <1Mch

- Non Recursive Engineering (NRE) costs are more and more dominant for high energy physics.

- Development of *standard* chips capable of handling a wide range of high energy physics applications, in order to warrant the NRE expenditure.

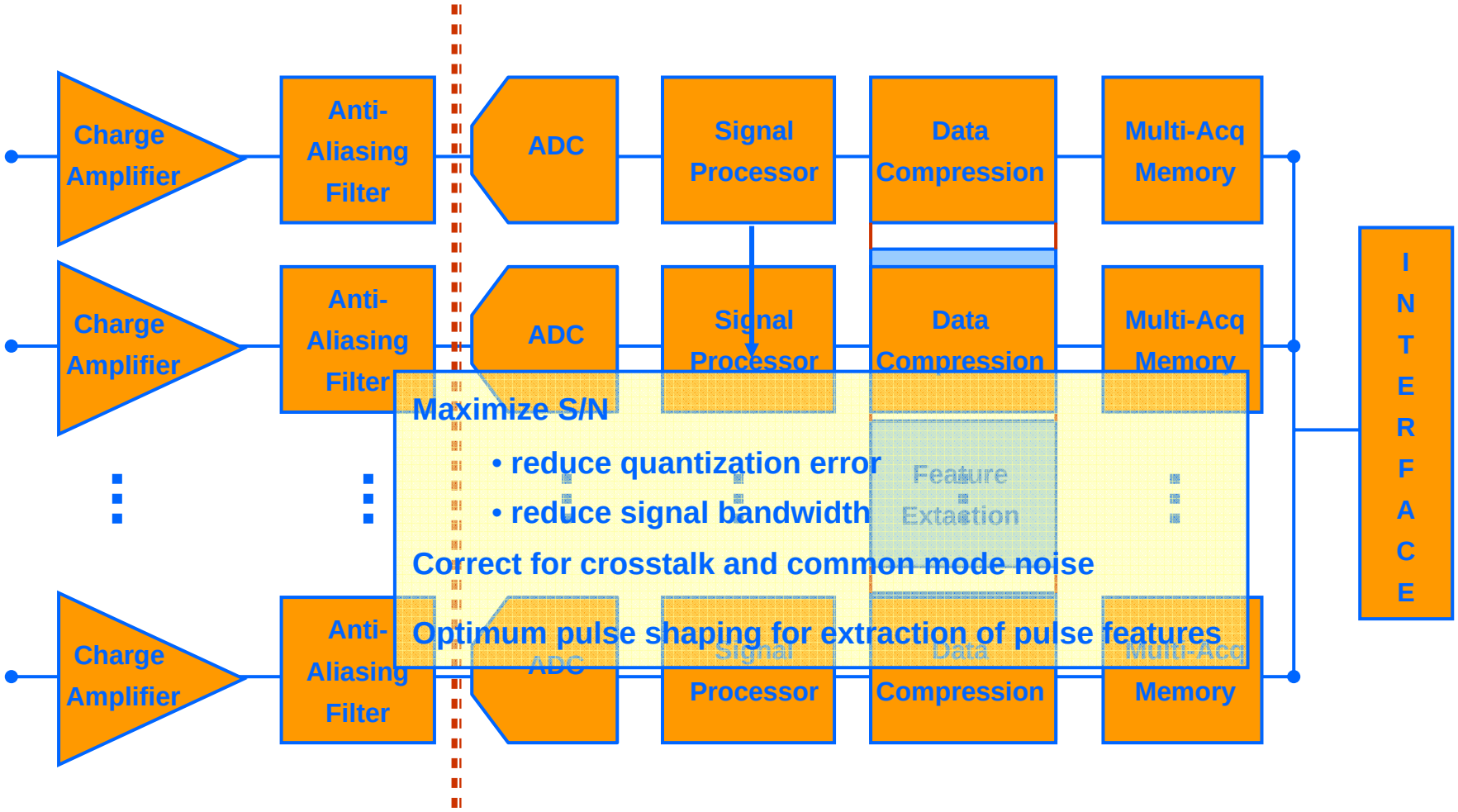
- Likely this polyvalence will be obtained through an increased level of programmability.

Motivations & Specifications 2/2

A general purpose charge readout chip

- ✓ number of channels: 32 or 64
- ✓ programmable charge amplifier:
  - sensitive to a charge in the range: ~10^2 - ~10^7 electrons
  - Input capacitance: 0.1pF to 10pF
  - Peaking time: 20ns – 100ns
- ✓ high-speed high-resolution A/D converter:
  - sampling rate in the range 40MHz - 160MHz;
- ✓ programmable digital filter for noise reduction and signal interpolation;
- ✓ a signal processor for the extraction and compression of the signal information (charge and time of occurrence).

Charge Readout Chip Block Diagram



Project Milestones

- Milestone I (Q1 2007) ⇒ Programmable Charge Amplifier (prototype)
  - 16 channel charge amplifier + anti-aliasing filter
- Milestone II (Q2 2007) ⇒ 10-bit multi-rate ADC (prototype)
  - 4-channel 10-bit 40-MHz ADC. The circuit can be operated as a 4-channel 40-MHz ADC or single-channel 160-MHz ADC
- Milestone III (Q2 2008) ⇒ Charge Readout Chip (prototype)
  - This circuit incorporates 32 (or 64) channels.
- Milestone IV (Q2 2009) ⇒ Charge Readout Chip (final version)

Low-noise Amplifier (CMOS 0.13μm)

Improved ENC

- ✓ Increased gm (Ideally approx. 20% per CMOS Generation)

➢ Low Supply Voltage limits SNR

- ✓ Smaller Dynamic Range
  - Rail to Rail Design
  - Invest Power to improve SNR
  - Big Capacitors
  - Design Shaping Circuit for Low Noise

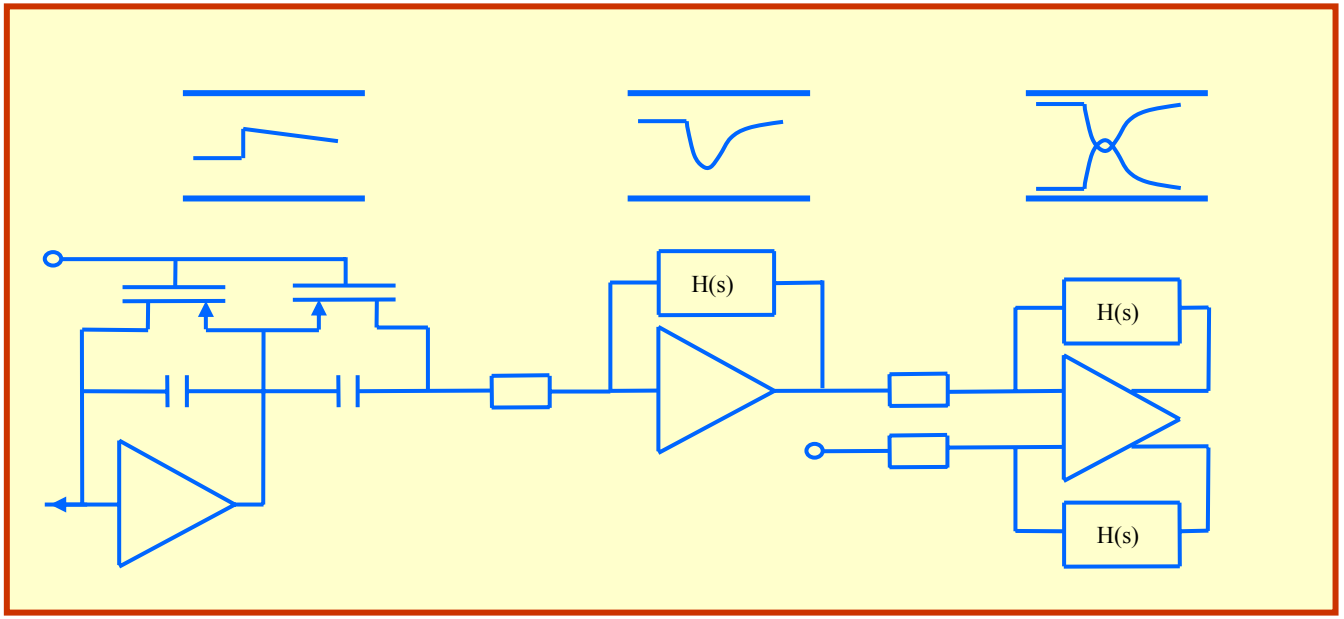
➢ Reduced Gate Oxide Thickness

- ✓ Gate Tunneling Current
- ✓ Radiation Tolerance

➢ Short Channel Effects

- ✓ Hot Carrier Stress – Reliability, Noise
- ✓ Velocity Saturation

Prototype Architecture



- PASA – Channel Architecture
  - Single Ended Charge Sensitive Preamplifier
  - Nonlinear Pole Zero Cancellation
  - 2 Shaping Amplifiers
  - Fully differential Rail to Rail Output Amplifier
    - Driving Capability of 30 pF
  - Optimized for one Signal Polarity

Programmable Charge Amplifier

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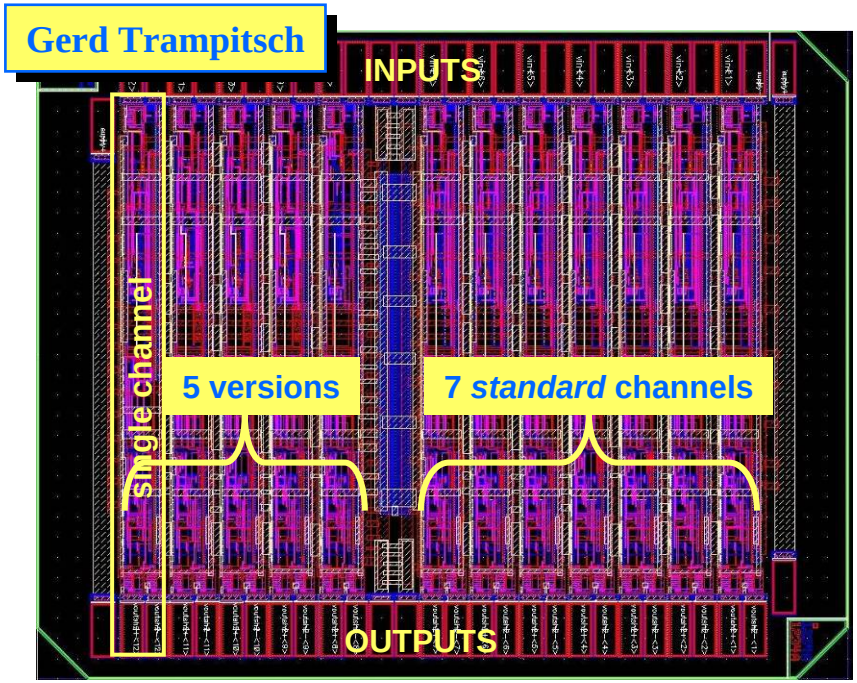


Production Engineering Data

- 12- channel 4th order CSA
- various architectures (classical folded cascode, novel rail-to-rail amplifier)
- process: IBM CMOS 0.13 μm
- area: 3 mm²
- 1.5 V single supply
- Package: CQFP 144
- MPR samples (40): Apr '06

Parameter	Requirement	Simulation	MPR Samples
Noise	< 500e	300e (10pF)	270e (10pF)
Conversion gain	10mV / fC	10mV / fC	9.5mV / fC
Peaking time (*standard*)	100ns	100ns	100ns
Non linearity	< 1%	< 0.35%	0.4%
Crosstalk	<0.3%		< 0.3%
Dynamic range	> 2000	3300	4600
Power consumption	< 20mW	10mW / ch	10mW / ch (30pF cl)

Programmable Charge Amplifier

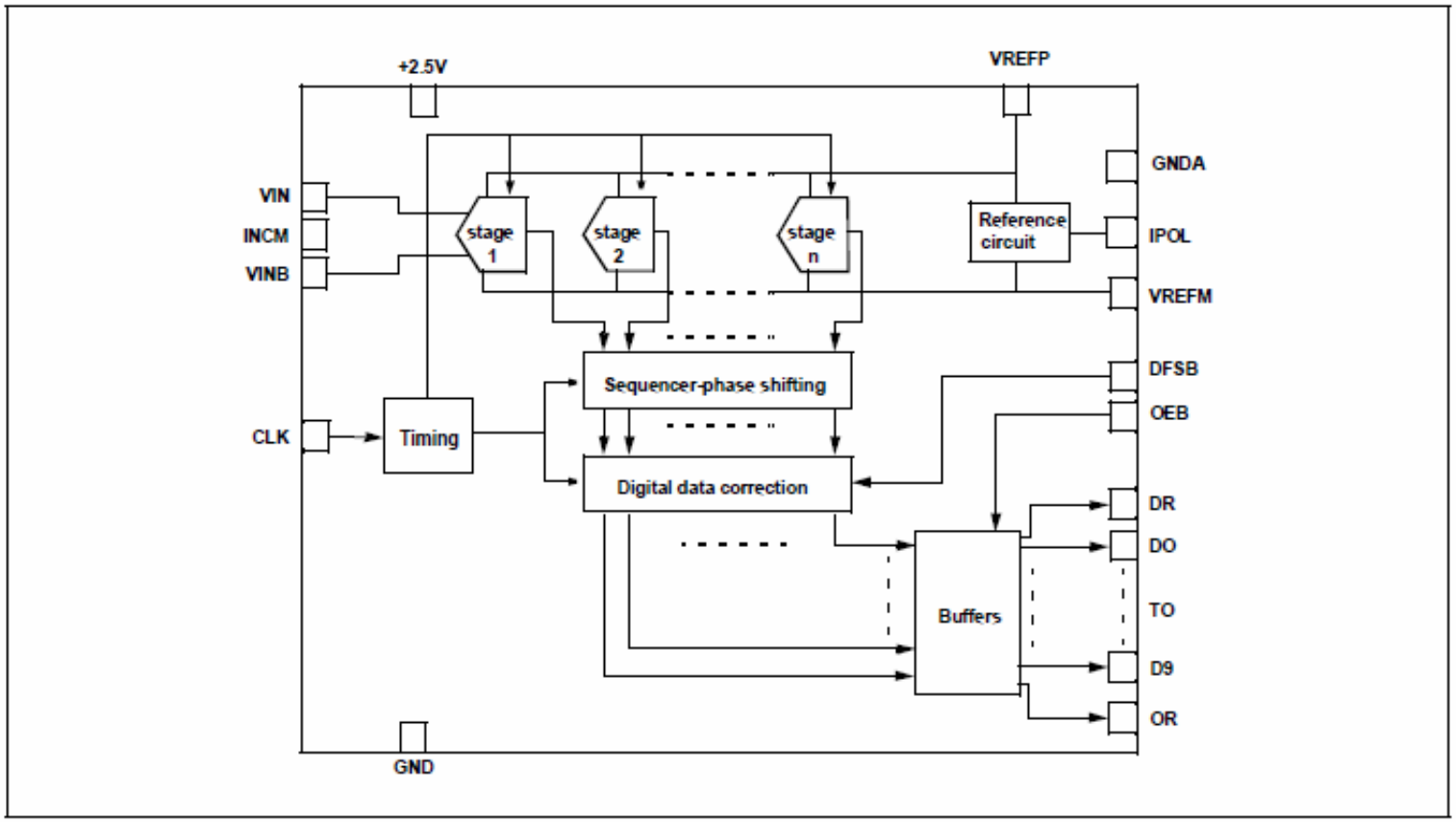
- **The CQFP 144 package has the same pin-count and similar pinout as the ALICE TPC PASA**
- **In the near future the new chip will be tested on a ALICE TPC FEC**

Next Step

- Milestone I (Q1 2007) ⇒ Programmable Charge Amplifier (prototype)
  - 16 channel charge amplifier + anti-aliasing filter
  - Programmable gain and peaking time (20ns – 100ns)
  - Both signal polarities
  - Design is in progress
  - Submission in Q1 2007

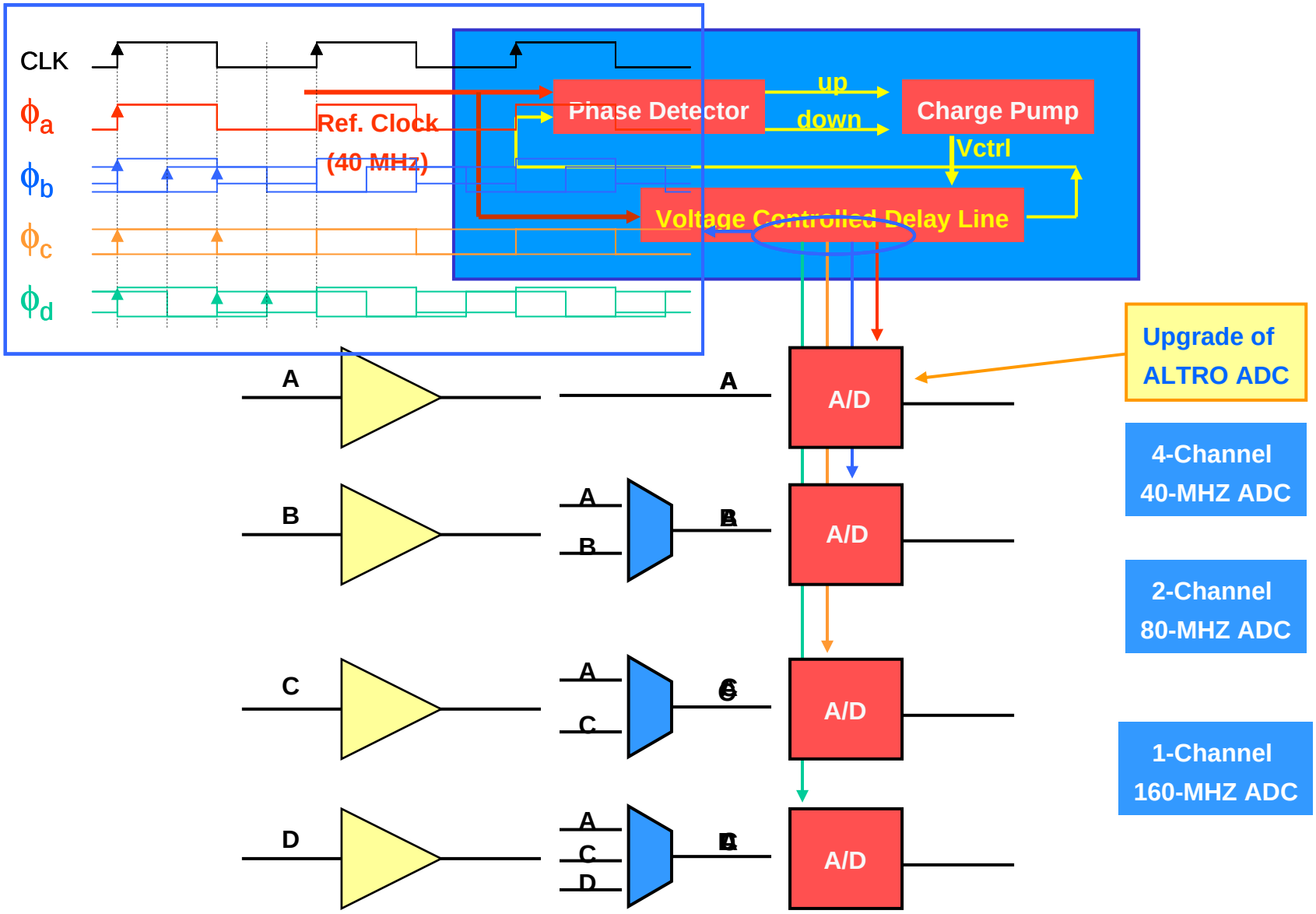
Pipelined ADC – 40 MHz

BLOCK DIAGRAM



- ALTRO – Pipelined ADC
  - Designed in 0.25 μm process
  - Design transferred to 0.13 μm – Upgrade of ALTRO ADC

Multi-Channel Time-Interleaved A/D Converter



Summary

- The development of a general purpose charge readout chip has started. This chip incorporates:
  - Programmable analogue front end
  - Multi-rate Analogue to Digital Converter
  - General purpose signal processor
- First prototype of the shaping amplifier in CMOS 0.13 µm
  - Submitted in December 2005
  - 40 samples of the MPWR successfully characterized in 2006
  - All circuit parameters meet the design specifications
  - The design and layout of a programmable gain and bandwidth amplifier is currently in progress and will be finished early next year
- Time interleaved Multi-Rate ADC
  - The basic building block was transferred to IBM 0.13 µm
  - Design is still in progress