CMOS Sensors for the JRA-1 Beam Telescope

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on behalf of the JRA-1 team

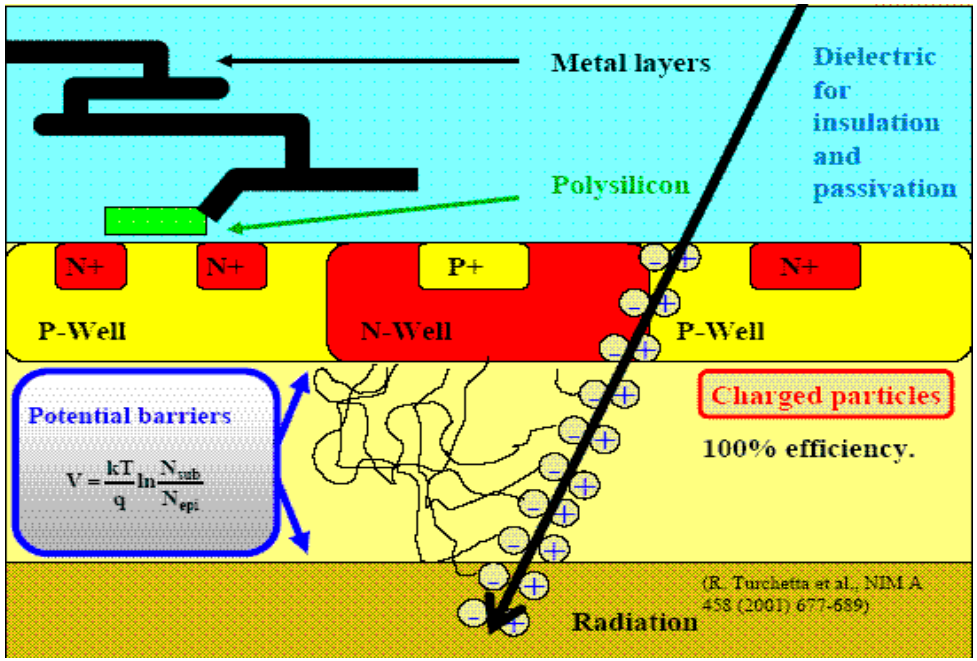
OUTLINE

- **Reminder on CMOS sensor technology**
- **Plans for JRA-1 beam telescope :**
  - **Demonstrator**
  - **Final set-up**
- **Sensors for the BT demonstrator :**
  - **Status of sensor fabrication**
  - **Expected performances (based on former prototypes)**
- **Sensors for the final BT set-up :**
  - **Status of development**
  - **Next steps**
- **Summary**

Main Features of the CMOS Sensor Technology

- p-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    Q $\sim$ 80 e-h / μm $\mapsto$ signal $\lesssim$ 1000 e^-
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
    with help of reflection on boundaries
    with p-well and substrate (high doping)

$\Rrightarrow$ thickness of epitaxial layer is of striking importance
$\rightarrowtail$ find the right fabrication process



- Specific advantages of CMOS sensors:
  - ◇ Signal processing μcircuits integrated on sensor substrate (system-on-chip) $\mapsto$ compact, flexible
  - ◇ Sensitive volume ($\sim$ epitaxial layer) is $\sim$ 10–15 μm thick $\longrightarrow$ thinning to $\gg$ 100 μm permitted
  - ◇ Standard, massive production, fabrication technology $\longrightarrow$ cheap, fast turn-over
  - ◇ Attractive balance between granularity, mat. budget, rad. tolerance, r.o. speed and power dissipation
  - ◇ May be operated at room temperature

- **BT demonstrator (Summer 2007)** $\rightarrowtail$ **specific application of well tested architecture :**
  - $<$ **1 cm**^{2} **sensors with analog output (and no integrated CDS)**
  - **read-out frequency** $\sim$ **1 kframe/s**
  - $\sim$ **2** μm **resolution in BT arms**
  - $\lesssim$ **1** μm **resolution on DUT surface**

- **Final BT (** $\lesssim$ **Summer 2009)** $\rightarrowtail$ **application of fast architecture under development :**
  - $\gtrsim$ **2 cm**^{2} **sensors with digitised output (after integrated CDS)**
  - **read-out frequency** $\sim$ **5 – 20 kframe/s**
  - $\sim$ **2 – 4.5** μm **resolution in BT arms**
  - $\lesssim$ **1** μm **resolution on DUT surface**

Real Size Sensors for the Beam Telescope Demonstrator

AMS 0.35 OPTO engineering run (submitted end of June):

≒ 2 + 4 wafers (8" ⇛ ∼ 50 reticles/wafer) ≒ 2 epitaxy thicknesses : ∼ 11 and 16 (?) μm

◇ triggered by MIMO★-3 (= MIMOSA-20) fabrication :

200 kpixels, ∼ 2 cm^2, 2 // outputs, $t_{r.o.} \lesssim$ 4 ms

◇ total cost ∼ 100 keuros (foundry) + 10 keuros (dicing & thinning)

+ 10 – 20 keuros (steering & r.o. specific PCB)

◇ includes 8 other chips :

✳ MIMOSA-16 : fast col. // architecture ⟶ final BT arms

✳ MIMOSA-17 (MIMO★-3M) : 0.8 x 0.8 cm^2, rad.tol., 800 μs

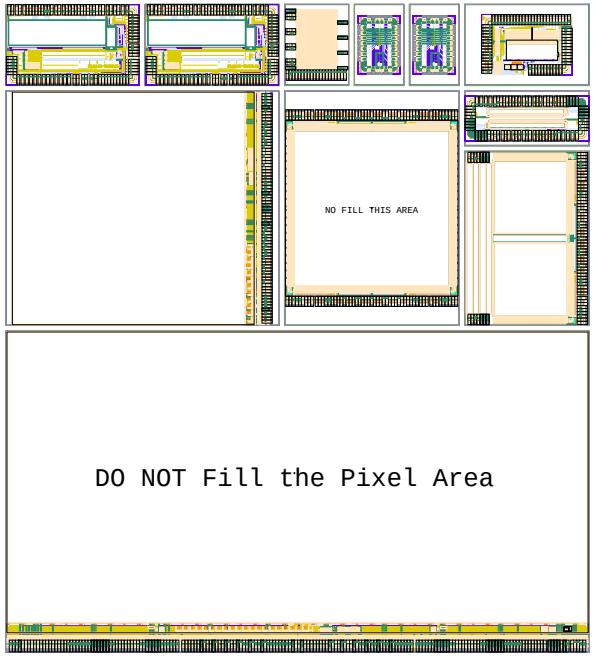
↪ demonstrator BT arms

✳ MIMOSA-18 (IMAGER) : precision $\lesssim$ 1 μm

↪ sub-micron resolution on DUT surface

✳ Flash-ADC, amplification micro-circuits, etc.

↪ Final BT arms



< ∼ 20 mm >

Time line :

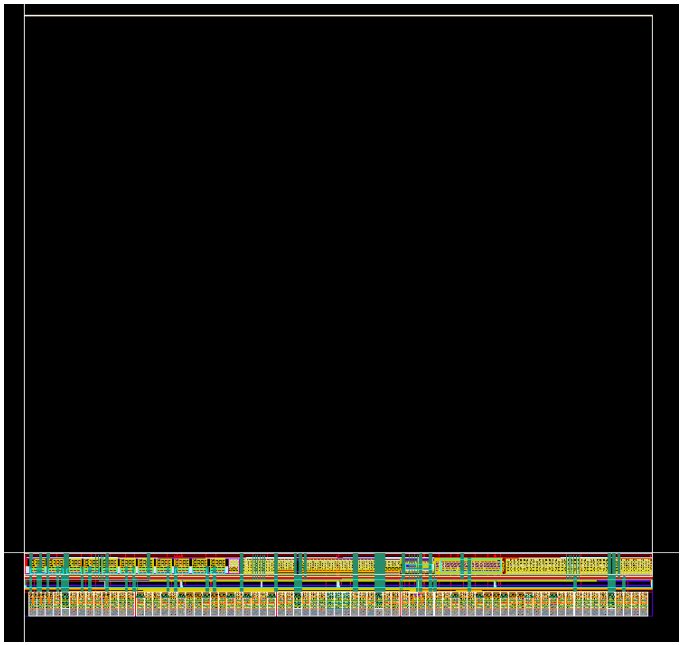
◇ 2 wafers back from foundry to CMP ⟼ available (diced) in Strasbourg by the end of this week

◇ first test results by end of 2006 : in particular fabrication yield,

2007 : assessment of chip performances, specific performances of ∼ 16 μm epitaxy

- **Will equip EUDET telescope demonstrator (e.g. 2 arms of 3 planes)**

  ⟼ commissionning in Summer 2007 at DESY



- **Medium size copy of STAR final sensor prototype :**

  (65 000 pixels instead of 205 000)

  ※ manufactured in AMS 0.35 μm OPTO techno.

  with $\gtrsim$ 11 μm and $\sim$ 16 μm epitaxial thickness

  ⟼ tests foreseen at DESY, INFN, IPHC early 2007

  ※ ionising rad. hard pixel design (validated with MIMOSA-11/-14)

  ※ 4 matrices of 64 x 256 pixels (30 μm pitch) treated in //

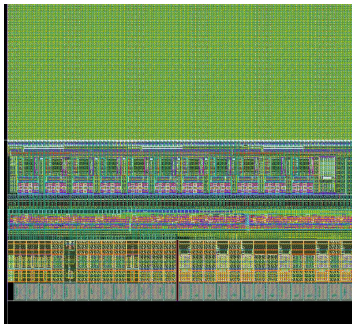
  ⟼ active area of $\sim$ 8 x 8 mm^2

  ※ 4 parallel analog outputs at 10 (or 20) MHz

  ⟼ frame r.o. time = 1.6 ms (or 800 μs)

  ※ integrated JTAG logic for steering

  ※ works at room temperature



High Resolution Sensor = MIMOSA-18

- **May equip DUT surface $\rightarrowtail$ provide high resol. despite mult. scattering**

  $\longmapsto$ commissionning in Summer 2007 at DESY (?)

- **Design close to MIMOSA-17 with smaller pitch :**

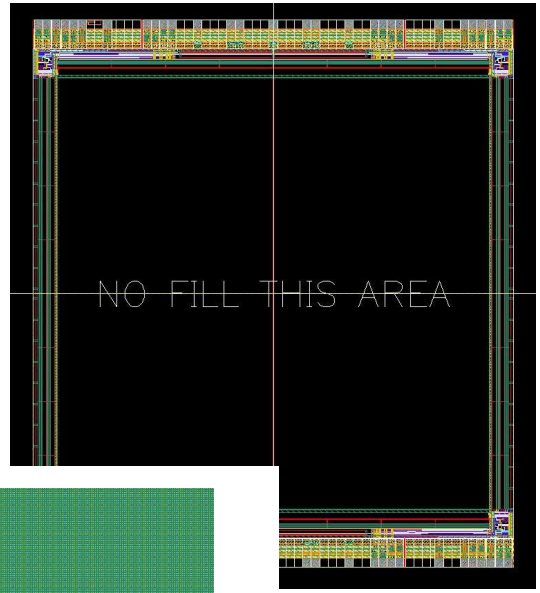
  (260 000 pixels instead of 65 000)

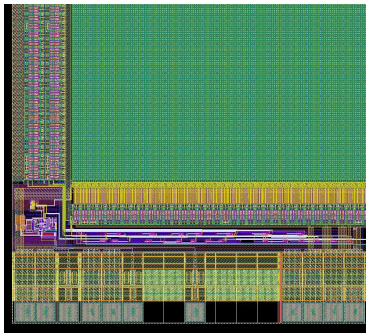
  ⁂ **manufactured in AMS 0.35 μm OPTO techno.**
  with $\gtrsim$ 11 μm and $\sim$ 16 μm epitaxial thickness
  $\longmapsto$ tests foreseen at IPHC $\gtrsim$ Nov. '06

  ⁂ **4 matrices of 256 x 256 pixels (10 μm pitch) treated in //**
  $\longmapsto$ active area of $\sim$ 5 x 5 mm^2

  ⁂ **4 parallel analog outputs at 10 (or 20) MHz**
  $\longmapsto$ frame r.o. time = 6.4 ms (or 3.2 ms)

  ⁂ **works at room temperature**



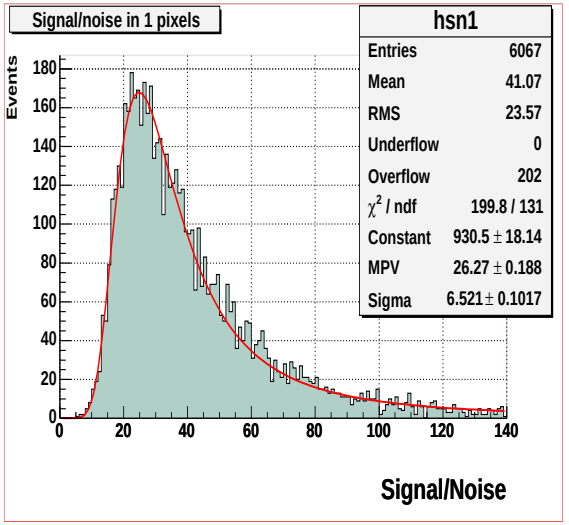


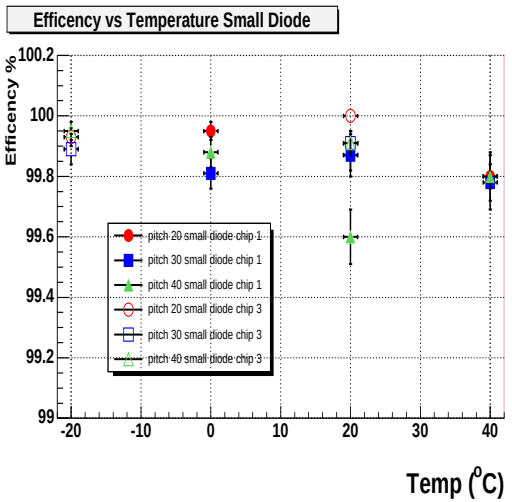
Established Performances of AMS-0.35 OPTO Technology

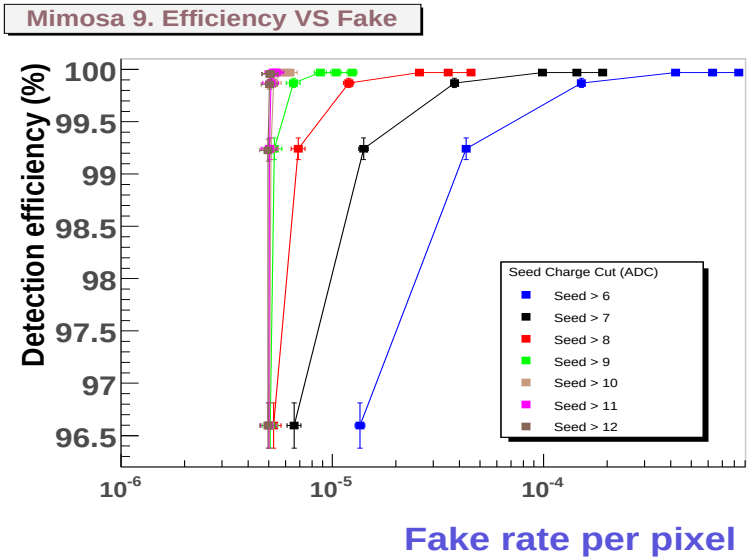
AMS 0.35 OPTO Performances : Detection Efficiency

Several MIMOSA chips tested on H.E. beams (SPS, DESY) $\mapsto$ well established performances :

- **Best performing technology: AMS 0.35 μm OPTO**
  (11–12 μm epitaxy $\rightarrowtail$ "20 μm" option tests in Fall'06)
- **N $\sim$ 10 e$^-$ $\mapsto$ S/N $\gtrsim$ 20 – 30 (MPV) $\Rrightarrow$ ϵ_{det} $\gtrsim$ 99.5 %**
- **T$_{oper.}$ $\gtrsim$ 40 °C**
- **Macroscopic sensors : MIMOSA-5 ($\sim$ 3.5 cm^2; 1 Mpix)**
  $\rightarrowtail$ MIMOSA-17 = new generation for EUDET BT







Efficiency vs rate of fake clusters :

- **vary cut on seed pixel : 6 $\rightarrowtail$ 12 ADC units ($\approxeq$ 4 – 8 N)**
- **vary cut on Σ of Q(crown) : 0, 3, 4, 9, 13, 17 ADC units**

$\Rrightarrow$ ϵ_{det} $\sim$ 99.9 % for fake rate $\sim 10^{-5}$

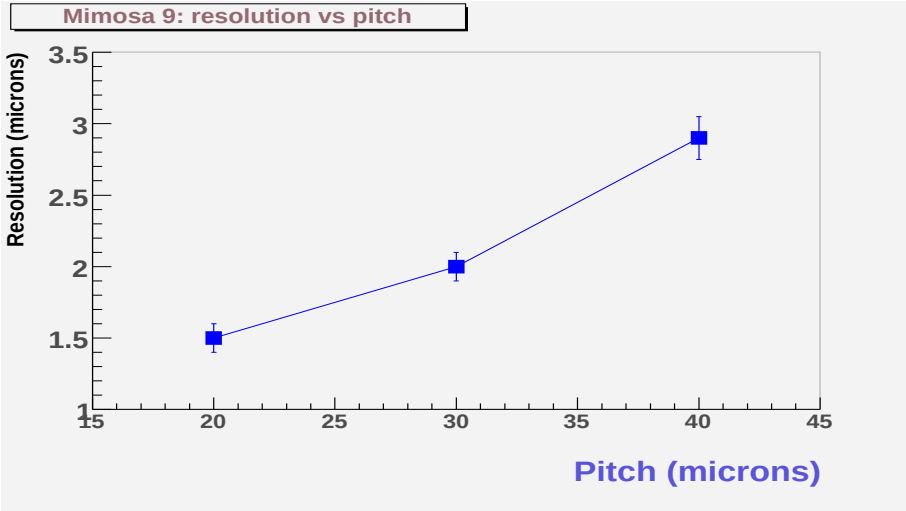
$\hookrightarrow$ track reconstruction ambiguïties $\sim$ 0

data rate from electronic noise $\sim$ 0

AMS-0.35 OPTO Perfomances : Spatial Resolution

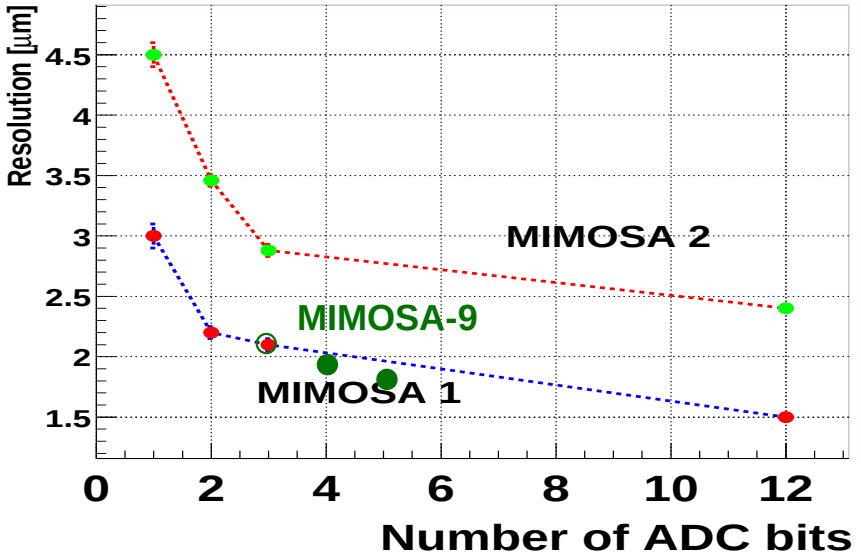
Single point resolution versus pixel pitch:

- clusters reconstructed with eta-function, exploiting charge sharing between pixels
- $\sigma_{sp} \sim 1.5\ \mu m$ (20 μm pitch)
  - $\longmapsto \sigma_{sp} \lesssim 2\ \mu m$ (30 μm pitch)
- obtained with signal charge encoded on 12 bits



σ_{sp} dependence on ADC granularity:

- minimise number of ADC bits
  - $\longmapsto$ minimise dimensions, $t_{r.o.}$ & P_{diss}
- effect simulated on real MIMOSA data
  (20 μm pitch ; 120 GeV/c π^- beam)



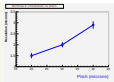
▷▷ $\sigma_{sp} < 2\ \mu m$ (4 bits) $\longmapsto$ 1.7–1.6 μm (5 bits)
(MIMOSA-9 : 20 μm pitch; T= + 20°C)

- Warning : results based on simple pixel (N $\lesssim$ 10 e^- ENC)
  - $\Rightarrow$ rad. tol. pixel integrating CDS (N $\lesssim$ 15 e^- ENC) not yet evaluated

- Numerous studies performed with X-Rays (10 keV), $\gamma(^{60}\text{Co})$, e^- (9.4 MeV), n ($\sim$ 1 MeV)
- Sensor radiation tolerance depends on fabrication techno., pixel design, T, $t_{r.o.}$, ...
- DESY beam (e.g. 10^4 e^-/cm^2/s) :
  - Integrated dose : $\sim$ 3 kRad / yr
  - Fluence : $\sim 10^{10}$ n_{eq} / cm^2 / yr
- Demonstrated radiation tolerance at room temperature :
  - Integrated dose : $\gtrsim$ 100 kRad – 1 MRad
  - Fluence : $\sim 10^{12}$ n_{eq} / cm^2

$\Rrightarrow$ Sensors are already adapted to long term running conditions at DESY

Sensors foreseen for the Ultimate Beam Telescope

  -

Essential Improvements Provided by Final Sensors

⇒ **Improvements focus on sensors equipping the arms (not DUT surface) :**

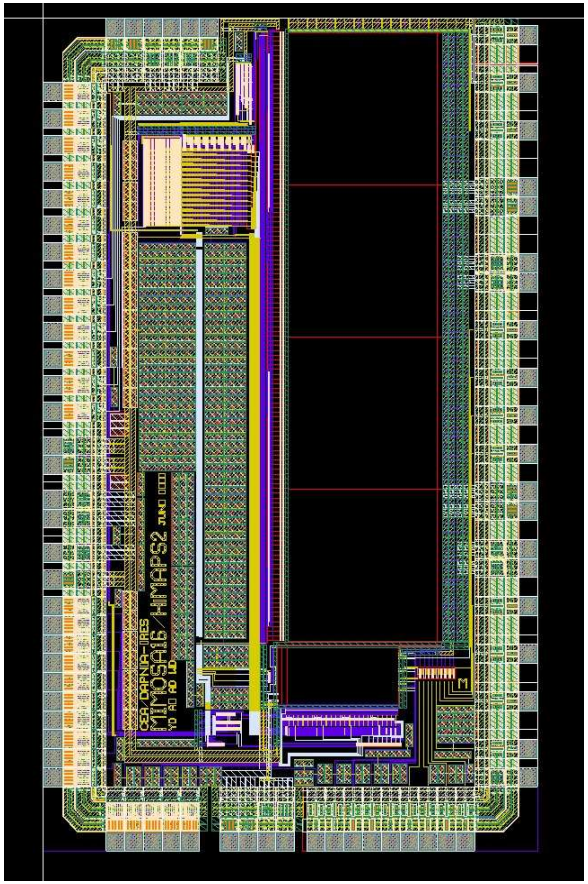
- **Increase of read-out speed by one order of magnitude :**
  - **Demonstrator provides frame read-out time of 1.6 ms (possibly 800 μs)**
  - **Final sensors will provide frame read-out time $\sim$ 100 μs (possibly $\sim$ 50 μs)**
- **Extension of sensitive area by factor 3.5 :**
  - **Demonstrator sensitive area : 7.68 x 7.68 mm^2**
  - **Final sensor sensitive area : 20.48 x 10.24 mm^2**
    - **$\longmapsto$ encompasses width of ILC-VD sensors**
- **Integrate several other improvements resulting from R&D progress**
  - **($\longmapsto$ signal amplification, data compression, etc.)**

- **3 micro-circuit components developed in parallel :**
  - **column // architecture with binary output**
  - **ADCs to be integrated at end of each column**
  - **∅ micro-circuits to be integrated downstream of each ADC**
- **Sharing of tasks :**
  - **Col. // architecture design : DAPNIA & IPHC**
  - **ADC designs : LPC-Clermont, LPSC-Grenoble, DAPNIA, IPHC**
  - **∅ micro-circuit design : IPHC (possibly others ...)**
  - **chips characterisation : IN2P3 (several labs), DAPNIA, DESY et al., INFN (several labs)**
- **2 design options under consideration :**
  - **Sensors with binary encoding of signal charge : most straightforward**
  - **Sensors with 4- or 5-bit ADC encoding : will provide twice better spatial resolution**

High Read-Out Speed Architecture

MIMOSA-16 design features :

- Fab. via STAR engin. run (Summer '06)
- AMS-0.35 OPTO translation of MIMOSA-8
  $\hookrightarrow \sim$ 11–16 μm epitaxy instead of $\lesssim$ 7 μm
- 32 // columns of 128 pixels (pitch: 25 μm)
- on-pixel CDS (repeated at end of each column)
- discriminator at end of each column
- 4 sub-arrays :
  - ⁂ 2 alike MIMOSA-8 (2 different pitches)
  - ⁂ 1 with ionising radiation tol. pixels
  - ⁂ 1 with enhanced in-pixel amplification
    (against noise of read-out chain)



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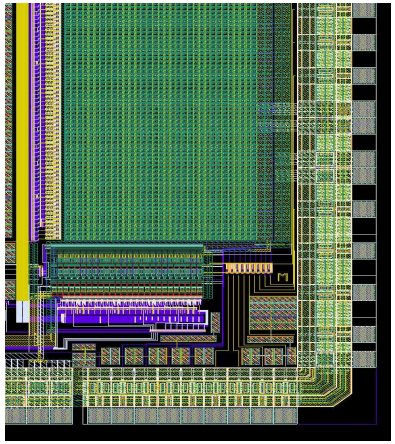


24 col. with discri.

Next steps :

- back from foundry $<$ end Oct. '06 $\longmapsto$ lab tests $\gtrsim$ Nov. '06 $\longmapsto$ beam tests $\gtrsim$ Summer 2007
- next generations :
  - ⁂ "large" prototype (320 columns of 256 pixels, 16 μm pitch, integrated $\varnothing$ micro-circuits) ???
  - ⁂ small prototypes with ADCs replacing discriminators

- **Several different ADC architectures under development at IN2P3 and DAPNIA**
  - **LPCC (Clermont) : flash 4+1.5-bit ADC $\mapsto$ 1st proto tested, 2nd proto back from foundry**
  - **LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5-bit ADC $\mapsto$ 1st proto tested, 2nd proto under test**
  - **DAPNIA (Saclay) : Ampli + SAR (4- and) 5-bit ADC $\mapsto$ 1st proto under test**
  - **IPHC (Strasbourg) : SAR 4-bit and Wilkinson 5-bit ADCs: 1st proto to be submitted end Oct. '06**

    ►►► **Present outcome of development :**

    ※ **Dominant differences between architectures : $\sim$ factor 2 in power & speed**

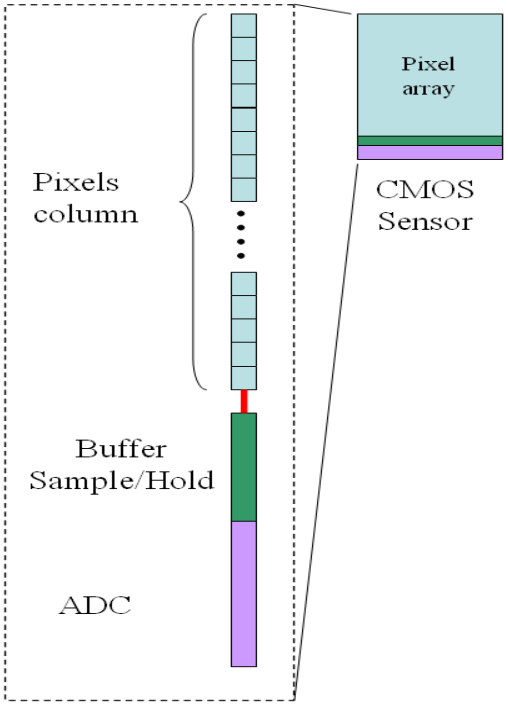
    ※ **Modest differences expected in single point resolution**

- **Next steps :**
  - **Final ADC designs expected to come out in 2007**
  - **Submission of 1st col. // pixel array proto equipped with ADCs & $\varnothing \gtrsim$ end 2007**

Prospect on Development of Final Sensors

Baseline Architecture with Integrated ADCs

- **Geometry :**
  - 1024 columns of 512 pixels
  - 20 μm pitch ($\longrightarrow \sigma_{sp} < 2.5\ \mu m$)
  - Sensitive area = 20.48 x 10.24 mm^2

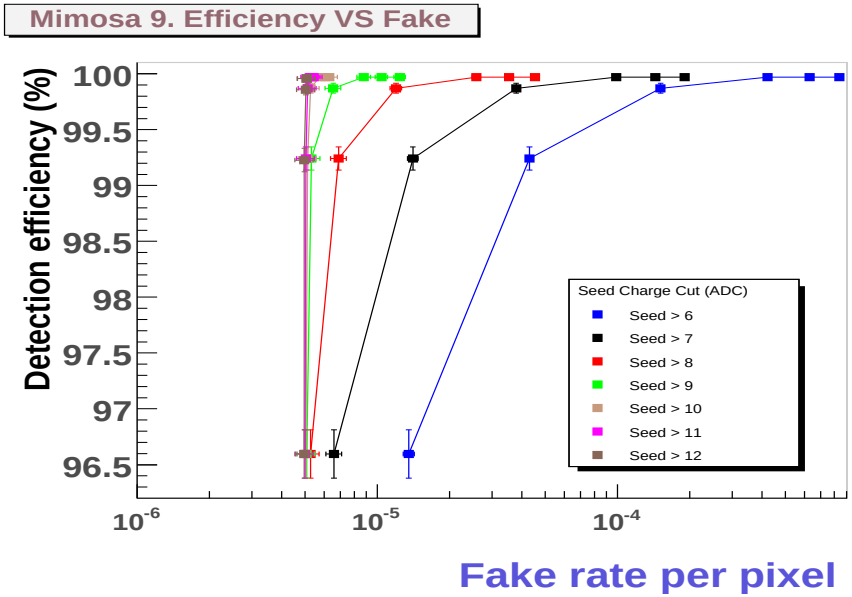


- **Functionnalities :**
  - pixels with integrated CDS (possibly repeated at end of column)
  - sensor with integrated 4-/5-bit ADC
    - ▷ ADC possibly preceded by discri. $\longrightarrow$ 1 ADC for 8 - 16 col. ?
  - $\emptyset$ micro-circuit integrated downstream (?) of ADCs

- **Read-out speed (adapted to DESY beam) :**
  - default $\mathbf{t_{r.o.}}$ = 512 lines / 5 MHz $\sim$ 100 μs
  - flexible clock frequency : e.g. 1 – 10 MHz $\longrightarrow$ $\mathbf{t_{r.o.}} \sim$ 500 – 50 μs

Expected Data Rate per Sensor

- **Baseline assumptions :**
  - sensor made of 1024 col. of 512 pixels $\longmapsto \sim 5{\cdot}10^5$ pixels / frame
  - $t_{r.o.}$ = 100 μs $\longmapsto$ 10 kfps (can be twice more or twice less)
  - $\lesssim$ 5 hits / frame
  - noisy pixel rate $>$ threshold $\lesssim 10^{-4}$ $\longmapsto$
  - pixel data size = 2 Bytes
    (10 bits of address & 5 bits for charge)



- **Data rate from pixel noise :**
  - 50 pixels / frame $\longmapsto$ 1 MB/s

- **Data rate from beam particle hits :**
  - 5 hits of 9 pixels / frame $\longmapsto$ 1 MB/s

$\Rightarrow$ **Total $<$ 1 kB/frame $\longmapsto$ few MB/s only**

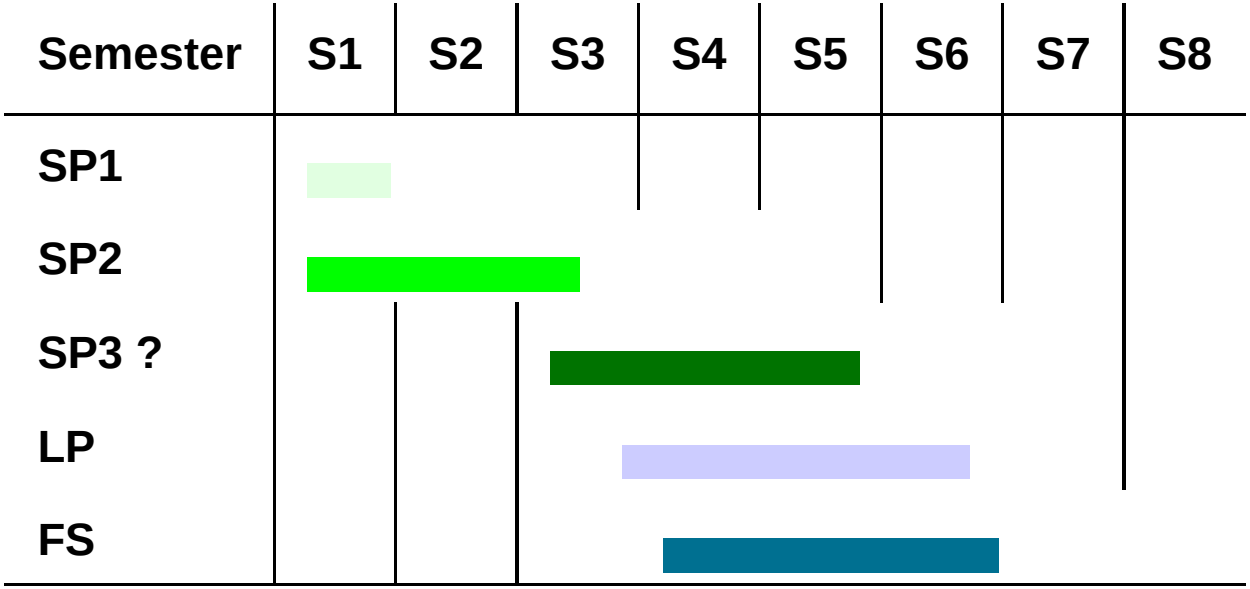
Simplified Architecture with Binary Output

- **Geometry :**
  - **1280 columns of 640 pixels**
  - **16 μm pitch ($\longrightarrow$ $\sigma_{sp} < 5\ \mu m$)**
  - **Sensitive area = 20.48 x 10.24 mm^2**

- **Functionnalities :**
  - **pixels with integrated CDS (possibly repeated at end of column)**
  - **column ended with integrated discriminator $\longrightarrow$ binary encoding of charge**
  - **$\emptyset$ micro-circuit integrated downstream of discriminators**

- **Read-out speed (adapted to DESY beams):**
  - **default $\mathbf{t_{r.o.}}$ = 640 lines / 6.4 MHz = 100 μs**
  - **flexible clock frequency : e.g. 1 – 10 MHz $\longrightarrow$ $\mathbf{t_{r.o.}}$ = 640 – 64 μs**

Provisionnal Time Line of Sensor Delivery



- **Sensor production based on 5 steps (perhaps only 4, i.e. SP3 included in LP) :**
  - **MIMOSA-8 $\equiv$ SP-1 : 25 μm pitch, epi $<$ 7 μm**
  - **MIMOSA-16 $\equiv$ SP-2 : 25 μm pitch, epi $\sim$ 11 or 16 μm, rad. tol.**
  - **M16+ $\equiv$ SP-3 : like SP-2 but integ. $\emptyset$, 20 μm pitch (ADC) or 16 μm pitch (binary)**
  - **M16++ $\equiv$ LP : like SP-3 but 320 col. of 256 pixels**
  - **M16+++ $\equiv$ FS : like LP but 1024 x 512 pixels (ADC) or 1280 x 640 pixels (binary)**

- **Sensors for BT demonstrator fabricated $\longmapsto$ based on already assessed architecture :**
  - **Arms : 8 x 8 mm^2 – 30 μm pitch – $\sim$ 1 kfps**
  - **DUT surface : 5 x 5 mm^2 – 10 μm pitch – $\sim$ 200 fps**
  - **Analog outputs**

    $\longmapsto$ Characterisation will start in Nov.-Dec. '06

    $\longmapsto$ Available for mounting early Spring '07

- **Development of final sensors for BT arm in progress $\longmapsto$ O(10) faster and 3.5 times larger :**
  - **Arms : 20 x 10 mm^2 – $\sim$ 15 - 20 μm pitch – $\sim$ 10 kfps**
  - **Sparsified and digitised signals**
  - **Column // architecture with integrated CDS and discriminator validated**
  - **Compact & fast ADCs under devt $\longmapsto$ expected to converge in 2007**
  - **$\varnothing$ micro-circuits expected to converge by Summer '08**

    $\longmapsto$ Final sensors available by 2009

- **Development of sensors will continue to benefit from synergy with other applications**