EUDET JRA1 Meeting, Munich October 2006 USB board Firmware & Software Development status



USB Imager Board



OUTLINE

- USB board firmware validation for EUDET
- **USB board software validation for EUDET**
- ▶ IPHC Telescope DAQ upgrade status
- ► Analogue signal integrity for MimoTel readout ...



MimoStar 2



USB board firmware upgrade has been done

- ► For EUDET project
- ▶ For the upgrade of our beam telescope DAQ from VME to USB

New features

- ► On board CDS calculation
 - ▶ Reduce event size Increase event rate Mandatory to reach 40 Events/s with 6 Mi*3M
- ► Trigger handling
 - **•** Reject trigger on first frame, read one more frame after trigger
- Multiple boards synchronization
 - ▶ In order to synchronize 6 MAPS planes readout

Without these new features the USB board would be useless for EUDET

Firmware validation : CDS on board

Status

- ▶ Implemented on board : 12 bits signed CDS = Frame 1 Frame 0 (Hit < 0)
- **•** Tested with a marker injected in analogue input to simulate a hit
- **Tested with real data : Mimo*2 + Analysis = same results as with RAW data mode**

It works - No problem seen

Availability

- **DAQ software and board firmware are ready**
- **•** Upgrade of data readout libraries for analysis software (Labview & Mathematica) done
- ► Upgrade of Labview analysis software done

To Do List ... work still to be done

Documentation

A dynamic switch CDS / RAW in DAQ SW monitoring to check base line level while taking data ...

Firmware validation : Trigger handling

Status

- ▶ Implemented on board firmware CDS sign handling in DAQ software (use trigger address)
- **•** Tested with 2 analogue markers : Trigger position & Hit simulation (Hit After and Before trigger)
- ▶ We have tried to perform exhaustive tests ... one bug discovered, but nothing critical

It works - No major problem seen

Availability & Limitations

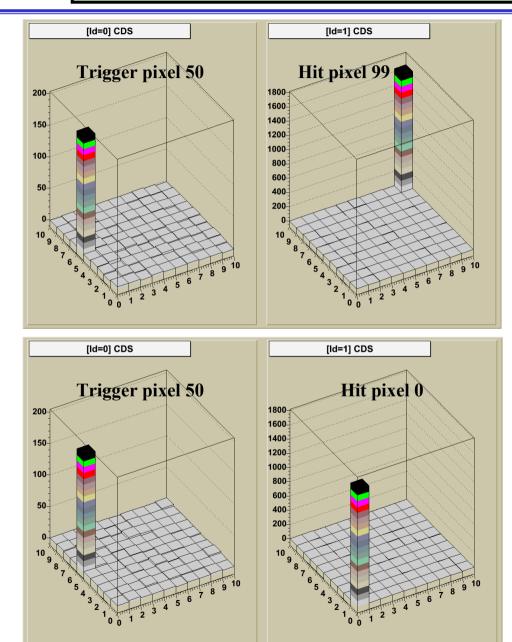
- **DAQ software & Preliminary version of board firmware are ready**
- ▶ Minimum of two veto frames between SYNC and trigger (will increase dead time)
- Mimosa matrix size must be an even number of pixels (it should not be a problem)

To Do List ... work still to be done

Documentation

▶ Fix bug : trigger on last pixel not seen – side effect (just need time to correct FW and check)

Firmware validation : Trigger test



Tested with short frame 100 pixels @ 2,5 Mhz

It's easier to check than with 8 k pixels ...

- **•** Trigger position on left matrix
- ▶ Hit position on right matrix
- ► CDS data = Frame (n) Frame (n-1)

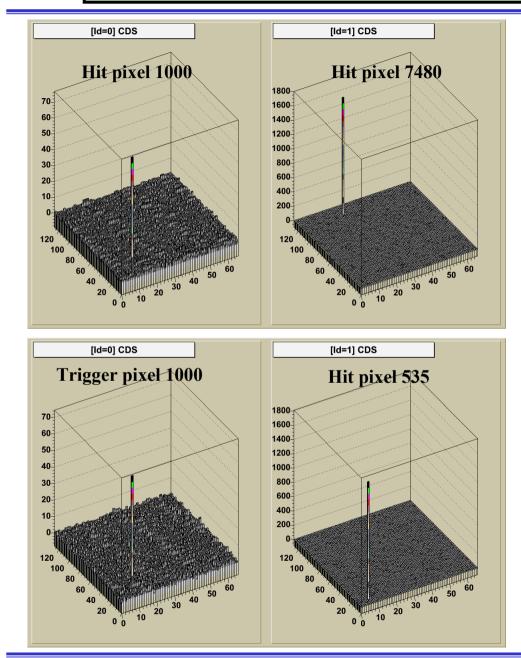
Test done

- **•** Trigger on Pixel 50 Frame 1
- ▶ Hit <u>after</u> trigger on Pixel 99 Frame 1
- ► Hit <u>before</u> trigger on Pixel 0 Frame 1

Result

- ► Hit is at the right position
- Hit sign has been corrected by software
 - ▶ Hit pixel 99 Signal = Fr(n-1) Fr(n) > 0
 - ▶ Hit pixel 0 Signal = Fr(n-1) Fr(n) < 0

Firmware validation : Real world test



Test with Mi*2 frame size - 8 k pixels @ 10 Mhz

- **•** Trigger position on left matrix
- Hit position on right matrix
- CDS data = Frame (n) Frame (n-1)

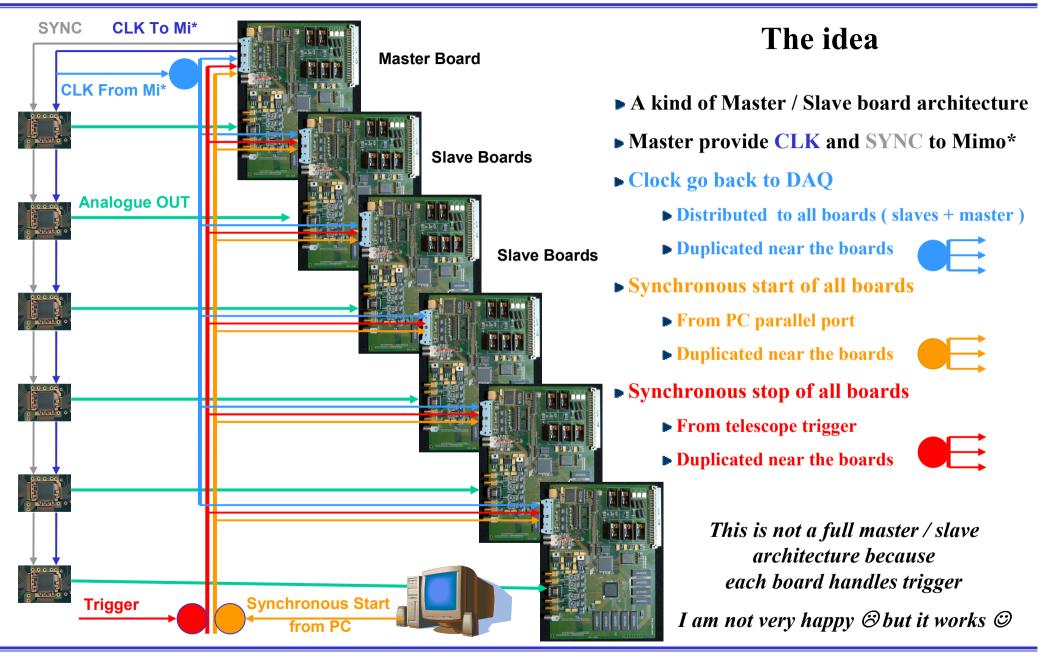
Test done

- **•** Trigger on Pixel 1000 Frame 1
- ► Hit <u>after</u> trigger on Pixel 7480 Frame 1
- ► Hit <u>before</u> trigger on Pixel 535 Frame 1

Result

- ▶ Hit is at the right position
- ► Hit sign has been corrected by software

Firmware validation : Boards synchronization



Firmware validation : Boards synchronization

Status

- Implemented on board firmware
- ▶ Test performed with 2 boards (Also tested with 6 boards, but not enough time for exhaustive tests)

It works - No problem seen

Availability

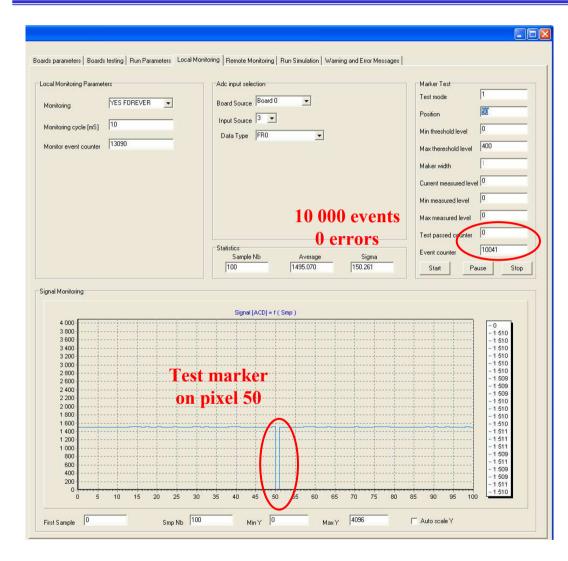
► DAQ software & board firmware are ready **Special HW** " is required to duplicate, synchronize signals ...



To Do List ... work still to be done

- ► Documentation
- Preliminary version of "Special HW" boards done by W DULINSKI

Firmware validation : Boards synchronization test



Test : 2 boards, 100 pixels frame @ 10 MHz We use "Marker Test" feature of DAQ GUI

- **•** The same marker is sent to two boards
- ▶ It MUST be at pixel 50 position
- We count when marker is at a different position

Result

- More than 10 000 events without error
- No error :
 - ▶ The marker is at right position
 - **•** The same position for the two boards

Firmware validation : Trigger handling with N boards

Status

- ▶ Nothing to implement on board firmware : duplicate trigger signal (synchronized to CLK)
- ▶ Tested with 2 boards (Also tested with 6 boards, but not enough time for exhaustive tests)

It works - No problem seen

Availability

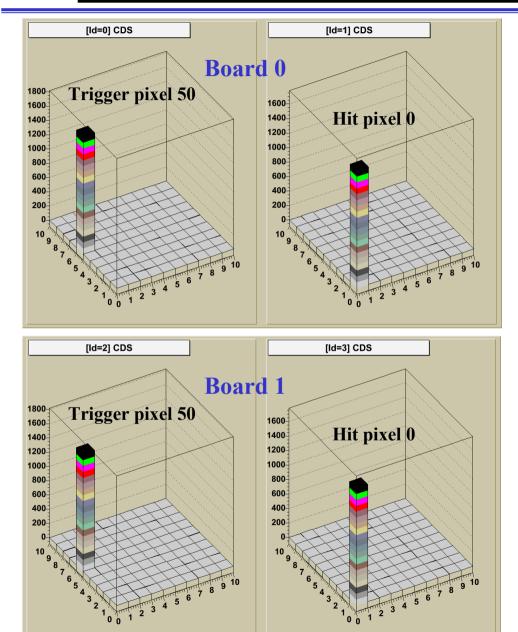
- ► DAQ software & board firmware are ready
- **" Special HW " is required to duplicate, synchronize signals ...**



To Do List ... work still to be done

- **Documentation**
- Preliminary version of "Special HW" boards done by W DULINSKI

Firmware validation : Trigger handling with N boards



Tested with 2 boards 100 pixels frame

- ► The same trigger & hit marker are sent to two boards
- **•** Trigger position on left matrix
- Hit position on right matrix
- **•** Top picture = Board 0 / Bottom picture = Board 1

Result

► Trigger and hit are at the same position on two boards

Firmware validation : Conclusion

The USB board firmware is ready for EUDET demonstrator

► CDS on board	: Ready & Tested
Trigger handling	: Ready & Tested
Multiple boards readout + Trigger handling	: Ready & Tested

We have tried to perform exhaustive tests and we have discovered no problem. But we can't say it's 100 % bug free, we only have done our best in the short time scale we have.

Availability ?

- **CDS on board can be useful for Mi*3M calibrations**
 - ► Firmware + DAQ Software + LabView Analysis + Doc => End of January 2007
- Trigger handling for DAQ integration
 - ▶ Very difficult to provide something before January 2007 (*I am also involved on others projects* ...)

How to do boards firmware upgrade?

▶ Send boards to Strasbourg at beginning of January 2007 ?

The goal

▶ Integration test with

- ▶ New board firmware (CDS, Trigger, Multiples boards synchronization)
- ▶ USB multi-threading readout of 6 boards (Demonstration of March 2006)
- ▶ IRQ handling with PC parallel port

► Why ?

- **•** To check if the whole architecture we have proposed is working
- **•** To measure maximal event rate in real conditions (should be close to 40 Hz)
- ▶ This test will help to avoid bad surprises in final demonstrator DAQ integration

► Results

- ▶ It has been done : Simulation of 6 Mi*3 readout, CDS on board, Trigger handling
- **•** Event rate is ~ 30 Hz : It's 25 % lower than simulation of March 2006 (40 Hz) because :
 - Trigger is rejected during 2 first veto frames and not only on first frame (due to current board FW limitation)
 - ► For trigger mode : CDS sign handling requires 1 more access per board to read trigger address _____ cost time

Software validation

Performances improvement

- Minimum veto frames number
 - **•** Requires a FW upgrade to allow trigger rejection only on first frame
 - ▶ It will be done for the demonstrator
- ▶ How to get back the time we loose to read trigger address ?
 - **Fast board control mode will help**
 - ▶ It uses // port signals instead of USB access to restart board after each event
 - ▶ It's developed on FW and SW sides, it will be ready for demonstrator
- Performances evaluation with fast board control
 - **•** Trigger happens at the beginning of first frame after veto => close to 40 Hz
 - ► Trigger happens at the end of first frame after veto => 37 Hz
 - ► Therefore realistic event rate will be 35 40 Hz for 6 MimoTel planes (Readout at 10 MHz)
- ▶ Performance evaluation of Mimosa 18 (Imager 512 x 512 pixels) DAQ
 - ▶ We can't use the same DAQ for MimoTel planes and Mimosa 18 => 2 DAQ as proposed in April 2006
 - Mimosa 18 DAQ will be the master (slowest one) and MimoTel DAQ the slave
 - ► Event rate ~ 12/15 Hz 1 USB board/plane ... ~ 18/24 Hz 2 boards ... ~ 20/30 Hz 4 boards (Clock 10/20 Mhz)

Development status of our beam telescope DAQ

Hybrid system (first step): Windows USB DAQ / Linux Monitoring

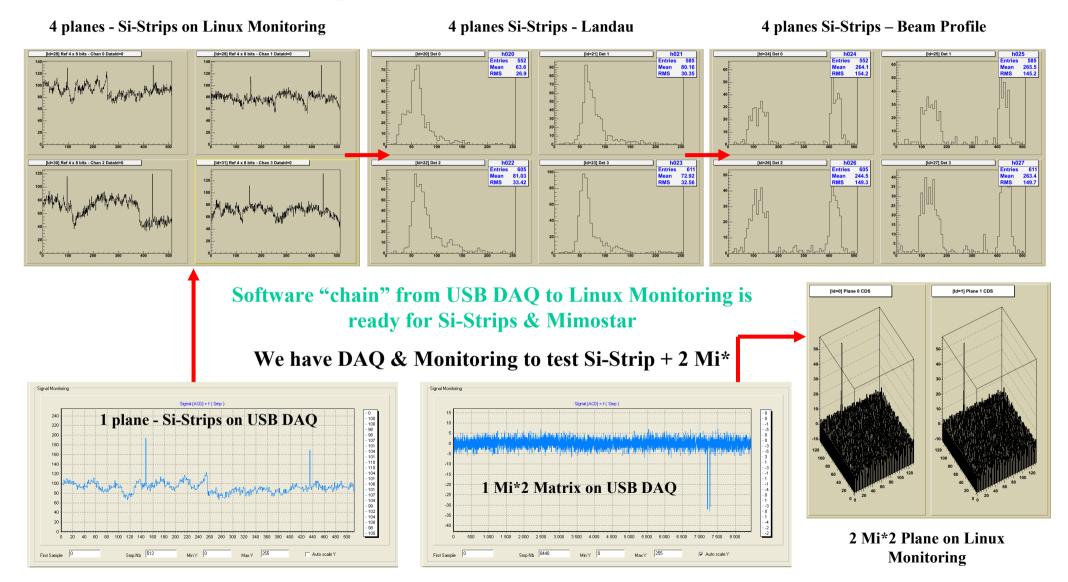
- Virtual mode implemented in Windows DAQ => Can run without boards
- **Run simulation implemented in Windows DAQ => Can replay an existing run**

This is very useful tools for whole DAQ chain development and debugging

- ▶ Interface to Linux monitoring for MAPS and Silicon Strips detectors (with RMP) is ready
- **Silicon Strips detectors control HW will be done in February 2007 (2 weeks)**
- ▶ Conclusion
 - ► Our telescope DAQ <u>for fix event size</u> IS " virtually " ready
 - ▶ We will have DAQ application to control 6 boards + JTAG application
 - **•** We will maintain and upgrade this software to follow USB board firmware upgrades

IPHC Telecope DAQ upgrade status

DAQ simulation – Si-Strips detector + 2 Mis*2 = Real software – Without hardware



IPHC Telescope DAQ upgrade status

What does it mean ?

- Windows DAQ for 6 MAPS plane is developed
- **Exhaustive tests will be done at IPHC**
- ▶ We have the tools (Monitoring) to integrate it in our Telescope
- ► A Beam Test will be possible with Si-Strip and 2 Mi* before June (Spring 2007?)

What can we share with EUDET?

How can we help EUDET and How EUDET can help us ?

o Is DAQ software development on both sides (IPHC – EUDET) a good idea ?

o It will consume a lot of time at each upgrade (Documentation, misunderstanding, bug fixing ...)

o In any case IPHC will have to provide a new driver at each board FW upgrade ...

o Is there a better idea – to save time – than the SDK I proposed in March 2006 ?

o May be splitting Tasks (on SW and <u>Manpower</u> point of view) with a clear interface can help ?

IPHC Telescope DAQ upgrade status

EUDET MAPS DAQ Ma	actor Application			
LODET MAPS DAQ M	aster Application			
Boards Configuration	MIMOSTAR2_10MHZ	Events Counter	0	
Run Directory	c:\data\mis_2	Ouput Data EUDET (Bohn S	5W)	
Run Number	14666	O IPHC (DISK.	RMP)	
Events Number	100000			
Events number / file	10000	Start Run	Stop Run	
Status	DAQ application stopped - Wa	it a start request		
IOS USB DAQ V3.1				(
Lou Cont I	Boards parameters Roards testing Run Parameters Loop	Monitoring Remote Monitoring Warning and Error Mess	sages	1
	Board 0 B	oard 1 Board 2 Bo	and 3 Board 4 Board	5
Crate Conf 11. Jc. a1a2.42x42.2500khz 11. jc. a3a1a2a3.42x42.2500khz 11. jc. a3a1a2a3.42x42.2500khz 11. jc. a3a12a42.00nhz 11. jc. a3a3.42x42.2500khz 11. jc. a1a3.42x42.200nhz		oard 1 Board 2 Bo	ard 3 Board 4 Board 4 Board 7 7 7	5
11 bc.a1b2.42x42.25004he 11 bc.a1b12x3.42x42.10mhe 11 bc.yx3b12x32.42x42.25004he 11 bc.yx3b12x32.42x42.25004he 11 bc.yx3b3.42x42.25004he 11 bc.a1b3.42x42.25004he 11 bc.a1b3.42x42.25004he MGSTAFA2 MG	Board 0 B Board Status ABSENT	cerd 1 Board 2 Bo	[3 [5	5
11. bc, a1a2, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, ab312x34, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc WDSTAR2, 10004hc MDSTAR2, 10004hc MDSTAR2, 10004hc	Board O B Board Status PASENT Board Type VFAS VFAS Selected Board P ADC USB V2	eerd 1 Board 2 Boo 7 7 7 7 7 7 7 7	[3 [5	5
11. bc, a1a2, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, ab312x34, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc WDSTAR2, 10004hc MDSTAR2, 10004hc MDSTAR2, 10004hc	Board Status Board Status ASENT Board Status PASENT Board Type VFAS VFAS Selected Board I Status ADC USB V2 General Parameter	Board 2 Board 2 Board 2 Poor [? [? [? [? [? [? [? [? [? [?	7 2 7 2 7 2	5
11. bc, a1a2, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, ab312x34, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc WDSTAR2, 10004hc MDSTAR2, 10004hc MDSTAR2, 10004hc	Board Status Board Status ASENT Board Type VTAS VTAS Selected Board II IIII General Parameter Board Type IIIA	Board 2 Board 2 <t< td=""><td>7 7 7 7</td><td>5</td></t<>	7 7 7 7	5
11. bc, a1a2, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, ab312x34, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc WDSTAR2, 10004hc MDSTAR2, 10004hc MDSTAR2, 10004hc	Board Status Board Status AdSENT Board Type VFAS VFAS Selected Board Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status ADC USB V2 Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status ADC USB V2 Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status ADC USB V2 Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status Adc Type Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status	Board 2 Board 2 Board 2 [? [? [? [? [? [? [? [? [? Staguesce Boosekere [? [? Reset Edge [? [? Reset Ck edge [? [?	7 2 7 7 7 7 7 5 50 Done Pixel Court 7 Rurning Wat 0	5
11. bc, a1a2, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, aba12x32, 42x42, 25004hc 11. bc, ab312x34, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc 11. bc, ab32, 42x42, 25004hc WDSTAR2, 10004hc MDSTAR2, 10004hc MDSTAR2, 10004hc	Board Status Board Status Addemonstration Board Type VFAS VFAS Selected Board Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status ADC USB V2 Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status ADC USB V2 Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status Board Type Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status Board Type Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status Board Type Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status Board Type Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status Board Type Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status Board Type Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status Board Type Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status Board Type Image: Comparison of the selected Board Status Image: Comparison of the selected Board Status Board Type Image: Comparison of the selected Board Status Image: Comparison of	eed 1 Board 2 Boo 2 7 7 2 7 2 7 500 core Reservices Reset Edge 7 Reset Ck obge 10 Reset Longth 1	P Professional President	5
11. bc, a1a2, 42x42, 25004re 11. bc, a0a162a3, 42x42, 10mre 11. bc, a0a162a3, 42x42, 25004re 11. bc, a0a3, 42x42, 25004re 11. bc, a0a3, 42x42, 25004re 11. bc, a1a2, 42x42, 10mre 10. bc, a1a2, 42x42, 10mre MOSTAR2, 100x4re MOSTAR2, 100x4re	Board Status Board Status AdSENT Board Type VFAS VFAS Selected Board Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status ADC USB V2 Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status ADC USB V2 Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status ADC USB V2 Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status Adc Type Image: Constraint of the selected Board Status Image: Constraint of the selected Board Status	eed 1 Board 2 Bo 7	17 12 17 12 17 12 17 Done 17 Normal 17 Normal 18 10 19 Status 19 Status 10 10 10 10 11 10 12 10 13 Status 14 10	5
11. bc, a1a2, 42x42, 25004re 11. bc, a0a162a3, 42x42, 10mre 11. bc, a0a162a3, 42x42, 25004re 11. bc, a0a3, 42x42, 25004re 11. bc, a0a3, 42x42, 25004re 11. bc, a1a2, 42x42, 10mre 10. bc, a1a2, 42x42, 10mre MOSTAR2, 100x4re MOSTAR2, 100x4re	Board Status Passed Type PASEINT Board Type VFAS VFAS Selected Board Image: Comparison of the type VFAS ADC USB V2 Image: Comparison of the type Image: Comparison of type Board Type Image: Comparison of type Image: Comparison of type Board Type Image: Comparison of type Image: Comparison of type Board Type Image: Comparison of type Image: Comparison of type Board Addeev Image: Comparison of type Image: Comparison of type Digital Parameters: Image: Comparison of type Image: Comparison of type	eed 1 Board 2 Bo 2 7 7 2 7 7 7 7 7 7 7 7 7 7 7 7 7 7	P P P Status P Status P Status Sequencel Status Status Status Status Status P <td< td=""><td>5</td></td<>	5
11. c., cliat. 42:442, 2000/re 11. c., cliat. 42:442, 2000/re	Board Status Board Status Board Status AdSENT Board Type VFAS ADC USB V2 V General Parameter Board Addee Board State U Board State U Dight Parameter Sampler / Pixels Nb	Board 2 Board 2 <t< td=""><td>12 12 12</td><td>5</td></t<>	12 12 12	5
1. c., olia 2. 2042, 2000/e 1. e., olia 2. 2042, 2000/e 10510/2, 2000/e 10510/2, 2000/e 10510/2, 2000/e 10510/2, 2000/e 10510/2, 2000/e 10510/2, 2000/e 10510/2, 2000/e 10510/2, 2000/e 1052, 2000/e	Board Status Based Type VFAS Board Type VFAS VFAS Selected Board Image: Selected Board Image: Selected Board ADC USB V2 Image: Selected Board Image: Selected Board Board Type Image: Selected Board Image: Selected Board Digital Parameters Samples Offset Image: Selected Board Samples Offset Image: Selected Board Image: Selected Board	Board 2 Board 2 Board 2 [? [?	P P P Status P Status P Status Sequencel Status Status Status Status Status P <td< td=""><td>5</td></td<>	5
11. L., c. No. 2, C. 2000-102 11. L., c. No. 2, C. 2000-102 10. L. 2000, C. 2000, C. 2000-102 10. L. 2000, C. 2000,	Board Status Board Status Board Status AdSENT Board Type VFAS ADC USB V2 VFAS General Parameters Board Type Board Type VFAS Board Addee 0 Board Addee 0 Digital Parameters Samples / Phetis Nb 9448 Samples / Phetis Nb 9447 Top Add 9447	Board 2 Board 2 Board 2 [? [?	12 12 12	5
1 L. p. Ala. 42-A42, 2008/s 1 . e. p. Ala. 42-A42, 2008/s 1	Board O B Board Status AdSENT Board Type VFAS Selected Board V ADC USE V2 V General Parameter Board Addee Board Addee 0 Board Addee 0 Dight Parameter Sampler / Phase Nb Sampler / Dubt Nb 9440 Sampler Othert No 0 Top Add 9447 Cock Divider P	aed 1 Boad 2 Bo 2 2 2 2 7 2 7 2 7 2 7 2 7 2 7 2	12 12 12	5
1. L. p. Ind. 4.5442 (2006): 1. e. p. Jin 4.543 (2.442) (1997): 1. e. p. Jin 4.544 (2.443) (1997): 1. e. p. Jin 4.544 (2.444) (1997): 1. e. p. e. p. p.	Board 0 B Board Status AddExit Board Type VFAS Selected Board Image: Comparison of the selected Board ADC USB V2 General Plannoles: Board Addree Image: Comparison of the selected Board Board Addree Image: Comparison of the selected Board Digital Plannoles: Image: Comparison of the selected Board Cook Divide Image: Comparison of the selected Board Cook Divide Image: Comparison of the selected Board Cook Divide Image: Comparison of the selected Board	aard 1 Board 2 Bo 2 2 2 2 7 2 7 2 7 2 7 2 7 2 7 2	12 12 12	5
11. c., c. lo. 2, 42.442, 2000/se 11. c., c. lo. 34.25, 24.24, 2006/se 11. c., c. lo. 34.25, 24.24, 2006/se 11. c., c. lo. 34.25, 24.24, 2006/se 11. c., c. lo. 34.25, 24.25, 2006/se 11. c., c. lo. 34.25, 24.25, 2006/se 11. c., c. lo. 34.25, 24.25, 2006/se 10. c. lo. 34.25, 24.25, 2006/se 10. c. lo. 34.2, 2006/se 10. c	Board O B Board Status Addesen Board Type VFAS Selected Board V ACC USB V2 V General Parameters Board Type Board Type Dogsal Parameters Board State IM Dogsal Parameters V Samples / Phelis Nb 9440 Samples / Phelis Nb 9447 Cock Delay 5 Spee 1 0	aed 1 Boad 2 Bo 2 2 2 2 7 2 7 2 7 2 7 2 7 2 7 2	12 12 12	5
11. c., c. lo. 2. 43-42, 2000 he 11. c., c. lo. 3. 43-54, 2. (behr 11. c., c. lo. 3. 44, 2. (behr 11. c., c. lo. 3. 44, 2. (behr 12. c. lo. 3. 44, 2. (behr 13. c. lo. 3. 44, 2. (behr 14. c. lo. 3. 44, 2. (behr 15. c. c. def, 2. beed, 1. (behr) 15. c. def, 2.	Board 0 B Board Status AddExit Board Type VFAS Selected Board Image: Comparison of the selected Board ADC USB V2 General Plannoles: Board Addree Image: Comparison of the selected Board Board Addree Image: Comparison of the selected Board Digital Plannoles: Image: Comparison of the selected Board Cook Divide Image: Comparison of the selected Board Cook Divide Image: Comparison of the selected Board Cook Divide Image: Comparison of the selected Board	aad 1 Boad 2 Bo 2 2 2 2 7 2 7 2 7 2 7 2 7 2 7 2	12 12 12	5
11. c., c. lo. 4. 6.442, 2000 he 11. c., c. lo. 4. 6.444, 10.444, 10.144, 10.144, 10.1444	Board 0 B Board Status Addesign Board Type VFAS Selected Board Image: Comparison of the selected Board ADC USB V2 General Parameters Board Type Image: Comparison of the selected Board Digital Parameters Image: Comparison of the selected Board Digital Parameters Image: Comparison of the selected Board Samples Officet Image: Comparison of the selected Board Digital Parameters Image: Comparison of the selected Board Samples Officet Image: Comparison of the selected Board Image: Comparison of the selected Board Image: Comparison of the selected Board Image: Selected Board Image: Comparison of the selected Board Image: Selected Board Image: Comparison of the selected Board Image: Selected Board Image: Comparison of the selected Board Image: Selected Board Image: Comparison of the selected Board Image: Selected Board Image: Comparison of the selected Board Image: Selected Board Image: Comparison of the selected Board Image: Selected Board Image: Comparison of the selected Board<	aad 1 Boad 2 Bo 2 2 2 2 7 2 7 2 7 2 7 2 7 2 7 2	12 12 12	5
11. b., c. hol. 4.544, 2500 he 11. b., c. hol. 4.544, 2500 he 12. b. c. hol. 4.545, 2500 he 12. b. c. hol. 4.545, 2500 he 12. b. c. hol. 4.545, 2500 he 13. b. c. hol. 4.554, 2500 he 14. b. c. hol. 4.554, 2500 he 15. b. c. hol.	Board 0 B Board Status AdSENT Board Type VFAS Selected Board V ADC USE V2 VFAS General Plannoles: Board Addree Board Addree V Board Addree V Digital Plannoles: Board Addree Digital Plannoles: V Board Addree V Digital Plannoles: V Digital Plannoles: V Digital Plannoles: V Digital Plannoles: V Clock Diredio 0 Top Adds 9447 Clock Diredio 2 Spipe 1 0 V Spipe 1 V Spipe 1 V Spipe Clock V Spipe Clock	aed 1 Boad 2 Bo 2 2 2 2 7 2 7 2 7 2 7 2 7 2 7 2	12 12 12	5
11. b., c. hol. 4.544, 2500 he 11. b., c. hol. 4.544, 2500 he 12. b. c. hol. 4.545, 2500 he 12. b. c. hol. 4.545, 2500 he 12. b. c. hol. 4.545, 2500 he 13. b. c. hol. 4.554, 2500 he 14. b. c. hol. 4.554, 2500 he 15. b. c. hol.	Board 0 B Board Status AdSENT Board Type VFAS Selected Board Image: Control of the selected Board ADC USB V2 Image: Control of the selected Board General Parameters Board Addee Board Addee Image: Control of the selected Board Dightal Parameters Sampler: / Private Nb Sampler: / Private Nb Image: Control of the selected Board Top Adds Image: Private Nb Cock, Delay 0 Image: Private Nb Sampler: / Private Nb Image: Private Nb Cock, Delay 0 Image: Private Nb Sampler: / Private Nb Image: Private Nb Cock, Delay 0 Image: Private Nb Image: Private Nb Image:	aed 1 Boad 2 Bo 2 2 2 2 7 2 7 2 7 2 7 2 7 2 7 2	12 12 12	5
11 L. c., al. 4. 64-42, 2000 her. 11 m. c., al. 4. 64-42, 2000 her. 11 m. c., al. 4. 64-42, 2000 her. 11 m. c., al. 6. 64-42, 2000 her. 12 m. c., al. 6. 64-62, 2000 her. 13 m. c., al. 6. 64-62, 2000 her. 14 m. c. al. 6. 64-62, 2000 her. 14 m. c	Board 0 B Board Status AdSENT Board Type VFAS Selected Board V ADC USB V2 V General Parameters Board Addree Board Addree 0 Board Addree 0 Board State 0 Board Addree 0 Datal Parameters V Sampler / Frietin Nb 0440 Sampler Officie 0 Top Adds 9447 Clock Dirder 2 > 10,000 Mits Spice 1 0 Spice State Sampler Context Spice State Sampler Context Clock Dirder 2 > 20,000 Mits Spice State 0 Spice State Sampler Context Clock Dirder 2 > 20,000 Mits Spice 1 0 Clock Dirder 2 > 20,000 Mits Clock Dirder 2 > 20,000 Mits Clock Dirder 2 > 20,000 Mits External State State 2 =	aed 1 Boad 2 Bo 2 2 2 2 7 2 7 2 7 2 7 2 7 2 7 2	12 12 12	5
11 L. c., al. 4. 64-42, 2000 her. 11 m. c., al. 4. 64-42, 2000 her. 11 m. c., al. 4. 64-42, 2000 her. 11 m. c., al. 6. 64-42, 2000 her. 12 m. c., al. 6. 64-62, 2000 her. 13 m. c., al. 6. 64-62, 2000 her. 14 m. c. al. 6. 64-62, 2000 her. 14 m. c	Board 0 B Board Status AdSENT Board Type VFAS Selected Board Image: Control of the selected Board ADC USB V2 General Parameters Board Addee Board Addee Board Addee Dight Parameters Sample: / Puels Nb Sample: / Puels Nb Dight Parameters Sample: Officet Dight Parameters Dight Parameters <	eed 1 Boad 2 Bo 2 2 2 7 2 7 2 7 2 7 3 00 0000 Permitter Pest Edge 7 Pest Edg	12 12 12	5
11 L. c., al. 4. 64-42, 2000 her. 11 m. c., al. 4. 64-42, 2000 her. 11 m. c., al. 4. 64-42, 2000 her. 11 m. c., al. 6. 64-42, 2000 her. 12 m. c., al. 6. 64-62, 2000 her. 13 m. c., al. 6. 64-62, 2000 her. 14 m. c. al. 6. 64-62, 2000 her. 14 m. c	Board 0 B Board Status AdSENT Board Type VFAS Selected Board Image: Comparison of the selected Board ADC USB V2 General Parameter Board Type Image: Comparison of the selected Board Digital Parameter Image: Comparison of the selected Board Samples (Thesh Nb Image: Comparison of the selected Board Digital Parameter Image: Comparison of the selected Board Samples (Thesh Nb Image: Comparison of the selected Board Samples (Thesh Nb Image: Comparison of the selected Board Stop Enable External Stop Enable External Stop Enable External Stop Comparison of the selected Board Stop Enable External Stop Enable External Stop Enable Analog Parameters	eerd 1 Board 2 Bo 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	12 12 12	5

One Idea ?

- Provide a remote control of IPHC DAQ
 - Limited set of parameters under remote control
 - ► Master application : Start, Stop, Status

► The advantages

- Reduced commands set (Easy to use)
 - Specify configuration
 - ► Start, Stop Run, get Status
- **Don't need to handle boards parameters files**
- ► Modify and store parameters from IPHC GUI
- ► No need to upgrade GUI to follow board FW
- **Bugs** will be quickly fixed because we use this SW
- ► We can apply the same idea for JTAG SW

" This is a kind of executable with command line interface to provide configuration parameters "

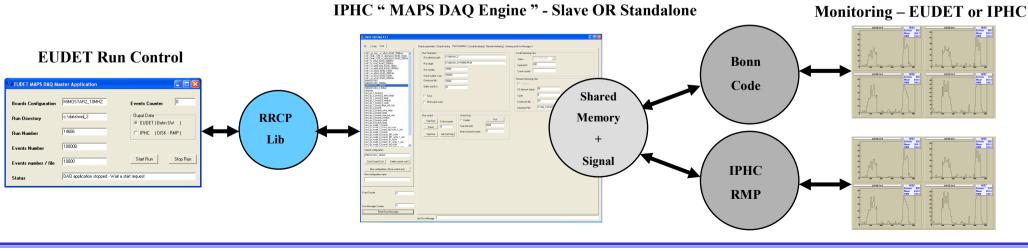
IPHC Telescope DAQ upgrade status

How to do it ?

- **RRCP** (Remote Run Control Protocol) and RMP (Remote Monitoring Protocol) libraries
- **RRCP and RMP libraries can allow**
 - ► A common interface for "MAPS DAQ engine " to EUDET Demonstrator and IPHC Telescope
 - Upper layer provides generic functions
 - **b** Lower layer implementation can be done in a different way for EUDET / IPHC
 - ▶ Upgrades to improve lower layer performances can be done without consequences on top application

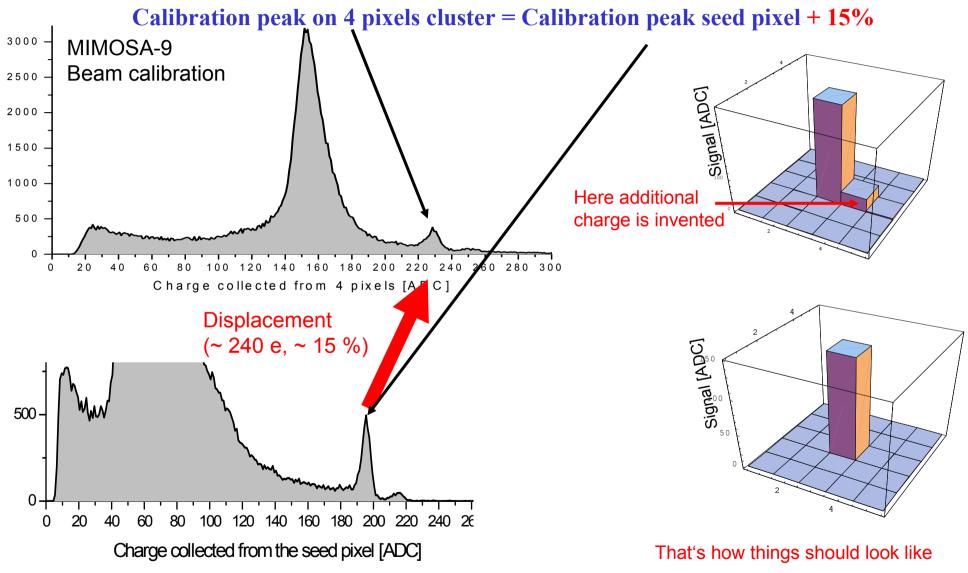
Advantages

- ▶ We can quickly Use and <u>Test</u> the "MAPS DAQ Engine " in our Telescope
- **Global SW** (Run Control, Monitoring) is not linked we are free on both side : EUDET / IPHC



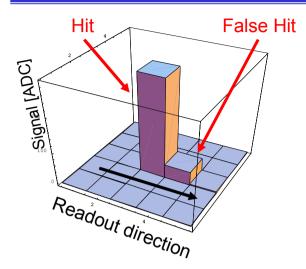
Analogue signal integrity for MimoTel readout – The problem

We have discovered a very strange result (Mimosa 5, 9, 11 ...)



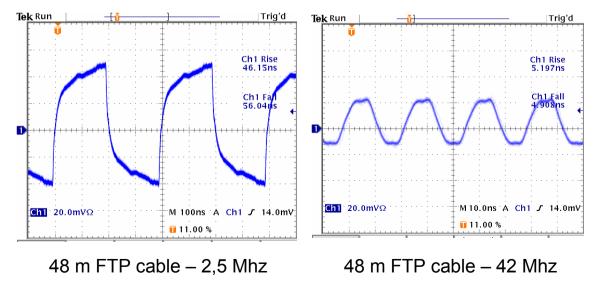
Slide borrowed from Michael Deveaux presentation

Analogue signal integrity for MimoTel readout – Preliminary Ideas



- It is worst with long cable ($40 \text{ m} \sim 15 \%$, $2 \text{ m} \sim 2\%$)
- ▶ It is not reflexion from preceding pixel (impedance mismatch)
- ▶ It is connected to cable bandwidth
- After a hit, the signal has not the time to fall down to base level
- ▶ If we consider 1° order system, to get 99 % of signal or 1 % error
 - **•** Rise / Fall time must be less than T Readout / 5
 - **•** For 10 MHz clock it gives 100 nS / 5 = 20 nS
- **•** This problem has never been studied with FTP cables foreseen for EUDET demonstrator

▶ But it has also been observed with Mi*2 and FTP cables



Test with 48 m FTP 100 MHz cable

- ► At 2,5 Mhz => Tr ~ Tf ~ 50 nS
- ► At 42 Mhz => Tr ~Tf ~ 5 nS
- ► We must be in a flat area of cable BW
- ► Coaxial cable is much better
- ► We may need to limit cable length

Detailled investigation must be done

Conclusion

Firmware

- **CDS** on board, Trigger handling, Synchronous readout The of N boards are ready
- ▶ Distribution of new boards FW and SW : we hope it will be possible for end of January 2007 ?

Software

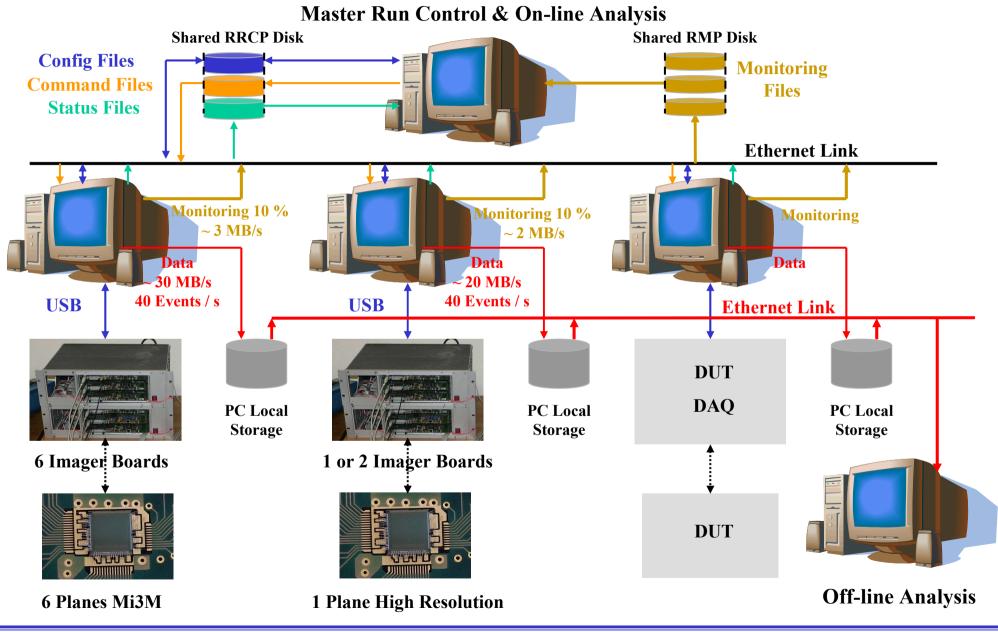
- **•** Test with 6 boards, CDS readout, trigger handling => Done : 30 Hz
- ▶ Integration in our beam Telescope, beam test possible in spring 2007
- Proposition of Master / Slave architecture for DAQ and JTAG SW

Integration

- ► A problem has been discovered on Mimosa readout chain
- ▶ It requires more detailed study (For example : test with Mi*2 at 10 MHz, 2 m, 10 m, 40 m)
- ► The consequence can be a cable length limitation between Telescope and DAQ

- **Demonstrator DAQ architecture proposition**
- ► RRCP
- ► RMP
- ▶ RRCP & RMP old slides (Design Review 06/04/2006)
- **•** Trigger position & Hit polarity

One proposition for Demonstrator DAQ



RRCP – Remote Run Control Protocol

The goal

- ▶ Provide a common set of functions for DAQ and JTAG remote control
- **Commands** functions
 - **Load a configuration file (Boards conf for DAQ Mimosa operating mode & bias for JTAG)**
 - **Set** run parameters : run number, events number, destination directory ...
 - **Execution :** Start Stop Run (DAQ) / Load Mimosa parameters in chip (JTAG)
- **Status** functions
 - ▶ Return status of command function call (passed / failed)
 - ► Return current event number (DAQ)

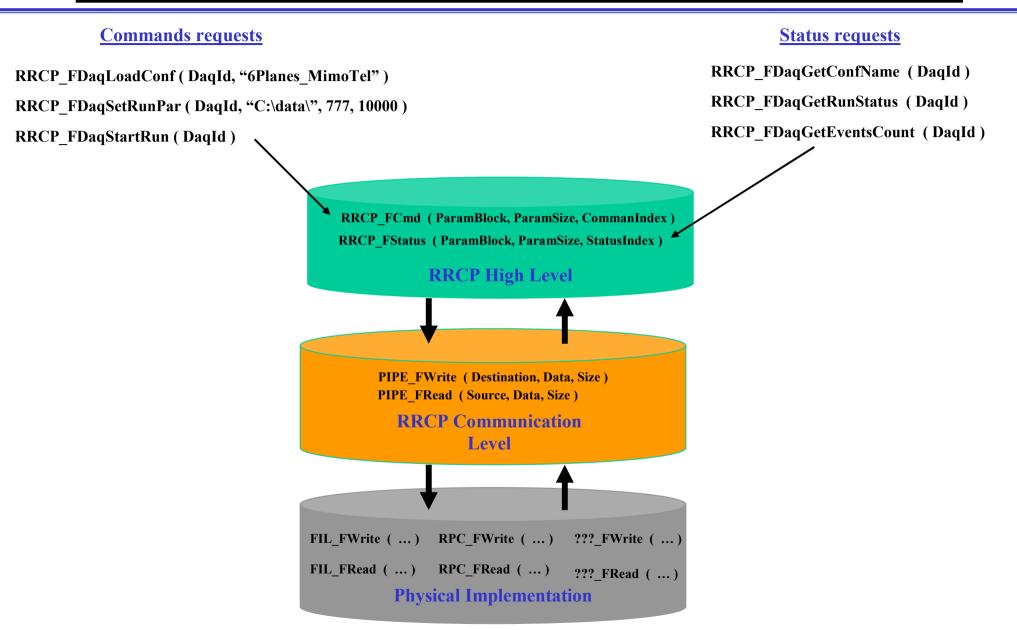
Implementation

- **•** Based on generic commands & status functions : parameter bloc, command number, return block
- Library based on three levels stack
 - ► Top

▶ Bottom

- **RRCP** abstraction layer high level functions : Start / Stop Run
- **Middle Middle Communication** layer " pipes " library
 - Physical implementation : command / status files with polling Network protocol (RPC–TCP/IP) ...

RRCP – Remote Run Control Protocol



RMP – Remote Monitoring Protocol

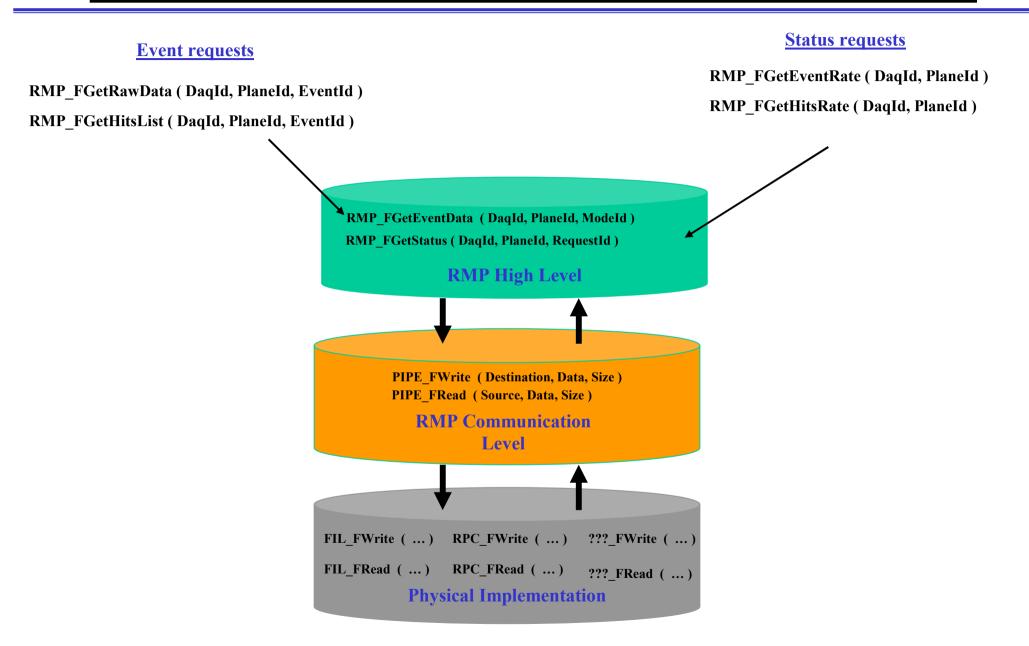
Windows USB DAQ / Linux Monitoring

- **•** Both are ready How to build a bridge between DAQ and Monitoring ?
- ► We have two different operating systems ...
- ► Can we avoid system programming ?
- ► Can we do something generic with minimum development efforts ?
- ► Can we build this bridge step by step ?
 - ► To have quickly a solution, of course not with best performances
 - **Upgrade later to improve transfer rate, flexibility**

One idea ... RMP based on files

- ▶ It was the backup solution of our VME DAQ (Main solution = shared buffers)
- ► We can adopt the same structure as for RRCP
 - ▶ Тор
- **RMP** abstraction layer high level functions : GetEvent ()
- Middle Communication layer " pipes " library
- ▶ Bottom
 ▶ Physical implementation : small data files with polling Network protocol (RPC–TCP/IP) ...

RMP – Remote Monitoring Protocol



How to synchronize MAPS, DUT, ... DAQ ? Remote Run Control Protocol (RRCP)

- **Each DAQ is controlled either**
 - ▶ In local, GUI acts as a master => Stand alone application in lab or User Telescope
 - **•** By a commands interpreter, GUI acts as a slave => EUDET Beam Telescope
- **Each DAQ handles his configuration files (stored in a working directory)**
- ► How it works ?
 - **EUDET Master Run Control application (MRC)**
 - **•** Copy configurations in each DAQ working directory
 - **Send command Start, Stop ... with parameters by RRCP (write command file)**
 - Slave DAQ applications
 - ▶ Interpreter receive commands by RRCP (read command file in polling)
 - **Execute** command
 - Return status file to MRC (write status file)

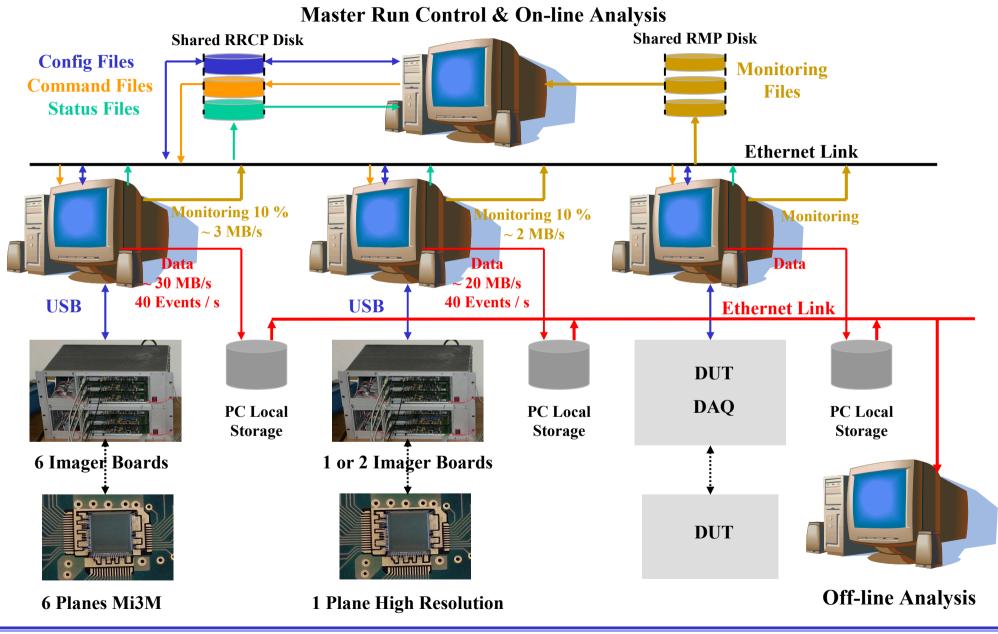
Remote Run Control Protocol ... RRCP ?

- ► This RRCP is not a genial idea ;-)
 - It's the standard way to control DAQ systems
 - **•** But implementation can be done in a basic way

► The implementation

- ▶ Using command and status files on a shared network drive
- **Command files from Master Run Control to slave DAQ**
- **Status files from slave DAQ to Master Run Control**
- Checking command / status files by slow polling remove file after processing
- ► A library provides RRCP function calls and files format
 - ► Only need to add Remote Control & Status report features on each DAQ software
 - **Each team can maintain his own DAQ software**

One proposition for Demonstrator DAQ



Conclusion

Remote Run Control & Remote Monitoring Protocols = Top layer + 2 implementations

- ▶ First basic version with files : easy to program & debug
- Second with standard network Protocols : RPC, Socket pipe ...
- ► No need to develop a global DAQ system <u>Application</u>
 - ► Master Run Control application
 - **Each DAQ is independent BUT can be controlled as a slave system**
 - ► Allow to use the same DAQ in User or EUDET context
 - ► It will be easier for DAQ upgrade => few modifications of MRC
- **•** On-line Monitoring and Off-line analysis
 - ▶ Provide libraries for event building (EVB) from all Data Sources (MAPS, DUT ...)
 - ► The same EVB libraries should be used for On-line & Off-line analysis

Two ideas to build Telescope global DAQ

► Idea N° 1 : DAQ HW API & Global DAQ Application

- **Each group provides HW API libraries (eg : USB Board SDK, JTAG SDK)**
- ▶ Need a global DAQ Application (" Active Application " : Real Time, SDR, EVB ...)

► Idea N° 2 : Slave DAQ & Master Run Control Application

- **Each group implements Slave Remote Control in his DAQ Application**
- ▶ Need a Master Run Control Application (" Passive Application ": Control, Supervision)

▶ Idea N°2 ... How to do : EVent Building (EVB) & Software Data Reduction (SDR)???

Pseudo on-line EVB from data files

► SDR ?

- ▶ in each DAQ Application => 2 Outputs : RAW (keep as reference) + after DR
- ► after final event building

Hit " After " trigger

Hit " Before " trigger

