

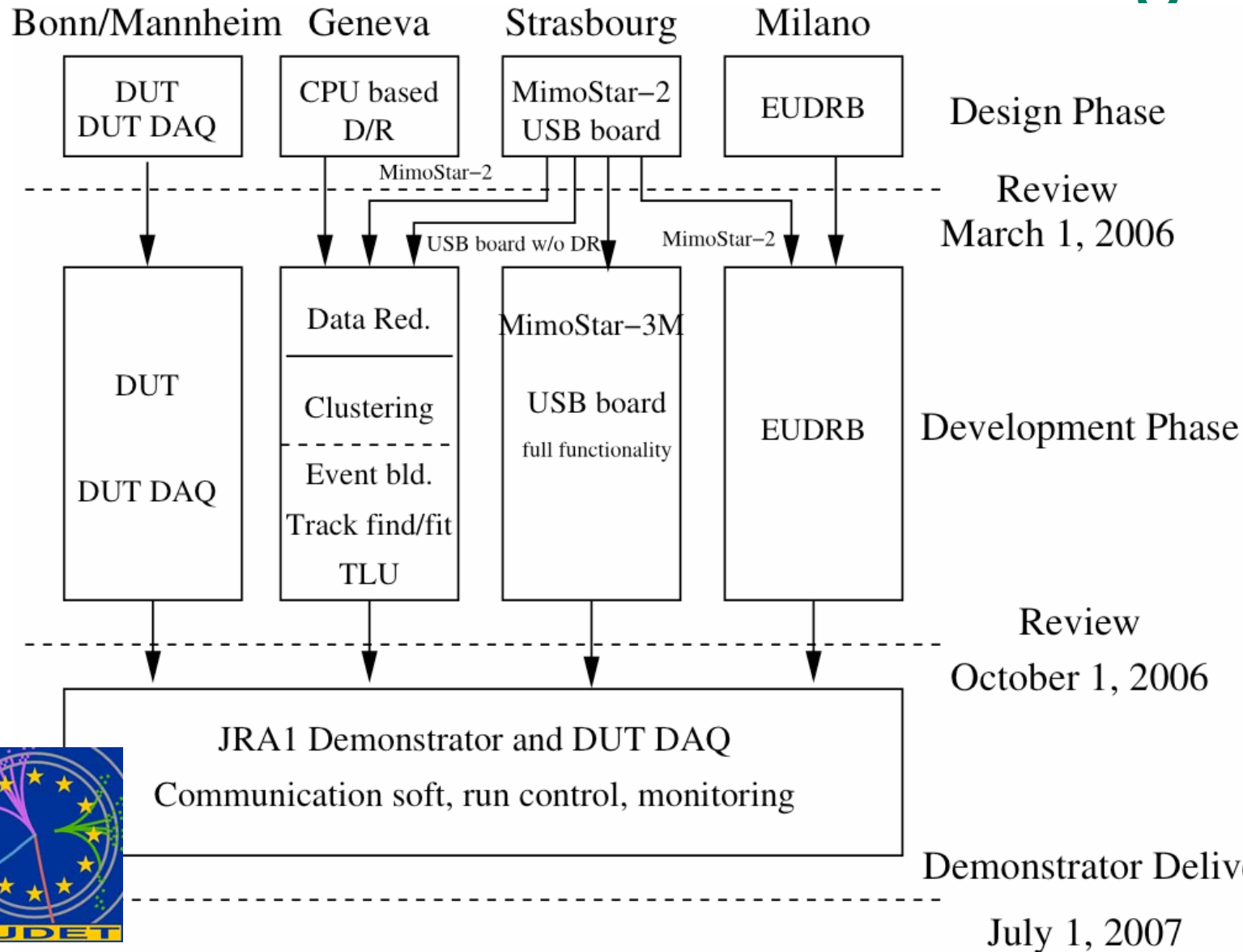
JRA1 DAQ Status

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- Status DAQ board INFN
- Strasbourg DAQ boards
- TLU Bristol
- Software Status
- Upcoming Tests
- Financial Status (no slides)



JRA 1 - DAQ Planning



A VME-64x based DAQ card for MAPS sensors

Overview of the operation of the EUDRB card

Basic features:

a) MODULARITY:

- **One** mother board (**EUDRB_MOBO**), built around an ALTERA CycloneII EP2C70F896C8N FPGA and hosting the core resources (SRAMs, FIFOs, VME64x interface, trigger port, diagnostic UART)
- **One** analog daughter card (**EUDRB_DCA**), based on the successful LEPSI and SUCIMA designs
- **One** digital daughter card (**EUDRB_DCD**), featuring a standard "PCI Mezzanine Card" interface to the mother board. It drives/receives control signals for the detectors and it features a USB 2.0 link

b) VME64X slave interface

c) USB2.0 interface

d) Interface to the EUDET trigger bus (trigger request, event number, busy)

e) Two readout modes:

- Zero Suppressed readout to minimize the readout dead-time while in normal data taking.
- Non Zero Suppressed readout of multiple frames for debugging or off-line pedestal and noise calculations

e) NIOS II, 32 bit "soft" microcontroller implemented in the CycloneII FPGA. It handles tasks like:

- on board diagnostics
- on-line calculation of pixel pedestal and noise (not interfering with data taking operations)
- remote configuration of the FPGA via RS-232, VME, USB2.0

A VME-64x based DAQ card for MAPS sensors

Overview of the operation of the EU DRB card

Clock rate of the FPGA : 80MHz (40MHz for the NIOS II processor)

- Clock rate of the A/D converter : up to 20MHz.

=> frame acquisition time: for a MIMOSA-V 1Mpixel sensor with 4 independent outputs sampled @20MHz: $262.144 * 50 \text{ ns} \sim 13 \text{ ms}$

-readout modes and trigger processing times

- "Full Frame" readout mode:

The card responds to a trigger by sending out ALL RAW pixel data for at least 3 frames(*): the frame being acquired at trigger time, the preceding one and the following one, for a total of 6MB per event.

In this readout mode the MAPS-DAQ it is allowed to stop the recording of new data from the MAPSs until the three frames selected by the trigger have been sent to the data acquisition CPU.

The latency in the EU DRB response to a trigger can thus be no less than ONE and up to TWO frame time

The processing time of a trigger includes:

- the data transfer time (assuming a sustained bandwidth of 80MB/s for block transfers in 2e-VME mode **each 3-frames event (6MB) can be acquired in about 1/13s per sensor**)
- the time to reset the MIMOSA V detectors at the end of the readout phase.

The **"TRIGGER_BUSY"** is set as soon as the trigger is received and released when data has been transferred to the host PC

(*) a design specification by Eleuterio Spiriti, INFN-ROMA III

A VME-64x based DAQ card for MAPS sensors

Overview of the operation of the EUDRB card

... from previous slide

- "Zero Suppressed" readout mode:

The card responds to a trigger by sending out a formatted block which includes an header and a trailer identifying the event number and the number of hits (**the final implementation will feature the wordcount in the header**).

Processing of a trigger in this mode does not stop the scan of the detector -> no loss of data due to trigger processing

The **latency** is virtually none, since the extraction of sparsified data from the pixel memories starts as soon as a trigger is received.

The **processing time** of a trigger includes:

- the extraction time (1 frame time): data is read from the pixel memories while they continue to be updated with new samples of pixel voltages. Address and data of "hit" pixels are stored into an output FIFO memory.

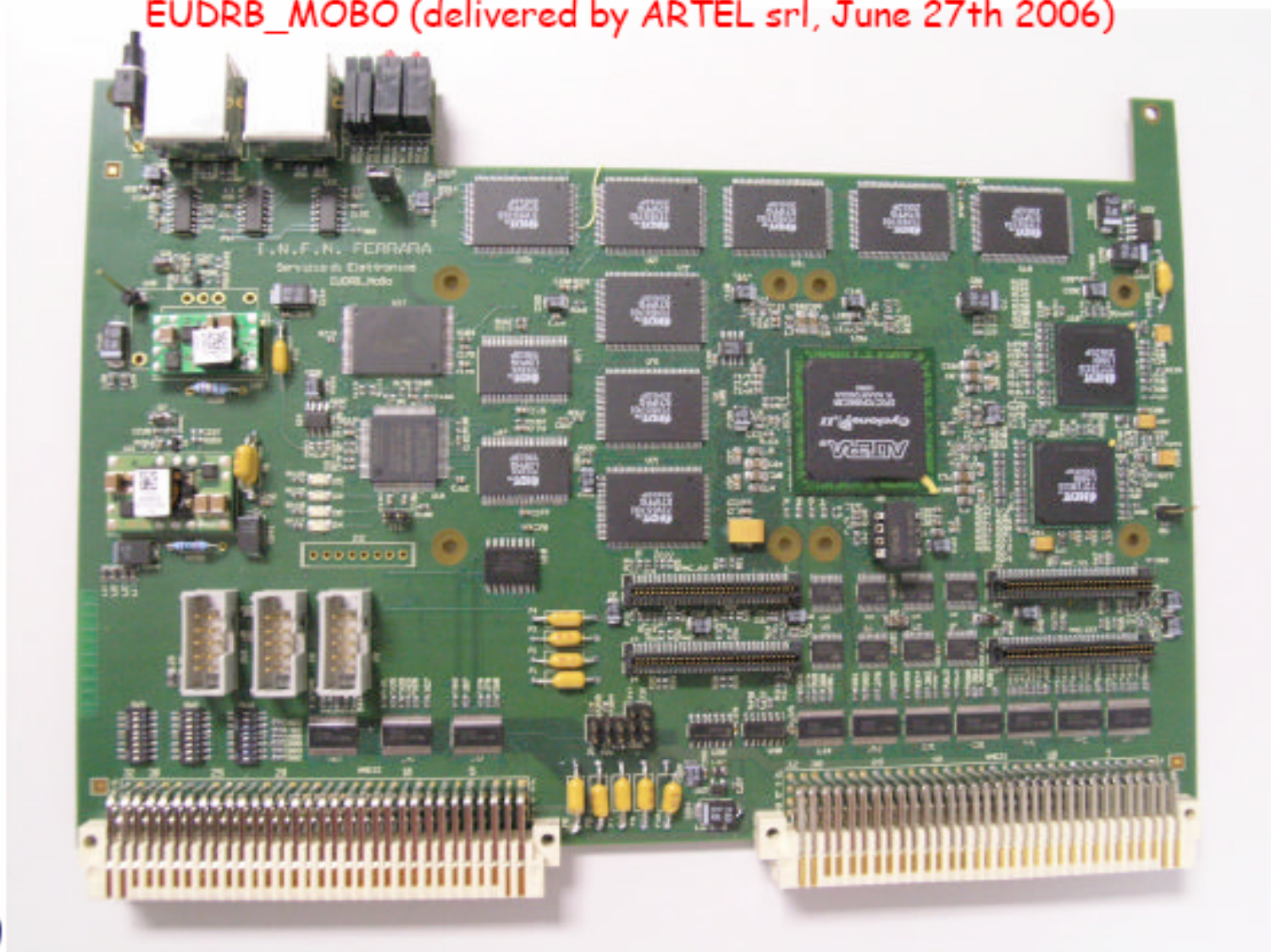
- the data transfer time: the output FIFO memory is read and its contents transferred to the host PC

The **"TRIGGER_BUSY"** is set as soon as the trigger is received and released when data has been transferred to the host PC.

In this mode it would also be possible to release the "TRIGGER_BUSY" right after filling the output FIFO, overlapping the readout phase of a trigger with the processing of the next

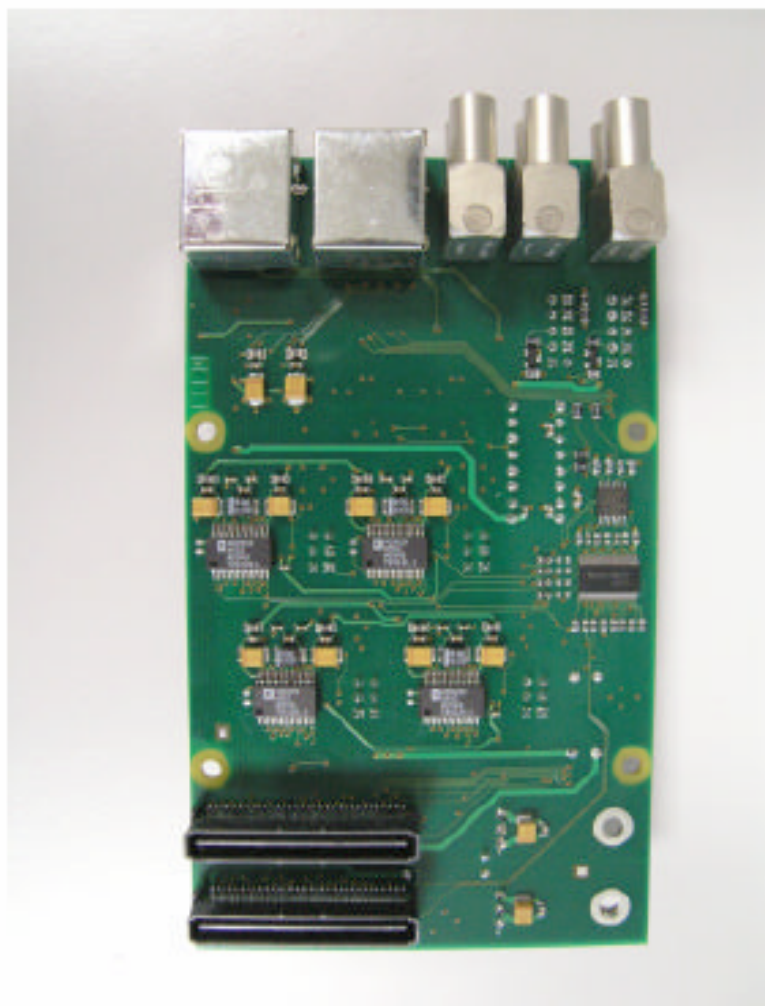
A VME-64x based DAQ card for MAPS sensors
Status report

EUDRB_MOBO (delivered by ARTEL srl, June 27th 2006)

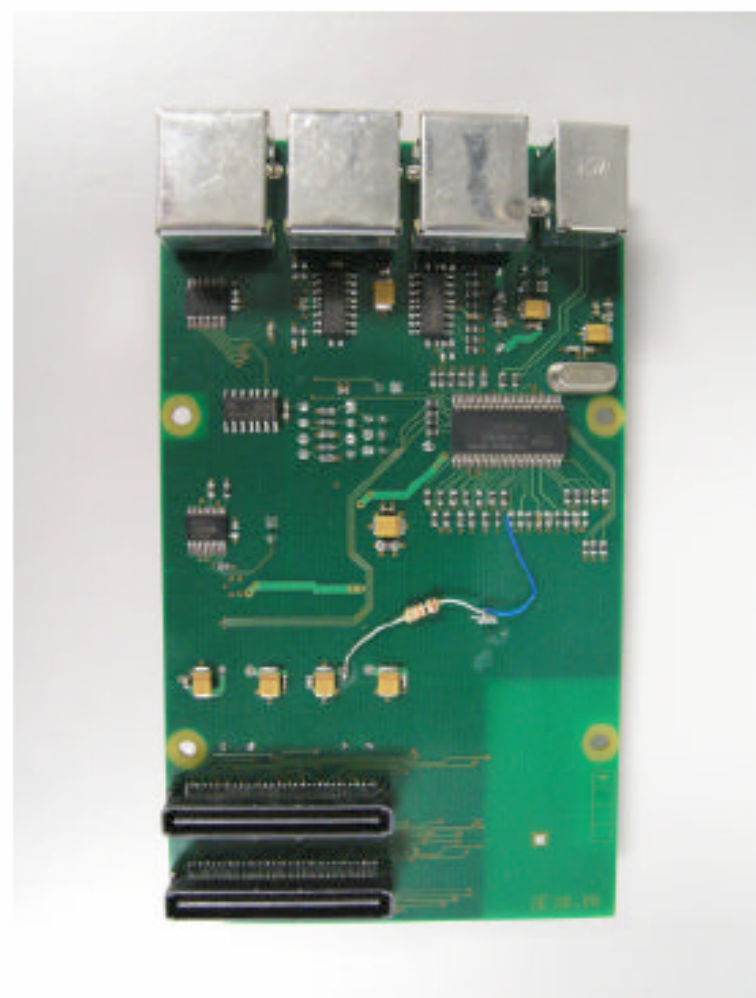


A VME-64x based DAQ card for MAPS sensors
Status report

EUDRB_DCA & EUDRB_DCD (delivered by ARTEL srl, June 27th 2006)



EUDRB_DCA: Analog daughter card
(bottom view)



EUDRB_DCD: Digital daughter card
(bottom view)

USB ADC Board & DAQ Status

To Do List for next weeks, on last EUDET meeting ...04/04/2006 ...

- ▶ On board CDS is implemented => **Must be Tested**
- ▶ Trigger handling is implemented => **Must be Tested**
- ▶ 6 Imager Boards synchronization - Master / Slave => **Must be implemented & tested**

It will require ~ 4 weeks. Due to others projects, this work has been shifted from April to September, we hope to finish for October meeting !

- ▶ A production of 12 USB ADC boards has been launched
 - ▶ Components ordering and mounting by a private company
 - ▶ We should receive first boards in October, **Wait for result ...Testing boards at lab ...**
 - ▶ We hope to deliver first boards in February - March 2007 (7 boards)
- ▶ JTAG GUI software extension for N Mimo* control is done

Trigger Logic Unit

- Simple Handshake via Trigger/Busy/Reset on RJ45 LVDS lines (or TTL-Lemo)
- Timestamp and event-number via USB

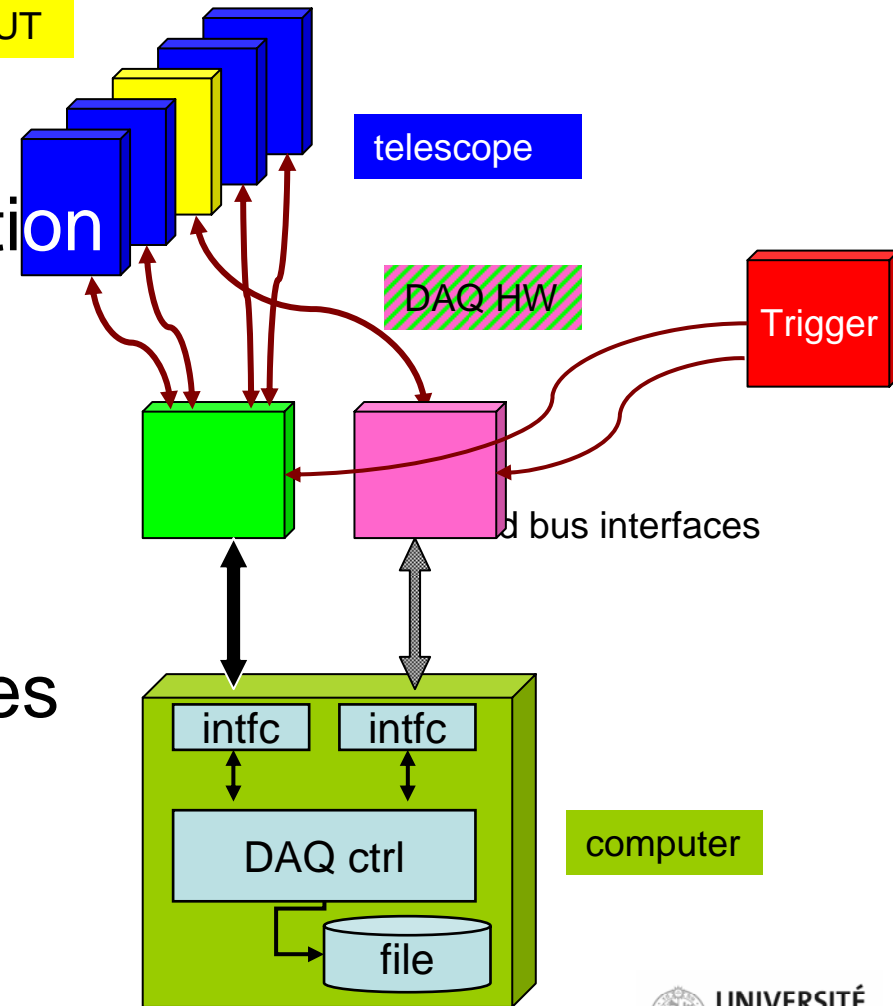
QuickTime™ and a
TIFF (LZW) decompressor
are needed to see this picture.

TLU - more info

- 1 box in Geneva, 1 in Bristol
 - tested in July by Emlyn, David and myself
- 3 more boxes under production
 - will be distributed to interested parties
 - may eventually need to be shared
- We have to deal out the money issue
- First 'guinea pig' will be Bonn in October

JRA1 - DAQ

- Synchronization via **DUT** common TLU
- Digitization/Sparsification with dedicated HW or commodity equipment (USB interface)
- SW level integration with standard interfaces



JRA1 - DAQ Software

- **Reuse - don't reinvent**
- **Combine:**
 - Existing DAQ from Bonn for DUT
 - Existing readout for Strasbourg hardware
 - Bristol library for TLU
- **Added functionality:**
 - creation of ROOT-files from binaries
- **Upcoming functionalities:**
 - Data reduction (CDS and Clustering)
 - Tracking (via Kalman-filter)
 - multi-PC acquisition, platform independence (?)



Buffer Monitor - 3 buffers found

Buffer Name	Type	Size	Fill	Total Written
DEPFET_1	DAQ	0x00010000	0.0%	0x00004720
OMO_DEPFET	OMO	0x00030000	9.5%	0x00004952
OMO_TEST	OMO	0x00030000	9.5%	0x00004952

DEPFET Dummy producer

Shared Buffer
Name: DEPFET_1 Size [ints]: 0x010000
Mod.ID: 0x1 Disconnect

Write full events (no zero supr.)

Amplitude
Sigma: 1000 Mean: 5000

Hits per Event
Sigma: 2 Mean: 5

Hit location
X: Sigma 6 Mean 32
Y: Sigma 6 Mean 64

Start Pause Stop

Stop at 1000

Events / sec. 100 350

FileWriter

Event Number: 340

Main Control

 DEPFET_1

OMO Info
OMO_DEPFET OMO_TEST
Send DAQ Buffers: DEPFET_1
OMO Fraction: 100

Found Data: DEPFET_1:337
Found Data: DEPFET_1:338
Found Data: DEPFET_1:339
Found Data: DEPFET_1:340
Found Data: DEPFET_1:341
Found Data: DEPFET_1:342
Found Data: DEPFET_1:343
Found Data: DEPFET_1:344

Write to File
Run number: 2073
Start Stop

File = X:\DAQ_EUDET\Runs

QuickTime™ and a TIFF (LZW) decompressor are needed to see this picture.

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EUDET - IPHC USB Imager Board SDK Demonstration Program v1.0

Board Control | Errors & Messages | Monitoring

Open Driver
Add Board
Read Firmware Version
Check Board
Init Board Registers

ADC USB V2 Use Software Settings

Board Status
 Stop Done Pixel Count: 4096
 Running Wait

Sequencer Status
 Stop Post Reset
 Wait Run
 Reset Sync Done

Analog Parameters
Chan Width: *RAW_CDS_0
Read Mode: FROM BEGIN

Dac control
Dac 1: 0 Dac 3: 0
Dac 2: 0 Dac 4: 0

Digital Parameters
Samples / Pixels Nb: 4096
Samples Offset: 0
Top Addr: 4095
Clock Divider: 0 => 50,000 Hz
Clock Delay: 0
Spare 1: 0
 Stop on pixel count Sequencer Enable
 External Clock Enable
 External Start Enable External Stop Enable
 External Start Edge External Stop Edge
External Start Source: LVDS External Stop Source: LVDS

Sequencer Parameters
Reset Edge: 0
Reset clk edge: 1
Reset Length: 0
Post Reset: 0
Max Cycle: 0
Trigger Veto: 0
Stop Delay: 0
Out Clk Invert: 0
Proc Enable: 0
 Stop Out Clk at End Of Acquisition

Shared Buffer
Name: STRAS_1 Size [ints]: 0x010000
Mod.ID: 0x1 Disconnect

Start Pause Stop

Stop at 1000

Events Sent: 1382

Status: Acquisition is running

Close Driver

Upcoming issues

- Beam test for Bonn people
 - we want to help them use the TLU
 - sort out software issues (Emlyn)
- Software development will go on (basically only started in July)
 - e.g. external triggering of Strasbourg board
 - Data reduction and event building
 - DAQ Version 2 (rewritten, cleaned up code) (if possible, for Demonstrator already)

Conclusions

- EUDET program is fully incorporated in the ILC detector R&D, giving additional funding on international scale
- **BUT: EUDET is a contract between us and the EU with well defined milestones and deliverables**
- Geneva is providing DAQ for JRA1 pixel telescope and is well on track



STAY TUNED FOR MORE

