EUDET
JRA3 ECAL and FEE

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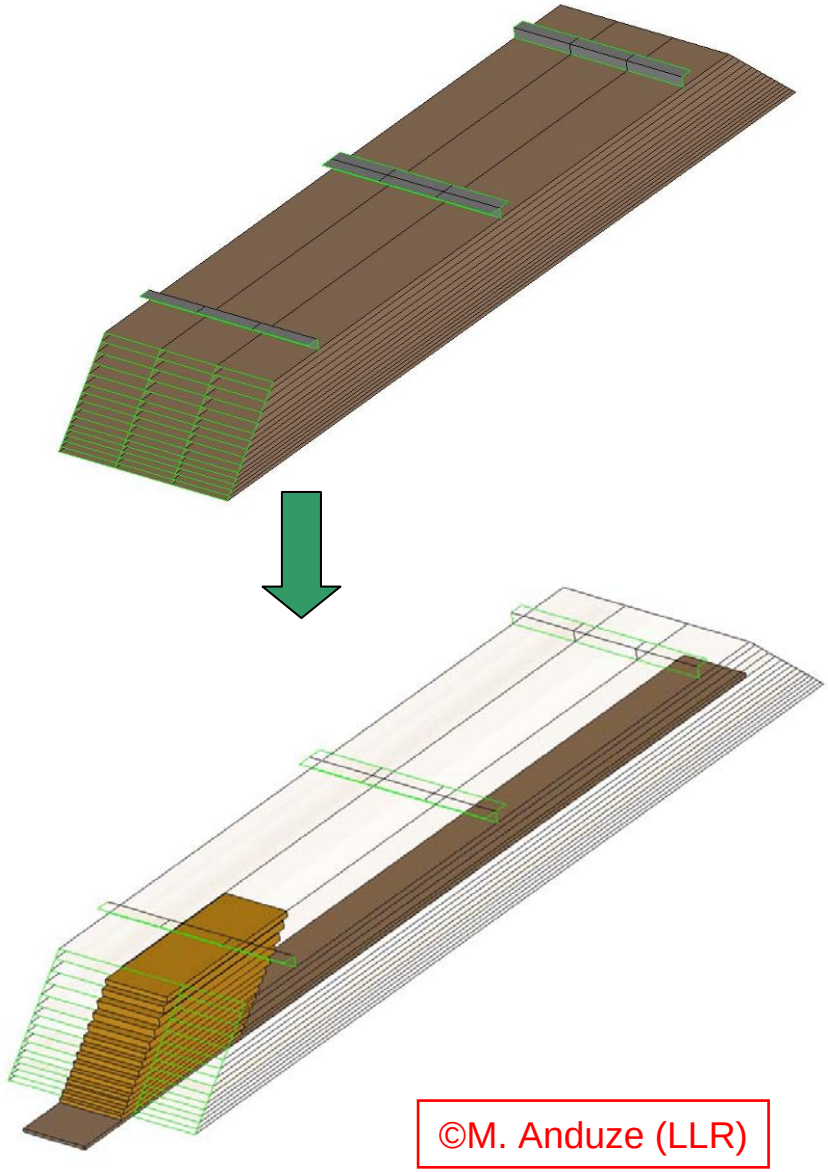
EUDET status meeting
DESY 10 sep 2006

EUDET : ECAL emodule

- **Electromagnetic calorimeter**
  - Prototype of a (~ 1/6) module 0 : **one line & one column**
  - 150 cm long, 12 cm wide 30 layers
  - 1800 + 10800 channels
  - Test full scale mechanics + PCB
  - Can go in test beam
  - Test full integration + edge communications
- **Similar in #channels as physics prototype**



Mechanical R&D (2006-2007)

- *Long Type H structures* :
  - Choice of radiator (W, alloys, Pb ?)
  - Design and fabrication of the long mould (adaptation of prototype mould)
  - Fabrication of validation model (1-3 samples)

- *Half module EUDET* :

  - 1.5 m long ; ≈ 500 Kg
  - real radiator sampling (2 or 3 thickness)

  - Design (mechanical simulations) of the module
  - Optimization of composite sheets : studies of main parameters (thickness, shape ...)
  - Fastening system on HCAL : design and destructive tests too
  - Design and fabrication of the mould
  - Transport tools
  - Fabrication of the structure (end 2007)
  - Mechanical support for beam test in 2008

A not exhaustive silicon R&D list

(largely not yet covered by enough people and institute)

Granularity … as low as possible , pixels not larger than 5x5 mm²

Wafers design

with/o guard ring

cost vs wafers size

AC or not on the wafers (R,C) impact on cost

Alternative approach

MAPS for digital readout (UK)

Assembling

Connection with glue, aging of glue/wafers, study of alternative, etc…

R&D for mass production

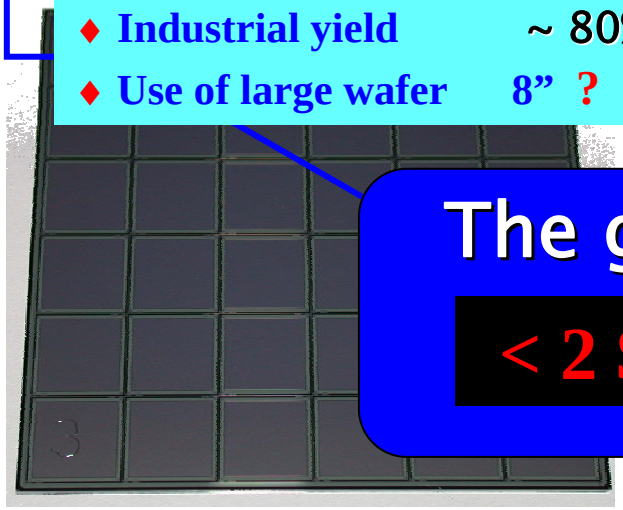
all design of the delivery tests

all design of the wafers calibration device

DETECTORS MATRIX

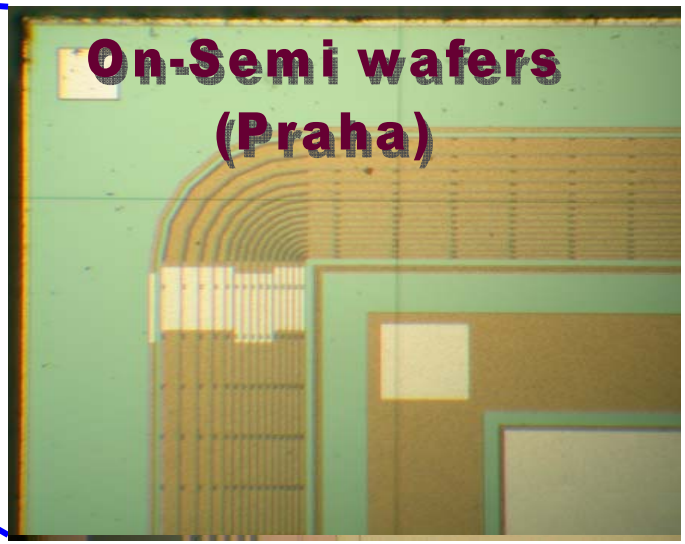
Relatively crude object when compared to a microstrip Matrix for a tracker

- Number of mask ~ 4
- Industrial yield ~ 80% ??
- Use of large wafer 8" ?



The goal is

< 2 $/cm²



ECAL design progress

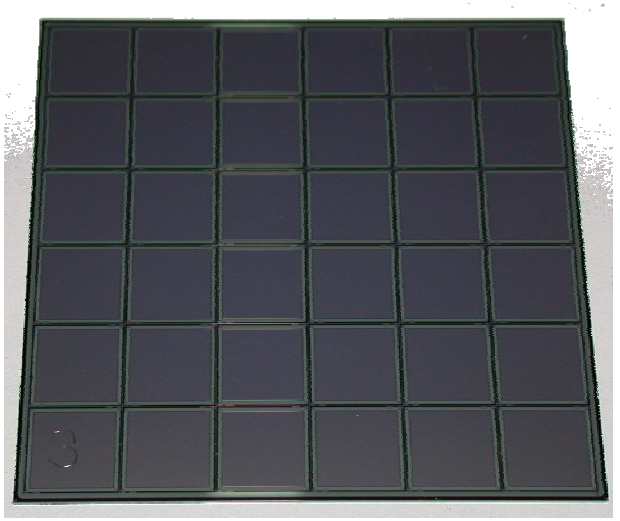
- **Mechanical studies**
  - Support structure : composite alveolae
  - Thermal studies
  - Detector optimization : multiple constraints (physics performance, electronics, cooling, overall detector layout)
  - 1 postdoc at CNRS/EP (Allister Levi-Sanchez)

- **Silicon wafers : many issues to be studied**
  - Granularity
  - AC/DC coupling
  - Fabrication costs

- **Mostly simulation and labour cost for 2006-mid 07**

Developments by CNRS Ecole Polytechnique and Prague

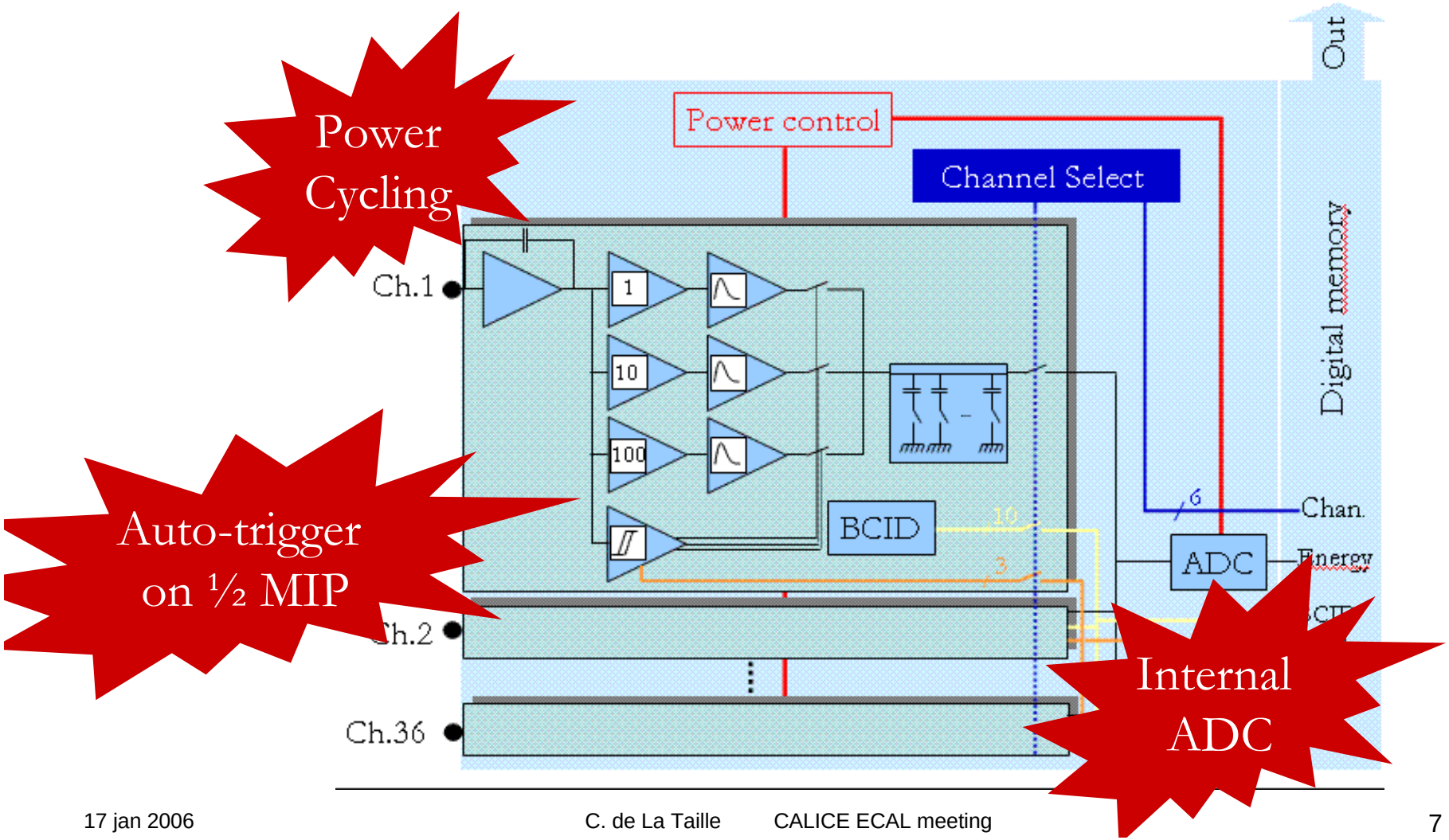
- **CNRS/EP : Mechanical studies of module**
  - Technical consulting : 28,5 k€



- **CNRS/EP : Silicon wafers for Eudet module**
  - Set of masks for production in korea : 10k€
  - Production of wafers in Brasil : 20 k€
- **IPASCR Prague : Silicon wafers for Eudet module**
  - Development of prototypes at ON Semiconductor Roznov
  - Cost : 10.3 k€
- **Financial summary estimate by end 06**
  - CNRS/EP 60k€ spent/ 9k€ requested
  - IPASCR : 10k€ spent/ 6k€ requested

Front End Electronics

- **Prototypes towards final front end ASICs integrated in detector**
  - test power cycling (ON 2ms OFF 200 ms)
  - Test data handling



JRA3 FEE responsibilities and schedule

- **Front-End electronics** (DESY, LAL, LPC, + LLR, LPSC)
  - Complete readout ASIC with power cycling and integrated ADC
  - ASIC for SiPMs and digital HAdronic calorimeter
  - Elementary stitchable motherboards
  - Data concentrator at module end

- **Schedule**
  - ECAL and DHCAL ASIC prototypes : mid 06
  - Second ECAL prototype mid 07
  - AHCAL ASIC prototype : mid 07
  - Small productions to equip modules : mid 08

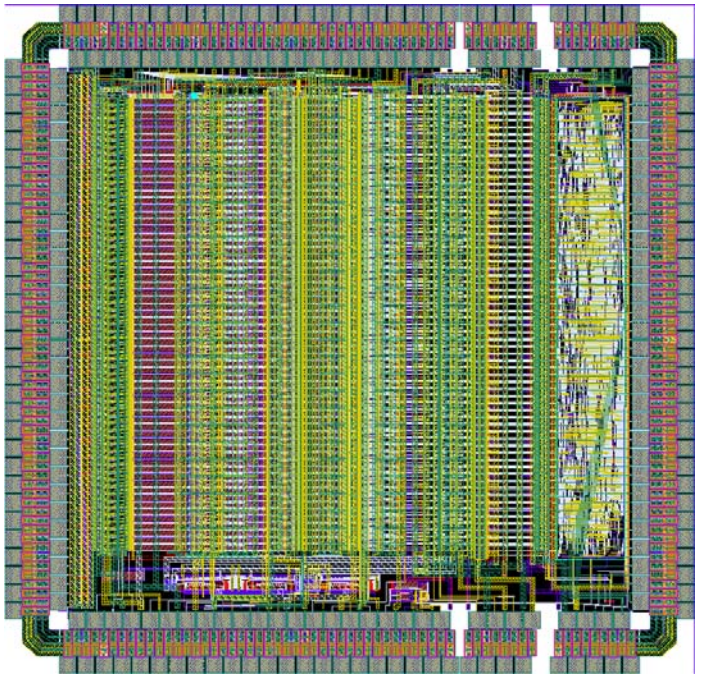
Developments in front-end electronics till sep 06

- **Definition of read-out scheme for 1.5m module**
  - Collaboration CNRS/UK : 1 postdoc at CNRS/EP (Clement Jauffrey)
  - Minimize power dissipation : Token ring scheme
  - EUDET note in preparation

- **Implementation in DHCAL Eudet ASIC**
  - Chip submitted 11 sept 06 ! : CNRS/LAL 18k€
  - Prototype of readout boards to follow
  - 1 postdoc to arrive at LAL in nov06

- **ECAL ASIC to follow in nov 06**
  - CNRS/LAL : 18k€

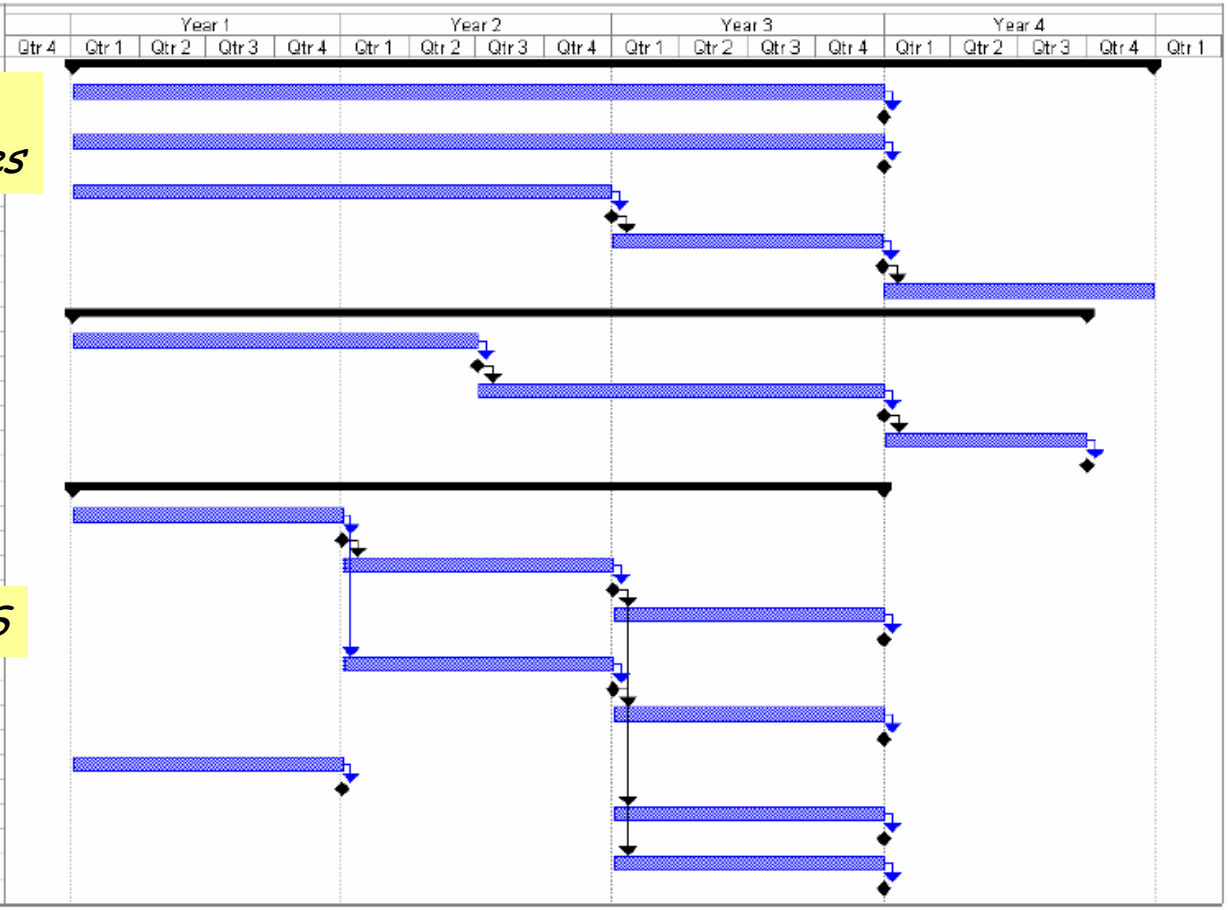
- **Financial summary estimate end 06**
  - 18 (or 36) k€ spent / 21 k requested



Backup slides

Milestones and Deliverables

ID	Task Name
193	**Forward calorimeter**
194	Design of laser positioning system
195	Prototype of laser positioning system
196	Development of sensor test facilities
197	Sensor test facilities ready
198	Development of readout electronics
199	Design of readout electronics
200	Production of readout electronics
201	Readout electronics ready
202	Test of readout electronics
203	**Data acquisition**
204	PCI prototype development
205	Prototype available
206	DAQ system prototype development
207	DAQ system prototype available
208	DAQ system production
209	DAQ system available
210	**Front-end electronics**
211	ECAL/AHCAL ASIC prototype TECH1 development
212	TECH1 prototype available
213	ECAL ASIC prototype TECH2 development
214	ECAL ASIC prototype TECH2 available
215	ECAL ASIC production TECH3
216	ECAL ASIC production TECH3 finalised
217	AHCAL ASIC prototype SiPM2 development
218	AHCAL ASIC prototype SiPM2 available
219	AHCAL ASIC production SiPM3
220	AHCAL ASIC production SiPM3 finalised
221	DHCAL ASIC prototype DHCAL1 development
222	DHCAL ASIC prototype DHCAL1 available
223	ECAL PCB production
224	ECAL PCB available
225	HCAL PCB production
226	HCAL PCB available



- **Not very detailed – but somewhat more rigid than we are used to**

Towards ECAL DAQ : data volume and rate

- **Assuming TESLA like bunch structure**
  - Bunch crossing period within bunch train = 176ns ~ 200ns
  - Number of crossings per bunch train = 4886 ~ 5000
  - Bunch train length = 860μs ~ 1ms
  - Bunch train period =250ms ~ 200ms

- **Raw Data volume**
  - 2 bytes Energy data/Channel, 20 Million channels
  - Raw data per bunch train ~ 20M × 5000 × 2 ~ 200GBytes ECAL
  - No way to digitize inside the ~ ms train
  - 10 kbytes/channel/train ~ 50 kbytes/ch/s
  - Physics data rate : 90 Mbytes/train = ~20 bytes/ch/s ~10^3

- **Zero suppression mandatory**
  - 10^3 rate reduction -> drastic for power dissipation
  - Digitize only signals over 1/2MIP with noise < MIP/10
  - Allow storage in front-end ASIC